SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
SHEET INDEX SUPPORTING INFORMATION	A1	1	2	3	4	5	6	7	8																	
SHEET INDEX (CONT)	A2	1	2	3	4	5	6	7	8																	
	A3	1	2	3	4	5	6	7	8																	
APPARATUS INDEX	A4	1	2	3	3	5	6	6	6																	
OPTION INDEX	A5						6	7	7																	
FS 1 MICROCONTROL	B1AA		2	3	4	4	4	4	4																	
	B1AB		2	3	3	3	3	3	3																	
	B1AC		2	3	4	4	4	4	4																	
	B1AD		2	3	3	3	3	3	3																	
	B1AE		2	3	3	3	3	3	3																	
	B1AF		2	3	4	4	4	4	4																	
	B1AG		2	3	3	3	3	3	3																	
	B1CA	1	2	3	4	4	4	7	7																	
	B1CB	1	2	3	4	4	4	7	7																	
	B1CC	1	2	3	4	4	4	7	7																	
	B1CD	1	2	3	4	4	4	7	7																	
	B1CE	1	2	3	4	4	4	7	7																	
	B1CF	1	2	3	4	4	4	7	7																	
	B1CG	1	2	3	4	4	4	7	7																	
	B1GA		2	3	3	5	5	5	5																	
	B1GB		2	3	3	3	3	3	3																	
	B1GC		2	3	3	5	5	5	5																	
	B1GD		2	3	3	3	3	3	3																	
	B1GE		2	3	4	4	4	4	4																	
	B1GF		2	3	3	3	3	3	3																	
	B1GG		2	3	3	3	3	3	3																	
	B1GH		2	3	3	5	5	5	5																	
	B1GJ		2	3	3	3	3	3	3																	
	B1GK		2	3	3	3	3	3	3																	
	B1GL		2	3	4	5	5	5	5																	
	B1GM		2	3	3	5	5	5	5																	
	B1GN		2	3	4	5	5	5	5																	
	B1GP		2	3	4	5	5	5	5																	
	B1GR		2	3	4	4	4	4	4																	
	B1GT		2	3	4	4	4	4	4																	
	B1GU		2	3	3	5	5	5	5																	
	B1GV		2	3	4	5	5	5	5																	
	B1GW		2	3	3	5	5	5	5																	
	B1GX		2	3	3	3	3	3	3																	
	B1GY		2	3	4	5	5	5	5																	
	B1HA		2	3	4	4	4	4	4																	
	B1HB		2	3	3	3	3	3	3																	
FS 2 DATA MANIPULATION LOGIC (DML)	B2AA		2	3	3	3	3	3	3																	
	B2AB		2	3	3	3	3	3	3																	
	B2AC		2	3	3	3	3	3	3																	
	B2CA	1	2	3	4	4	4	7	7																	
	B2CB	1	2	3	4	4	4	7	7																	
	B2CC	1	2	3	4	4	4	7	7																	
	B2CD	1	2	3	4	4	4	7	7																	
	B2CE	1	2	3	4	4	4	7	7																	
	B2GA		2	3	3	5	5	5	5																	
	B2GB		2	3	3	5	5	5	5																	
	B2GC		2	3	4	5	5	5	5																	
	B2GD		2	3	3	5	5	5	5																	
	B2GE		2	3	3	3	3	3	3																	
	B2GF		2	3	3	3	3	3	3																	
	B2GG		2	3	3	3	3	3	3																	
	B2GH		2	3	4	5	5	5	5																	
	B2GJ		2	3	4	5	5	5	5																	
	B2GK		2	3	3	5	5	5	5																	
	B2GL		2	3	3	3	3	3	3																	
	B2GM		2	3	3	3	3	3	3																	
	B2GN		2	3	3	3	3	3	3																	
	B2GP		2	3	3	5	5	5	5																	
	B2GR		2	3	4	5	5	5	5																	

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
FS 3 GENERAL REGISTERS (R0-R15)	B3AA		2	3	3	3	3	3	3																	
	B3AB		2	3	3	3	3	3	3																	
	B3AC		2	3	3	3	3	3	3																	
	B3CA	1	2	3	3	3	3	7	7																	
	B3CB	1	2	3	3	3	3	7	7																	
	B3CC	1	2	3	3	3	3	7	7																	
	B3CD	1	2	3	3	3	3	7	7																	
	B3CE	1	2	3	3	3	3	7	7																	
	B3GA		2	3	3	3	3	3	3																	
	B3GB		2	3	3	5	5	5	5																	
	B3GC		2	3	3	3	3	3	3																	
FS 4 PROCESSOR BUS CONTROLLER	B4AA		2	3	4	5	5	5	8																	
	B4AB		2	3	3	5	5	5	5																	
	B4AC		2	3	3	5	5	5	5																	
	B4AD		2	3	3	5	5	5	5																	
	B4AE		2	3	4	5	5	5	5																	
	B4AF		2	3	4	5	5	5	5																	
	B4CA	1	2	3	4	5	5	7	8																	
	B4CB	1	2	3	4	5	5	7	7																	
	B4CC	1	2	3	4	5	5	7	7																	
	B4CD	1	2	3	4	5	5	7	7																	
	B4CE	1	2	3	4	5	5	7	7																	
	B4CF	1	2	3	4	5	5	7	7																	
	B4CG	1	2	3	4	5	5	7	7																	
	B4CH		2	3	4	5	5	7	7																	
	B4GA		2	3	3	5	5	5	5																	
	B4GB		2	3	3	5	5	5	5																	
	B4GC		2	3	3	5	5	5	5																	
	B4GD		2	3	4	5	5	5	5																	
	B4GE		2	3	3	5	5	5	5																	
	B4GF		2	3	4	5	5	5	5																	
	B4GG		2	3	4	5	5	5	5																	
	B4GH		2	3	4	5	5	5	5																	
	B4GJ		2	3	3	5	5	5	5																	
	B4GK		2	3	4	5	5	5	5																	
	B4GL		2	3	4	5	5	5	5																	
	B4GM		2	3	4	5	5	5	6																	
	B4GN		2	3	4	5	5	5	5																	
	B4GP		2	3	4	5	5	5	8																	
	B4GR		2	3	4	5	5	5	5																	
	B4GT		2	3	4	5	5	5	5																	
	B4GU		2	3	4	5	5	5	5																	
	B4GV		2	3	3	5	5	5	5																	
	B4GW		2	3	4	5	5	5	5																	
	B4GX		2	3	4	5	5	5	5																	

DWG ISSUE	CD ISSUE	DWG ISSUE	CD ISSUE	DWG ISSUE	CD ISSUE
1	1				

DWG ISSUE	CD ISSUE	DATE ISSUED	DRAWN	APP'D
2A	1 APPX 1A	12-17-75	AS DNR	DJM LAW RFG
3A	1 APPX 2A	12-17-75	AS DNR	DJM LAW RFG
4A	1 APPX 3A	12-15-76	CDD DNR	DJM LEG RFG
5A	1 APPX 4A	6-21-77	SE DNR	DJM LEG JBD
6D	1 APPX 5D	6-21-77	TAB DNR	DJM LEG JBD
7D	1 APPX 6D	12-5-77	NA DNR	DJM LEG MG
8A	1 APPX 7A	2-14-79	AS DNR	DJM LEG LDD

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING, ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK SCHEMATIC	CPS-*
EQUIPMENT DRAWING	J1C050A
MICROPROGRAM STORE CKT	
a. 512 WORDS	SD-4C005-01
b. 1024 WORDS	SD-4C005-02

*- SCHEMATICS OF ALL FA, FB AND FC-CODED CIRCUIT PACKS USED IN THIS CIRCUIT ARE SHOWN ON DRAWINGS NUMBERED WITH A CPS PREFIX FOLLOWED BY THE CODE OF THE PACK, E.G., CPS-FA1010.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE 8A

1N9B

COMMON SYSTEMS

3A CENTRAL CONTROL
CIRCUIT

②

AT&TCO
STANDARD

SD-1C900-01-A1
291 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

SHEET INDEX (CONT)

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
FS 5 SPECIAL REGISTERS	B5AA		2	3	3	3	3	3	3																	
	B5AB		2	3	3	5	5	5	5																	
	B5AC		2	3	4	5	5	5	5																	
	B5AD		2	3	4	5	5	5	5																	
	B5AE		2	3	4	4	4	4	4																	
	B5AF		2	3	3	5	5	5	5																	
	B5CA	1	2	3	4	5	5	5	5																	
	B5CB	1	2	3	4	5	5	5	5																	
	B5CC	1	2	3	4	5	5	5	5																	
	B5CD	1	2	3	4	5	5	5	5																	
	B5GA		2	3	3	3	3	3	3																	
	B5GB		2	3	4	5	5	5	5																	
	B5GC		2	3	3	5	5	5	5																	
	B5GD		2	3	3	5	5	5	5																	
	B5GE		2	3	4	5	5	5	5																	
	B5GF		2	3	4	4	4	4	4																	
	B5GG		2	3	3	5	5	3	5																	
FS 6 DATA TRANSFER CHECK CIRCUITS	B6AA		2	3	3	3	3	3	3																	
	B6AB		2	3	3	3	3	3	3																	
	B6AC		2	3	3	3	3	3	3																	
	B6CA	1	2	3	4	4	4	4	4																	
	B6CB	1	2	3	4	4	4	4	4																	
	B6GA		2	3	3	3	3	3	3																	
	B6GB		2	3	3	3	3	3	3																	
	B6GC		2	3	3	5	5	5	5																	
	B6GD		2	3	3	3	3	3	3																	
	B6GE		2	3	3	3	3	3	3																	
	B6GF		2	3	4	4	4	4	4																	
	B6GG		2	3	3	5	5	5	5																	
	B6GH		2	3	3	5	5	5	5																	
FS 7 CONSOLE FUNCTIONS (INCLUDING PROCESSOR INITIALIZATION HARDWARE)	B7AA		2	3	3	5	5	5	5																	
	B7AB		2	3	4	4	4	4	4																	
	B7AC		2	3	4	4	4	4	4																	
	B7AD		2	3	4	4	4	4	4																	
	B7AE		2	3	3	5	5	5	5																	
	B7AF		2	3	4	4	4	4	4																	
	B7AG		2	3	3	3	3	3	3																	
	B7CA	1	2	3	4	5	5	5	5																	
	B7CB	1	2	3	4	5	5	5	5																	
	B7CC	1	2	3	4	5	5	5	5																	
	B7CD	1	2	3	4	5	5	5	5																	
	B7CE	1	2	3	4	5	5	5	5																	
	B7GA		2	3	4	5	5	5	5																	
	B7GB		2	3	4	5	5	5	5																	
	B7GC		2	3	3	5	5	5	5																	
	B7GD		2	3	3	5	5	5	5																	
	B7GE		2	3	4	5	5	5	5																	
	B7GF		2	3	3	5	5	5	5																	
	B7GG		2	3	3	5	5	5	5																	
	B7GH		2	3	3	5	5	5	5																	
	B7GJ		2	3	3	5	5	5	5																	
	B7GK		2	3	4	5	5	5	5																	

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
FS 8 CLOCK, PROGRAM TIMER AND TIMING COUNTER	B8AA		2	3	4	5	5	5	5																	
	B8AB		2	3	4	4	4	4	4																	
	B8CA	1	2	3	4	4	4	4	4																	
	B8GA		2	3	4	5	5	5	5																	
	B8GB		2	3	3	5	5	5	5																	
	B8GC		2	3	3	5	5	5	5																	
	B8GD		2	3	4	5	5	5	5																	
	B8GE		2	3	3	5	5	5	5																	
	B8GF		2	3	3	5	5	5	5																	
FS 9 MAINTENANCE CHANNEL	B9AA		2	3	3	3	3	3	3																	
	B9AB		2	3	3	3	3	3	3																	
	B9CA	1	2	3	3	3	3	3	3																	
	B9CB	1	2	3	3	3	3	3	3																	
	B9GA		2	3	3	5	5	5	5																	
	B9GB		2	3	3	5	5	5	5																	
	B9GC		2	3	3	5	5	5	5																	
	B9GD		2	3	3	3	3	3	3																	
	B9GE		2	3	3	5	5	5	5																	
	B9GF		2	3	3	5	5	5	5																	
	B9GG		2	3	3	5	5	5	5																	
	B9GH		2	3	3	5	5	5	5																	
	B9GJ		2	3	3	5	5	5	5																	
	B9GK		2	3	3	3	3	3	3																	
	B9GL		2	3	3	3	3	3	3																	
	B9GM		2	3	3	3	3	3	3																	
	B9GN		2	3	3	5	5	5	5																	
	B9GP		2	3	3	3	3	3	[illegible]																	
FS 10 I/0 CHANNELS	B10AA		2	3	3	3	3	3	3																	
	B10AB		2	3	3	5	5	5	5																	
	B10AC		2	3	3	5	5	5	5																	
	B10AD		2	3	3	3	3	3	3																	
	B10CA	1	2	3	3	5	5	5	5																	
	B10CB	1	2	3	3	5	5	5	5																	
	B10CC	1	2	3	3	5	5	5	5																	
	B10CD	1	2	3	3	5	5	5	5																	
	B10CE	1	2	3	3	5	5	5	5																	
	B10CF	1	2	3	3	5	5	5	5																	
	B10GA		2	3	3	5	5	5	5																	
	B10GB		2	3	3	5	5	5	5																	
	B10GC		2	3	3	5	5	5	5																	
	B10GD		2	3	3	5	5	5	5																	
	B10GE		2	3	3	3	3	3	3																	
	B10GF		2	3	3	5	5	5	5																	
	B10GG		2	3	3	5	5	5	5																	
	B10GH		2	3	3	3	3	3	3																	
	B10GJ		2	3	3	5	5	5	5																	

DRAWING ISSUE

ISSUE
8A

3A CENTRAL CONTROL

②

SD-1C900-01-A2

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

SHEET INDEX (CONT)

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
FS 11 EXTENDED MAIN MEMORY INTERFACE	B11AA		2	3	4	5	5	5	5																	
	B11AB		2	3	4	4	4	4	4																	
	B11CA	1	2	3	4	5	5	5	5																	
	B11CB	1	2	3	4	5	5	5	5																	
	B11GA		2	3	3	5	5	5	5																	
	B11GB		2	3	4	5	5	5	5																	
	B11GC		2	3	3	3	3	3	3																	
	B11GD		2	3	3	3	3	3	3																	
	B11GE		2	3	4	4	4	4	4																	
FS 12 MICROPROGRAM STORE (4096 X 32-BIT WORDS)	B12AA		2	3	4	4	6	6	6																	
	B12AB		2	3	4	4	6	6	6																	
SHEET CANCELED ON ISSUE 4A	B12AC																									
FS 12 MICROPROGRAM STORE (4096 X 32-BIT WORDS)	B12CA	1	2	3	4	4	6	6	6																	
	B12CB	1	2	3	4	4	6	6	6																	
	B12CC	1	2	3	4	4	6	6	6																	
	B12CD	1	2	3	4	4	6	6	6																	
	B12CE	1	2	3	4	4	6	6	6																	
	B12CF	1	2	3	4	4	6	6	6																	
	B12CG	1	2	3	4	4	6	6	6																	
	B12CH	1	2	3	4	4	6	6	6																	
	B12GA		2	3	4	4	6	6	6																	
	B12GB		2	3	3	5	6	6	6																	
	B12GC		2	3	4	5	6	6	6																	
	B12GD						6	6	6																	
FS 13 PROTECTION CIRCUIT	B13AA		2	3	3	5	5	5	5																	
	B13AB		2	3	3	5	5	5	5																	
	B13CA	1	2	3	3	5	5	7	7																	
	B13CB	1	2	3	3	5	5	7	7																	
	B13GA		2	3	3	5	5	5	5																	
FS 14 POWER	B14AA	1	2	3	3	3	6	7	7																	
	B14AB	1	2	3	3	3	6	7	7																	
	B14AC	1	2	3	4	4	6	7	7																	
	B14AD		2	3	3	3	6	7	7																	
	B14AE		2	3	3	3	6	7	7																	
	B14AF		2	3	3	3	3	7	7																	
SHEET CANCELED ON ISSUE 4A	B14AG																									
FS 14 POWER	B14CA	1	2	3	3	3	6	7	7																	
	B14CB	1	2	3	3	3	6	7	7																	
	B14CC	1	2	3	3	3	6	7	7																	
	B14CD	1	2	3	3	3	6	7	7																	
	B14CE	1	2	3	3	3	6	7	7																	
	B14CF	1	2	3	3	3	6	7	7																	
	B14CG	1	2	3	3	3	6	7	7																	

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
APP FIG. 1	C1	1	2	3	3	5	6	6	6																	
	C2	1	2	3	3	5	6	6	6																	
APP FIG. 2-5	C3	1	2	3	3	5	6	6	6																	
SHEET CANCELED ON ISSUE 2A	C4																									
CIRCUIT NOTES	D1	1	2	3	3	5	6	7	7																	
EQUIPMENT NOTES	D2	1	2	3	4	4	6	7	7																	
INFORMATION NOTES	D3	1	2	3	4	4	4	4	4																	
	D4	1	2	3	3	3	3	3	3																	
	D5	1	2	3	3	3	3	3	3																	
	D6	1	2	3	3	3	3	3	3																	
	D7	1	2	3	3	3	3	3	3																	
	D8	1	2	3	3	3	3	3	3																	
	D9	1	2	3	3	3	3	3	3																	
	D10	1	2	3	3	5	5	5	5																	
	D11	1	2	3	3	5	5	5	5																	
	D12	1	2	3	3	5	5	5	5																	
	D13	1	2	3	3	5	5	[illegible]	5																	
	D14	1	2	3	4	5	5	5	5																	
	D15	1	2	3	3	3	6	6	6																	
	D16	1	2	3	3	5	5	5	5																	
	D17	1	2	3	4	5	5	5	5																	
	D18	1	2	3	3	3	3	3	3																	
	D19		2	3	4	4	4	4	4																	
	D20		2	3	3	5	5	5	5																	
	D21		2	3	3	3	3	3	3																	
	D22		2	3	3	5	5	5	5																	
	D23		2	3	3	3	3	3	3																	
	D24		2	3	4	5	5	5	5																	
	D25		2	3	3	5	5	5	5																	
	D26		2	3	3	3	3	3	3																	
	D27		2	3	3	3	3	3	3																	
	D28		2	3	3	3	3	3	[illegible]																	
	D29		2	3	3	3	3	[illegible]	3																	
CAD NOTES	GB1	1	2	3	3	3	3	3	3																	
CAD 1 UNIT SYMBOL	GB2	1	2	3	4	5	5	5	5																	
	GB3	1	2	3	4	5	5	5	5																	
	GB4	1	2	3	4	4	4	4	4																	
	GB5	1	2	3	4	4	4	4	4																	
	GB6	1	2	3	4	4	6	7	7																	
	GB7	1	2	3	4	5	6	7	7																	
CAD 2-5	GB8	1	2	3	4	4	4	4	4																	
CAD 6,7, P/0 CAD 8	GB9	1	2	3	4	4	6	6	6																	
P/0 CAD 8	GB10	1	2	3	4	4	4	4	4																	
SHEET CANCELED ON ISSUE 2A	GB11																									

DRAWING ISSUE

ISSUE 8A

3A CENTRAL CONTROL ②

SD-1C900-01-A3

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PRINTED IN U.S.A.

APPARATUS INDEX

CIRCUIT PACKS

EQUIP LOC	APP NO.	FIGURE SH NO.
02-01	1	C1
02-02	1	C1
02-03	1	C1
02-04	5	C3
02-05	2	C3
02-06	2	C3
02-07	2	C3
02-08	1	C1
02-09	1	C1
02-10	1	C1
02-11	1	C1
02-12	1	C1
02-13	1	C1
02-14	1	C1
02-16	1	C1
02-17	1	C1
02-18	1	C1
02-19	1	C1
02-20	1	C1
02-21	1	C1
02-22	1	C1
02-23	1	C1
02-24	1	C1
02-25	1	C1
02-26	1	C1
02-27	1	C1
02-28	1	C1
02-29	1	C1
02-31	1	C1
02-32	1	C1
02-33	1	C1
02-34	1	C1
02-35	1	C1
02-36	1	C1
02-37	1	C1
02-38	1	C1
02-39	1	C1
02-40	1	C1
02-41	1	C1
02-42	1	C1
02-43	1	C1
02-44	1	C1
06-01	1	C1
06-02	1	C1
06-03	1	C1
06-04	1	C1
06-05	5	C3
06-06	1	C1
06-07	5	C3
06-08	5	C3
06-09	1	C1
06-10	1	C1
06-11	1	C1
06-12	1	C1
06-13	1	C1
06-14	1	C1
06-16	1	C1
06-17	1	C1
06-18	1	C1
06-19	1	C2
06-20	1	C2
06-21	1	C2
06-22	1	C2
06-23	1	C2

CIRCUIT PACKS(CONT)

EQUIP LOC	APP NO.	FIGURE SH NO.
06-24	1	C2
06-25	1	C2
06-26	1	C2
06-27	1	C2
06-28	1	C2
06-29	1	C2
06-31	1	C2
06-32	1	C2
06-33	1	C2
06-34	1	C2
06-35	1	C2
06-36	1	C2
06-37	1	C2
06-38	1	C2
06-39	1	C2
06-40	1	C2
06-41	1	C2
06-42	1	C2
06-43	1	C2
06-44	1	C2
10-01	1	C2
10-02	1	C2
10-03	1	C2
10-04	1	C2
10-05	1	C2
10-06	1	C2
10-07	3	C3
10-08	3	C3
10-09	3	C3
10-10	3	C3
10-11	4	C3
10-12	4	C3
10-13	4	C3
10-14	4	C3
10-16	1	C2
10-17	1	C2
10-18	1	C2
10-19	1	C2
10-20	1	C2
10-21	1	C2
10-22	1	C2
10-23	1	C2
10-24	1	C2
10-25	1	C2
10-26	1	C2
10-27	1	C2
10-28	1	C2
10-29	1	C2

DESIG		
+12VREF	1	C2
3V054A.B	1	C1
3V054C.D	1	C1
3V054E.F	1	C1
3V058A.B	1	C1
3V058C.F	1	C2
3V058D.E	1	C1
3V062A.B	1	C2
3V062C	1	C2
CLOCK	1	C2
DMLORPLG	1	C2
DML1RPHG	1	C2
DML00700	1	C2

CIRCUIT PACKS(CONT)

DESIG	APP NO.	FIG. SH NO.
DML01508	1	C2
DML01916	1	C2
DML10700	1	C2
DML11508	1	C2
DML11916	1	C2
FCHECKER	1	C1
FDECODER	1	C2
IO00SCA	1	C2
IO00SCB	1	C2
IO01SCA	3	C3
IO01SCB	3	C3
IO02SCA	4	C3
IO02SCB	4	C3
IOD00	1	C2
IOD01	3	C3
IOD02	4	C3
IOS00	1	C2
IOS01	3	C3
IOS02	4	C3
MC B1	1	C1
MC B2	1	C1
MC B3	1	C1
MC B4	1	C2
MC B5	1	C2
MC B6	1	C2
MC B7	1	C1
MCH10-00	1	C1
MCH21-11	1	C1
MCHCNTRL	1	C1
MP0.0	1	C1
MP0.1	1	C2
MP1.0	1	C1
MP1.1	1	C2
MP2.0	1	C1
MP2.1	1	C2
MP3.0	1	C1
MP3.1	1	C2
MP4.0	1	C1
MP4.1	1	C2
MP5.0	1	C1
MP5.1	1	C2
MP6.0	1	C1
MP6.1	1	C2
MP7.0	1	C1
MP7.1	1	C2
PBC0	1	C1
PBC1	1	C1
PROT00	5	C3
PROT01	5	C3
PROT02	5	C3
PROT03	5	C3
SPARE	1	C1
SPARE	1	C1
SPARE	1	C2
SPARE	1	C2
STBT2116	2	C3
STBT2722	2	C3
STBTPH28	2	C3
TCHECKER	1	C1
TDECODER	1	C2
TS1	1	C2
TS2	1	C2
TS3	1	C2
TS4	1	C2

CIRCUIT PACKS(CONT)

DESIG	APP NO.	FIG. SH NO.
TS5	1	C2
TS6	1	C2
TS7	1	C2
TS8	1	C2
TS9	1	C2

CIRCUIT PACK-CP

DESIG	LOCATION FS/SYM	APPFIG	EQPT
+12VREF	14/9	1	10-28
3V054A.B	14/1	1	02-01
3V054C.D	14/2	1	02-14
3V054E.F	14/3	1	02-44
3V058A.B	14/4	1	06-01
3V058C.F	14/6	1	06-44
3V058D.E	14/5	1	06-02
3V062A.B	14/8	1	10-29
3V062C	14/7	1	10-01
ADRPTPRD	4/4	1	02-25
BACK.MSB	6/4	1	02-25
CLOCK	8/3	1	06-31
CPANITRF	7/1	1	06-06
CRYS OSC	8/1	1	06-29
C.TA.LOG	7/3	1	02-24
DB09-00	7/5	1	10-23
DBHL1910	7/4	1	10-22
DISENBPO	7/20	1	06-06
DMLORPLG	2/1	1	06-26
DML1RPHG	2/5	1	06-23
DML00700	2/4	1	06-27
DML01508	2/3	1	06-25
DML01916	2/2	1	06-28
DML10700	2/8	1	06-24
DML11508	2/7	1	06-22
DML11916	2/6	1	06-21
DMLMATCH	2/9	1	06-20
DSR	4/2	1	02-23
ER09-00	5/2	1	10-23
ERHL1910	5/1	1	10-22
FCHECKER	6/2	1	06-04
FDECODER	1/13	1	06-33
GBPCHECK	6/3	1	06-20
GRBT0800	3/9	1	06-09
GRBT0901	3/8	1	06-10
GRBT1002	3/7	1	06-11
GRBT1103	3/6	1	06-12
GRBT1204	3/5	1	06-13
GRBT1305	3/4	1	06-14
GRBT1406	3/3	1	06-16
GRBT1507	3/2	1	06-17
GRBTPHPL	3/1	1	06-18
INTRPLOG	5/3	1	02-25
IO00SCA	10/3	1	10-05
IO00SCB	10/4	1	10-06
IO01SCA	10/7	3	10-09
IO01SCB	10/8	3	10-10
IO02SCA	10/11	4	10-13
IO02SCB	10/12	4	10-14
IO CHCHK	6/5	1	02-31
IOD00	10/2	1	10-04
IOD01	10/6	3	10-08
IOD02	10/10	4	10-12
IOS00	10/1	1	10-03
IOS01	10/5	3	10-07
IOS02	10/9	4	10-11
IOTIM	8/5	1	06-29
MC B1	1/3	1	02-35
MC B2	1/2	1	02-34
MC B3	1/1	1	02-33
MC B4	1/4	1	06-32
MC B5	1/7	1	06-19
MC B6	1/5	1	06-35
MC B7	1/8	1	02-32

CIRLUIT PACK-CP (CONT)

DESIG	LOCATION FS/SYM	APPFIG	EQPT
MC B8	1/6	1	02-31
MCH10-00	9/3	1	02-29
MCH21-11	9/2	1	02-28
MCHCNTRL	9/4	1	02-27
MISCDECB	1/9	1	06-06
MISCDECC	1/12	1	02-19
MISCDECD	1/14	1	02-20
MISCDECE	1/10	1	02-2[illegible]
MISCKT	7/6	1	06-06
MP0.0	12/8	1	02-36
MP0.1	12/7	1	06-36
MP1.0	12/6	1	02-37
MP1.1	12/5	1	06-37
MP2.0	12/4	1	02-38
MP2.1	12/3	1	06-38
MP3.0	12/2	1	02-39
MP3.1	12/1	1	06-39
MP4.0	12/16	1	02-40
MP4.1	12/15	1	06-40
MP5.0	12/14	1	02-41
MP5.1	12/13	1	06-41
MP6.0	12/12	1	02-42
MP6.1	12/11	1	06-42
MP7.0	12/10	1	02-43
MP7.1	12/9	1	06-43
MRFLOGIC	7/19	1	02-25
MTBT0800	7/18	1	02-08
MTRT0901	7/17	1	02-09
MTBT1002	7/16	1	02-10
MTBT1103	7/15	1	02-11
MTBT1204	7/14	1	02-12
MTBT1305	7/13	1	02-13
MTBT1406	7/12	1	02-16
MTBT1507	7/11	1	02-17
MTBT1816	7/10	1	02-19
MTBT1917	7/9	1	02-20
MTBTPHPL	7/8	1	02-18
MTHENLGC	7/7	1	06-06
PBC0	4/1	1	02-21
PBC1	4/3	1	02-22
PROT00	13/1	5	06-05
PROT01	13/2	5	06-07
PROT02	13/3	5	06-08
PROT03	13/4	5	02-04
PT.TC	8/4	1	02-24
REG.SEL	7/2	1	02-31
SPR08.00	5/14	1	06-09
SPR09.01	5/13	1	06-10
SPR10.02	5/12	1	06-11
SPR11.03	5/11	1	06-12
SPR12.04	5/10	1	06-13
SPR13.05	5/9	1	06-14
SPR14.06	5/8	1	06-16
SPR15.07	5/7	1	06-17
SPR18.16	5/6	1	02-19

CIRCUIT PACK-CP (CONT)

DESIG	LOCATION FS/SYM	APPFIG	EQPT
SPR19.17	5/5	1	02-20
SPRPH.PL	5/4	1	06-18
SSPINTRF	7/22	1	06-06
SSPTRNSF	7/21	1	02-26
STBT0800	4/15	1	02-08
STBT0901	4/14	1	02-09
STBT1002	4/13	1	02-10
STBT1103	4/12	1	02-11
STBT1204	4/11	1	02-12
STBT1305	4/10	1	02-13
STBT1406	4/9	1	02-16
STBT1507	4/8	1	02-17
STBT1816	4/7	1	02-19
STBT1917	4/6	1	02-20
STBT2116	11/3	2	02-05
STBT2722	11/2	2	02-06
STBTPH28	11/1	2	02-07
STBTPHPL	4/5	1	02-18
TCHECKER	6/1	1	02-02
TDECODER	1/11	1	06-34
TRNSFINT	9/1	1	02-26
TTMO	8/2	1	06-29

CONNECTOR

DESIG	LOCATION FS/SYM	APPFIG	EQPT
SPARE	14/11	1	06-03
SPARE	14/10	1	02-03
SPARE	14/19	1	10-24
SPARE	14/20	1	10-25
TS1	14/12	1	10-02
TS2	14/13	1	10-16
TS3	14/14	1	10-17
TS4	14/15	1	10-18
TS5	14/16	1	10-19
TS6	14/17	1	10-20
TS7	14/18	1	10-21
TS8	14/21	1	10-26
TS9	14/22	1	10-27

ISSUE
6D

3A CENTRAL CONTROL

BELL TELEPHONE LABORATORIES
INCORPORATED

DWG SIZE
C2

SD-1C900-01-A4

SD-1C900-01-A4

OPTION INDEX

APP OR WRG	RATED ON ISSUE	REF NOTES	LOCATION
Z	A&M 6		12/(1-16),14/(3,6,25,28)
Y	STD 6		1/7,2/(6,7,9),3/(1-6), 4/(1-3,5-11),13/(1-6), 14/(1,2,4,8,10)
X	MD 7		1/7,2/(6,7,9),3/(1-6), 4/(1-3,5-11),13/(1-6), 14/(1,2,4,8,10)
W	STD 7		1/7,2/(6,7,9),3/(1-6), 4/(1-3,5-11),13/(1-6), 14/(1,2,4,8,10)

ISSUE
7D

3A CENTRAL CONTROL

②

SD-1C900-01-A5

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

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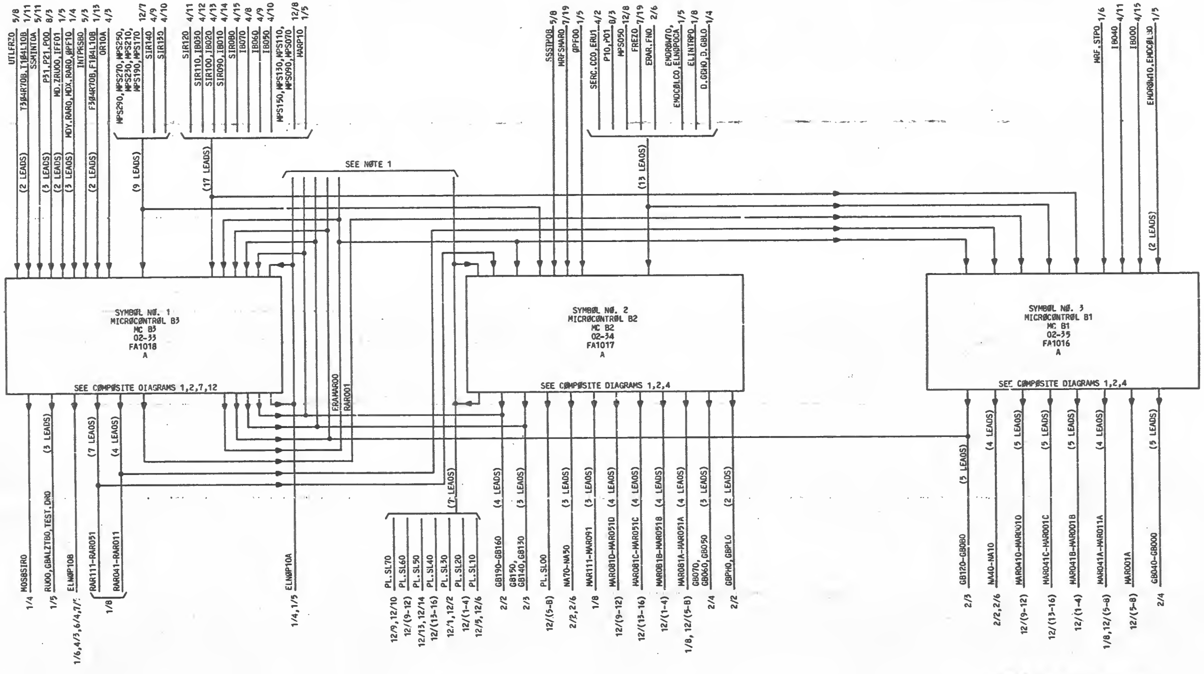
PART OF FS I

MICROCONTROL
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (OI). ALL OFF-PAGE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.
2. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 1
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

②

DWG SIZE	ISSUE
6S	4A

BELL LABORATORIES

SD-1C900-01

BIAA

E-7021 (12-73)

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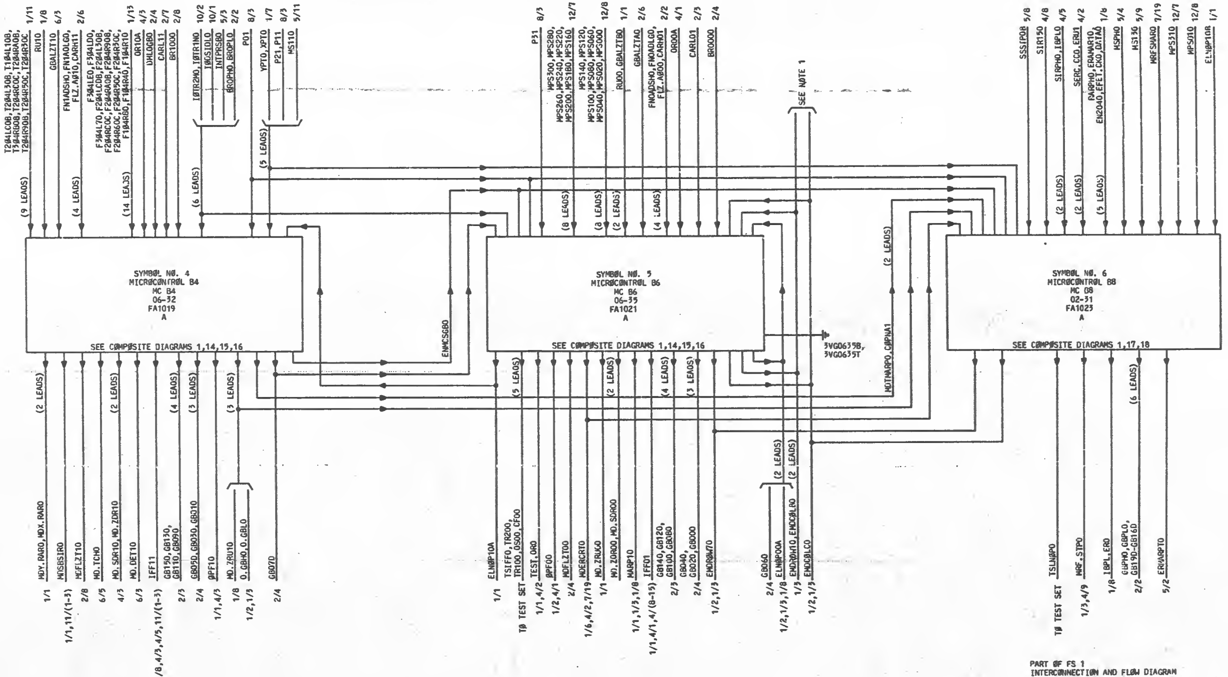
PART OF FS 1

MICROCONTROL
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (OI). ALL OFF-PAGE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.

2. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 1
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES | SD-1C900-01 | B1AB

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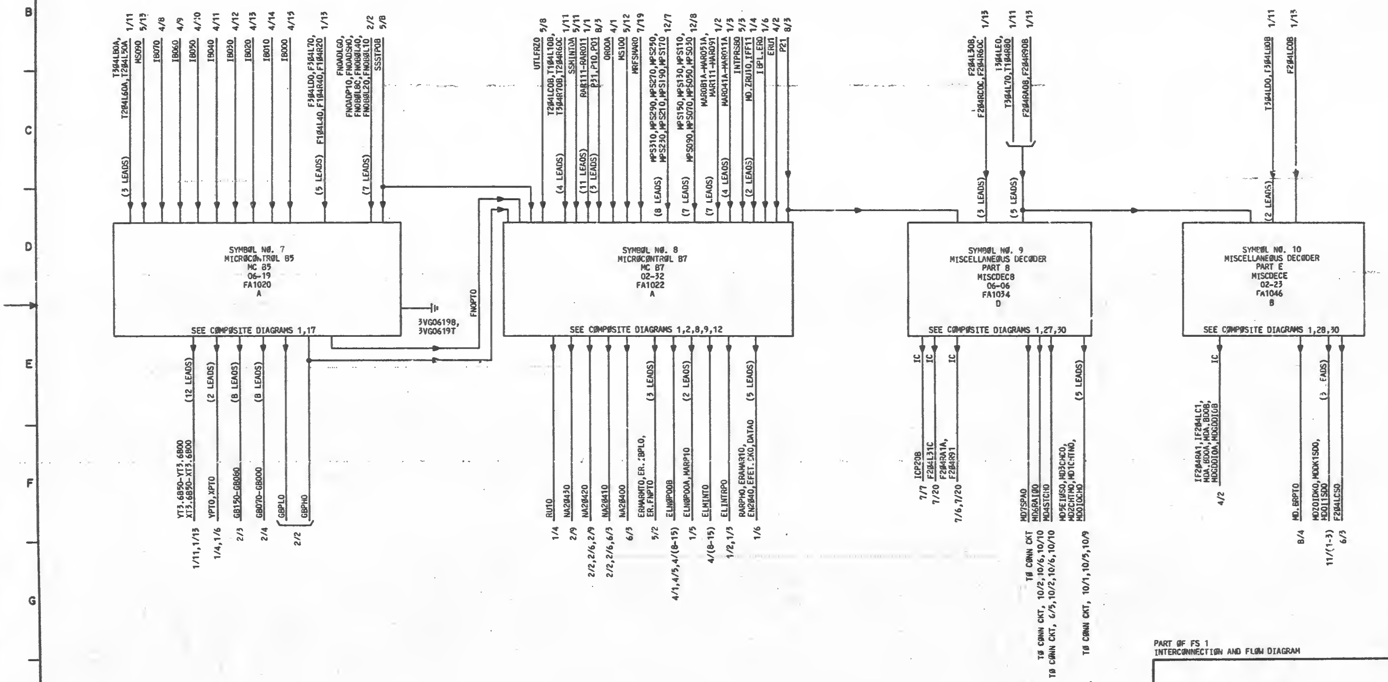
PART OF FS I

MICROCONTROL
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 1
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	BIAC

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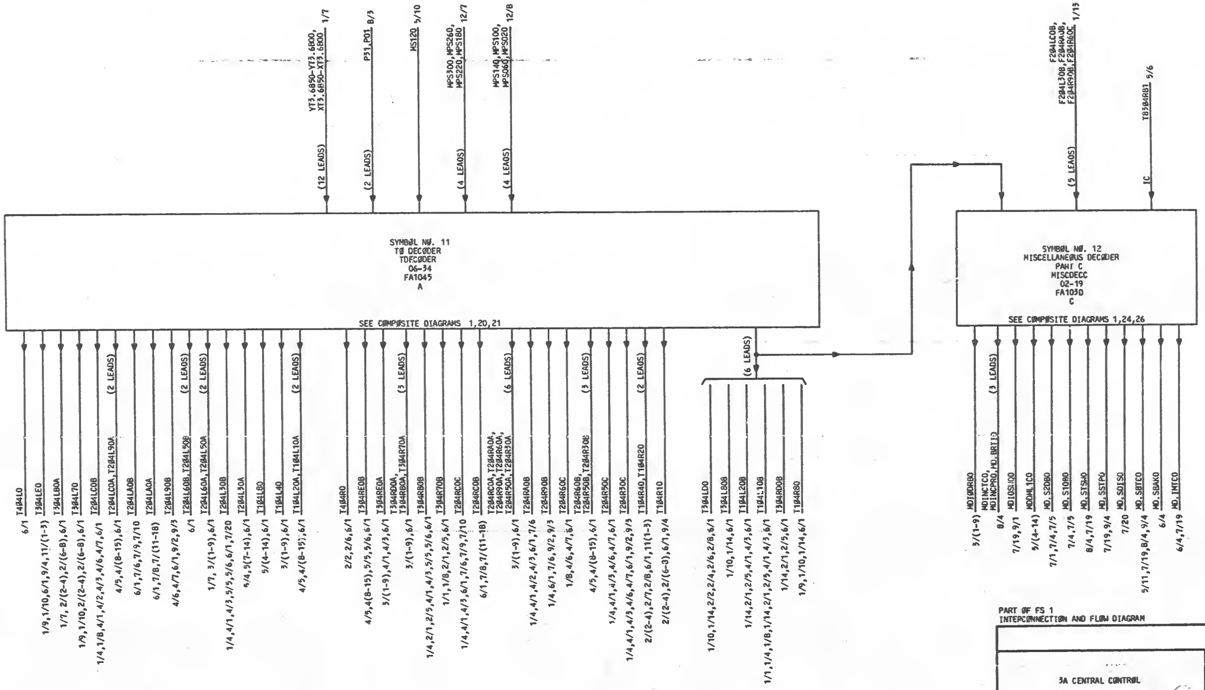
PART OF FS I

MICROCONTROL
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



YT3.6B50-YT3.6B00,
XT3.6B50-XT3.6B00 1/7
(12 LEADS)
P31,P01 B/3
(2 LEADS)
MS120 5/10
MPS300,MPS260,
MPS220,MPS180 12/7
(4 LEADS)
MPS140,MPS100,
MPS060,MPS020 12/8
(4 LEADS)
SYMBOL NO. 11
TO DECODER
TDECODER
06-34
FA1045
A
SEE COMPOSITE DIAGRAMS 1,20,21
T404L0 6/1
T304LE0 1/9,1/10,6/1,9/4,11/(1-3)
T304LB0A 1/7, 2/(2-4),2/(6-8),6/1
T304L70 1/9,1/10,2/(2-4),2/(6-8),6/1
T204LC0B 1/4,1/8,4/1,4/2,4/3,4/6,4/7,6/1
(2 LEADS)
T204LC0A,T204L90A 4/5,4/(8-15),6/1
T204LA0B 6/1,7/6,7/9,7/10
T204LA0A 6/1,7/8,7/(11-18)
T204L90B 4/6,4/7,6/1,9/2,9/3
(2 LEADS)
T204L60B,T204L50B 6/1
(2 LEADS)
T204L60A,T204L50A 1/7, 3/(1-9),6/1
T204L30B 1/4,4/1,4/3,5/5,5/6,6/1,7/20
T204L30A 4/4,5(7-14),6/1
T104L80 5/(4-14),6/1
T104L40 3/(1-9),6/1
(2 LEADS)
T104L20A,T104L10A 4/5,4/(8-15),6/1
T404R0 2/2,2/6,6/1
T304RE0B 4/5,4(8-15),5/5,5/6,6/1
T304RE0A 3/(1-9),4/1,4/3,6/1
(3 LEADS)
T304RD0A,
T304RB0A,T304R70A 3/(1-9),6/1
T304RB0B 1/4,2/1,2/5,4/1,4/3,5/5,5/6,6/1
T304R70B 1/1,1/8,2/1,2/5,6/1
T204RC0C 1/4,4/1,4/3,6/1,7/6,7/9,7/10
T204RC0B 6/1,7/8,7/(11-18)
(6 LEADS)
T204RC0A,T204RA0A,
T204R90A,T204R60A,
T204R50A,T204R30A 3/(1-9),6/1
T204RA0B 1/4,4/1,4/2,4/3,6/1,7/6
T204R90B 1/4,6/1,7/6,9/2,9/3
T204R60C 1/8,4/6,4/7,6/1
(3 LEADS)
T204R60B,
T204R50B,T204R30B 4/5,4/(8-15),6/1
T204R50C 1/4,4/1,4/3,4/6,4/7,6/1
T204R30C 1/4,4/1,4/3,4/6,4/7,6/1,9/2,9/3
(2 LEADS)
T104R40,T104R20 2/(2-4),2/7,2/8,6/1,11(1-3)
T104R10 2/(2-4),2/(6-3),6/1,9/4
(6 LEADS)
T304LD0 1/10,1/14,2/2,2/4,2/6,2/8,6/1
T304L808 1/10,1/14,6/1
T104L20B 1/14,2/1,2/5,4/1,4/3,6/1
T104L108 1/1,1/4,1/8,1/14,2/1,2/5,4/1,4/3,6/1
T304RD0B 1/14,2/1,2/5,6/1
T104R80 1/9,1/10,1/14,6/1
F204LC0B,
F204L30B,F204RA0B,
F204R90B,F204R60C 1/13
(5 LEADS)
T8304RB1 5/6
1C
SYMBOL NO. 12
MISCELLANEOUS DECODER
PART C
MISCDECC
02-19
FA103D
C
SEE COMPOSITE DIAGRAMS 1,24,26
MDI0DRB0 3/(1-9)
(3 LEADS)
MDINCTC0,
MDINCPR0,MD.BRTI0 8/4
MDI0SU00 7/19,9/1
MD0ML1C0 5/(4-14)
MD.S2DB0 7/1,7/4,7/5
MD.S10R0 7/4,7/5
MD.STSW0 8/4,7/19
MD.SSTP0 7/19,9/4
MD.SDIS0 7/20
MD.SBTC0 5/11,7/19,8/4,9/4
MD.SBAK0 6/4
MD.IMTC0 6/4,7/19

PART OF FS 1
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	BIAD

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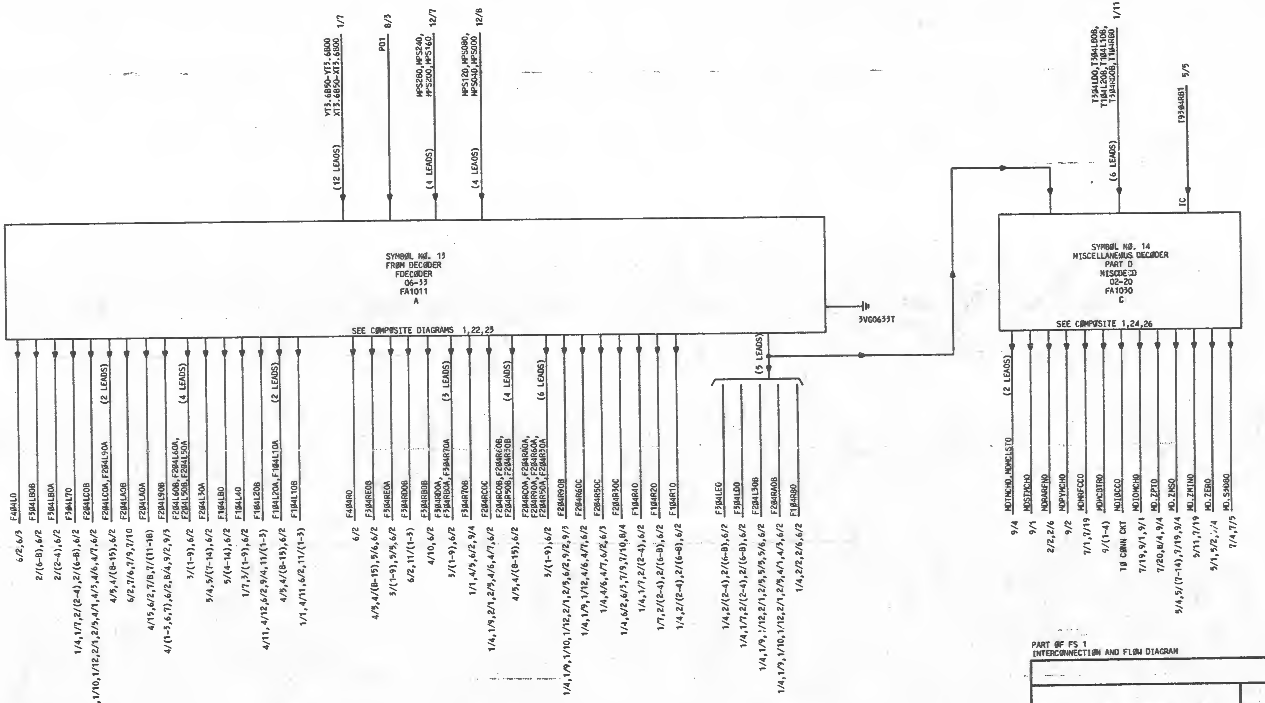
E-7421 (12-75)

PART OF FS I

MICROCONTROL
INTERCONNECTION AND FLOW DIAGRAM

NOTE:
1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.


YT3.6B50-YT3.6B00 XT3.6B50-XT3.6B00 1/7
(12 LEADS)
P01 8/3
MPS280,MPS240, MPS200,MPS160 12/7
(4 LEADS)
MPS120,MPS080, MPS040,MPS000 12/8
(4 LEADS)
T304LD0,T304LD0B, T104L20B,T104L10B, T304RD0B,T104RB0 1/11
(6 LEADS)
T9304RB1 5/5
IC
SYMBOL NO. 13
FROM DECODER
FDECODER
06-33
FA1011
A
SEE COMPOSITE DIAGRAMS 1,22,23
3VG0633T
SYMBOL NO. 14
MISCELLANEOUS DECODER
PART D
MISCDECD
02-20
FA1030
C
SEE COMPOSITE 1,24,26
F404L0 6/2,6/3
F304LB0B 2/(6-B),6/2
F304LB0A 2/(2-4),6/2
F304L70 1/4,1/7,2/(2-4),2/(6-B),6/2
F204LC0B 1/4,1/10,1/12,2/1,2/5,4/1,4/3,4/6,4/7,6/2
(2 LEADS)
F204LC0A,F204L90A 4/5,4/(8-15),6/2
F204LA0B 6/2,7/6,7/9,7/10
F204LA0A 4/15,6/2,7/8,7/(11-18)
F204L90B 4/(1-3,6,7),6/2,8/4,9/2,9/3
(4 LEADS)
F204L60B,F204L60A, F204L50B,F204L50A 3/(1-9),6/2
F204L30A 5/4,5/(7-14),6/2
F104LB0 5/(4-14),6/2
F104L40 1/7,3/(1-9),6/2
F104L20B 4/11,4/12,6/2,9/4,11/(1-3)
(2 LEADS)
F104L20A,F104L10A 4/5,4/(8-15),6/2
F104L10B 1/1,4/11,6/2,11/(1-3)
F404R0 6/2
F304RE0B 4/5,4/(B-15),5/6,6/2
F304RE0A 3/(1-9),5/5,6/2
F304RD0B 6/2,11/(1-3)
F304RB0B 4/10,6/2
(3 LEADS)
F304RD0A, F304RB0A,F304R70A 3/(1-9),6/2
F304R70B 1/1,4/5,6/2,9/4
F204RC0C 1/4,1/9,2/1,2/5,4/6,4/7,6/2
(4 LEADS)
F204RC0B,F204R60B, F204R50B,F204R30B 4/5,4/(8-15),6/2
(6 LEADS)
F204RC0A,F204RA0A, F204R90A,F204R60A, F204R50A,F204R30A 3/(1-9),6/2
F204R90B 1/4,1/9,1/10,1/12,2/1,2/5,6/2,9/2,9/3
F204R60C 1/4,1/9,1/12,4/6,4/7,6/2
F204R50C 1/4,4/6,4/7,6/2,6/3
F204R30C 1/4,6/2,6/3,7/9,7/10,8/4
F104R40 1/4,1/7,2/(2-4),6/2
F104R20 1/7,2/(2-4),2/(6-B),6/2
F104R10 1/4,2/(2-4),2/(6-8),6/2
(5 LEADS)
F304LE0 1/4,2/(2-4),2/(6-B),6/2
F304LD0 1/4,1/7,2/(2-4),2/(6-B),6/2
F204L30B 1/4,1/9,1/12,2/1,2/5,5/5,5/6,6/2
F204RA0B 1/4,1/3,1/10,1/12,2/1,2/5,4/1,4/3,6/2
F104RB0 1/4,2/2,2/6,6/2
(2 LEADS)
MDTMCH0,MDMCLST0 9/4
MDSTMCH0 9/1
MDRARFN0 2/2,2/6
MDPYMCH0 9/2
MDMRFCC0 7/1,7/19
MDMC3TR0 9/(1-4)
MDI0CC0 10 CONN CKT
MDIOMCH0 7/19,9/1,9/1
MD.ZPT0 7/20,8/4,9/4
MD.ZMS0 5/4,5/(7-14),7/19,9/4
MD.ZMIN0 5/11,7/19
MD.ZER0 5/1,5/2,:/4
MD.S3DB0 7/4,7/5

PART OF FS 1
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

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PART OF FS 1

MICROCONTROL

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
BROPH0	PARITY HIGH OF THE BR REGISTER (COPY 0)
BROPL0	PARITY LOW OF THE BR REGISTER (COPY 0)
BR0000	BIT 0 OF THE BR REGISTER (COPY 0)
BR1000	BIT 0 OF THE BR REGISTER (COPY 1)
CARH01	CARRY HIGH FROM DML (COPY 0)
CARH11	CARRY HIGH FROM DML (COPY 1)
CARL01	CARRY LOW FROM DML (COPY 0)
CARL11	CARRY LOW FROM DML (COPY 1)
CF00	CONDITION FLIP-FLOP (COPY 0)
CF10	CONDITION FLIP-FLOP (COPY 1)
COPNA1	COMPLEMENT PARITY OF NEXT ADDRESS FOR THE MAR
D.GBH0	ENABLE DATA HIGH TO THE GB
D.GBL0	ENABLE DATA LOW TO THE GB
DATA0	DATA MICRO-INSTRUCTION CONTROL
DML0GB0	DML TO THE GB (COPY 0)
DR00A	DATA READY FLIP-FLOP (COPY 0)
DR10A	DATA READY FLIP-FLOP (COPY 1)
DS00	DATA MANIPULATION LOGIC STATUS FLIP-FLOP (COPY 0)
DS10	DATA MANIPULATION LOGIC STATUS FLIP-FLOP (COPY 1)
EFET.CK0	ENABLE MAIN MEMORY FETCH
ELINTRP0	ENABLE LOAD INTERRUPTS
ELMINT0	ENABLE LOAD MICROINTERPRET INSTRUCTIONS
ELNOP00A	ENABLE LOAD NEW OPCODE (COPY 0)
ELNOP00B	ENABLE LOAD NEW OPCODE (COPY 0)
ELNOP10A	ENABLE LOAD NEW OPCODE (COPY 1)
ELNOP10B	ENABLE LOAD NEW OPCODE (COPY 1)
EMDCOLB0	ENABLE MISC. DECODER COLUMN 11
EMDCOLC0	ENABLE MISC. DECODER COLUMN 12
EMDROW10	ENABLE MISC. DECODER ROW 1
EMDROW70	ENABLE MISC. DECODER ROW 7
ENMCSGB0	ENABLE MICROCONTROL STATUS REGISTER TO THE GATING BUS
EN2040	ENABLE THE 2 OUT OF 4 AUXILIARY DECODER
ER.FNPT0	FUNCTION REGISTER PARITY ERROR
ER.IBPL0	IB PARITY LOW ERROR
ERAMAR00	ENABLE RAR TO THE MAR (COPY 0)
ERAMAR10	ENABLE RAR TO THE MAR (COPY 1)
ERAR.FN0	ENABLE RAR TO THE FUNCTION REGISTER
ERMARMT0	MAR-RAR MATCH ERROR
ERMARPT0	MAR PARITY ERROR
ERU1	ERROR RETURN ADDRESS REGISTER UPDATE BIT
FLZ.A000	ALL ONES FOUND IN A FIND LOW ZERO'S TEST (COPY 0)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
FLZ.A010	ALL ONES FOUND IN A FIND LOW ZERO'S TEST (COPY 1)
FN0ADLG0	ADD LONG BIT OF THE FUNCTION RESITER (COPY 0)
FN0ADP10	ADD + 1 BIT OF THE FUNCTION REGISTER (COPY 0)
FN0ADSH0	ADD SHORT BIT OF FUNCTION REGISTER (COPY 0)
FN0BOL(1,2,4,8)0	BOOLEAN BITS 1, 2, 4, 8 OF THE FUNCTION REGISTER (COPY 0)
FN0PT0	FUNCTION REGISTER PARITY BIT
FN1ADLG0	ADD LONG BIT OF FUNCTION REGISTER (COPY 1)
FN1ADSH0	ADD SHORT BIT OF FUNCTION REGISTER (COPY 1)
FREZ0	MAR FREEZE CONTROL LEAD
GBALZTA0	GATING BUS ALL ZEROS TEST PART A (COPY 0)
GBALZTB0	GATING BUS ALL ZEROS TEST PART B (COPY 0)
GBALZT10	GATING BUS ALL ZEROS TEST (COPY 1)
GBPH0	PARITY HIGH OF THE GATING BUS
GBPL0	PARITY LOW OF THE GATING BUS
GBG00-GB190	BITS 0-19 OF THE GATING BUS
IBPL.ER0	IB PARITY LOW ERROR (UNSTROBED)
IBPL0	PARITY LOW OF THE IB REGISTER
IB000-IB070	BITS 0-7 OF THE IB REGISTER
ICP208	CLOCK PHASE P20 [IC]
IFF01	I FLIP-FLOP (COPY 0)
IFF11	I FLIP-FLOP (COPY 1)
INTPRSB0	INTERRUPT PRESENT LEAD BUFFERED. (STROBED AND "ANDED" WITH BIN)
IODSIDL0	IDLE STATE CONDITION FROM IO CHANNELS TO THE DS BIT
IOTR1N0	IO TRANSMIT NORMAL STATE FROM IO CHANNELS TO THE TR1 BIT
IOTR2M0	IO TRANSMIT MAINTENANCE FROM IO CHANNELS TO THE TR2 BIT
MARP10	ADD 1 TO THE MAR REGISTER
MAR001(A-D) - MAR081(A-D)	OUTPUTS OF THE MAR REGISTER BITS 0-8 (INPUTS TO MICROSTORE)
MAR091-MAR111	OUTPUTS OF THE MAR REGISTER BITS 9-11 (REENCODED PLANE SELECT)
MD.BRPT0	MISC. DECODER CONTROL. GATE THE BR(8-15) TO THE PT REGISTER (BITS 8-15 OF TI)
MD.BRTI0	MISC. DECODER, GATE BR REGISTER TO THE TIMING REGISTER
MD.DET10	MISC. DECODER DETECTOR
MD.IMTC0	MISC. DECODER, IDLE MAINTENANCE CHANNEL
MD.SBAK0	MISC. DECODER, SET THE BA CHECK BIT
MD.SBTC0	MISC. DECODER, SET BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MD.SDIS0	MISC. DECODER, SET DISABLE FLIP-FLOP
MD.SDR00	MISC. DECODER, SET DATA READY FLIP-FLOP (COPY 0)
MD.SDR10	MISC. DECODER, SET DATA READY FLIP-FLOP (COPY 1)
MD.SSTP0	MISC. DECODER, SET STOP FLIP-FLOP (BIT 14 OF THE SS)
MD.STSW0	MISC. DECODER, STOP AND SWITCH CENTRAL CONTROL
MD.S1DB0	MISC. DECODER, GATE SWITCH REGISTER 1 TO THE DB
MD.S2DB0	MISC. DECODER, GATE SWITCH REGISTER 2 TO THE DB
MD.S3DB0	MISC. DECODER, GATE SWITCH REGISTER 3 TO THE DB
MD.TCH0	MISC. DECODER, TEST I/O CHANNEL
MD.ZDR00	MISC. DECODER, ZERO DATA READY FLIP-FLOP (COPY 0)
MD.ZDR10	MISC. DECODER, ZERO DATA READY FLIP-FLOP (COPY 1)
MD.ZER0	MISC. DECODER, ZERO THE ERROR REGISTER
MD.ZMIN0	MISC. DECODER, ZERO THE MICROINTERPRET BIT (BIT 11 OF THE SS)
MD.ZMS0	MISC. DECODER, ZERO THE MAINTENANCE STATE REGISTER
MD.ZPT0	MISC. DECODER, ZERO THE PROGRAM TIMER
MD.ZRU00	MISC. DECODER, ZERO THE RU FLIP-FLOP (COPY 0)
MD.ZRU10	MISC. DECODER, ZERO THE RU FLIP-FLOP (COPY 1)
MDA.BD0(A,B)	ENABLE GATING OF THE BAD DATA AND THE ADDRESS OF A DOUBLE STORE READ OPERATION TO THE DK AND AK REGISTERS RESPECTIVELY
MDDI1SD0	MISC. DECODER, GATE DI1 INTO THE SDR
MDDK1SD0	MISC. DECODER, GATE DK1 INTO THE SDR
MDDML1C0	MISC. DECODER, GATE THE DML COPY 1 TO THE CR REGISTER
MDERCRT0	MISCELLANEOUS DECODER RETURN FROM COMPLEMENT CORRECTION MICROSUBROUTINE
MDFLZT00	MISC. DECODER, ENABLE FIND LOW 0 TEST (COPY 0)
MDFLZT10	MISC. DECODER, ENABLE FIND LOW 0 TEST (COPY 1)
MDGDDI0(A,B)	ENABLE GATING OF THE GOOD DATA OF THE DOUBLE STORE READ OPERATION TO THE DI REGISTER
MDIDMCH0	MISC. DECODER, IDLE THE MCA
MDIDSW00	MISC. DECODER, IDLE THE SWITCH SEQUENCER
MDINCPR0	MISC. DECODER, INCREMENT THE PRESCALER
MDINCTC0	MISC. DECODER, INCREMENT THE TC
MDIOCC0	MISC. DECODER, INTERRUPT THE OTHER CENTRAL CONTROL
MDIODRB0	MISC. DECODER, GATE THE IOD TO R11

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MDMCBTR0	MISC. DECODER, GATE THE MCHB TO THE TR REGISTER
MDMCLST0	MISC. DECODER, LOAD THE START BIT INTO THE MCA
MDMRFCC0	MISC. DECODER, MAINTENANCE RESET FUNCTION (MRF) TO THE CENTRAL CONTROL
MDPYMCH0	MISC. DECODER, GATE BR PARITY BITS TO THE MCA
MDRARFN0	MISC. DECODER, GATE THE RAR TO THE FUNCTION REGISTER
MDSBSIR0	MISC. DECODER, GATE SIB TO SIR1
MDSTMCH0	MISC. DECODER, START THE MCA
MDTMARP0	TOGGLE MAR PARITY
MDTMCAG	MISC. DECODER, TEST THE MCA
MDX.RAR0	MISC. DECODER, GATE THE X FIELD OF THE IB TO THE LOW 4 BITS OF THE RAR
MDY.RAR0	MISCELLANEOUS DECODER, GATE THE Y FIELD OF THE IB TO THE LOW 4 BITS OF THE RAR
MDZDIDK0	MISC. DECODER, CLEAR THE DI1 AND DK1 REGISTERS
MD0IDCH0	MISC. DECODER, IDLE THE SELECTED I/O CHANNEL
MD1CHTN0	MISC. DECODER, LOAD THE SELECTED I/O CHANNEL WITH TRANSMIT NORMAL
MD2CHTM0	MISCELLAENOUS DECODER, LOAD THE SELECTED I/O CHANNEL WITH TRANSMIT MAINTENANCE
MC3CHC0	MISC. DECODER, LOAD THE SELECTED I/O CHANNEL WITH THE CONTROL FIELD DEFINED BY THE LOW 4 BITS OF GENERAL REGISTER 9

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 4A

BELL LABORATORIES

SD-1C900-01

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PART OF FS 1

MICROCONTROL

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MD4STCH0	MISC. DECODER, START THE SELECTED I/O CHANNEL
MD5EIOS0	MISC. DECODER, ENABLE THE IOS REGISTER TO BE GATED TO THE IOD IN THE SELECT I/O CHANNEL
MD6RAIO0	MISC. DECODER, ENABLE GATING FROM R10 TO THE IOD REGISTER IN THE SELECTED I/O CHANNEL
MD7SPA0	MISC. DECODER, SPARE CONTROL SIGNAL FOR I/O CHANNEL
MPS000-MPS310	BITS 0-31 OF THE MICRO-PROGRAM STORE OUTPUT
MRF.STP0	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF), 'OR' OF THE MRF SIGNAL AND THE STOP FLIP-FLOP
MRFSMAR0	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) SET MAR TO STARTING INITIALIZATION ADDRESS
MSPH0	PARITY HIGH OF MAINTENANCE STATE REGISTER
MS090	BIT 9 MAINTENANCE STATE REGISTER (ENABLE IB 3 OF 6 TRANSLATORS AND DISABLE FROM FIELD OF CHECK)
MS100	BIT 10 MAINTENANCE STATE REGISTER (ENABLE MAR-RAR MATCH)
MS110	BIT 11 MAINTENANCE STATE REGISTER (HOLD MAR PARITY)
MS120	BIT 12 MAINTENANCE STATE REGISTER (DISABLE TO FIELD)
MS130	BIT 13 OF MAINTENANCE STATE REGISTER
NA00	BIT 0 OF THE NEXT ADDRESS FIELD OF THE MIR
NA10	BIT 1 OF THE NEXT ADDRESS FIELD OF THE MIR
NA20400-NA20430	OUTPUTS OF THE 2 OUT OF 4 AUXILIARY DECODER ATTACHED TO BITS 8 TO 11 AT THE MIR NEXT ACDRESS FIELD
NA20-NA70	BITS 2-7 OF THE NEXT ADDRESS FIELD OF THE MIR
OPF00	OPCODE FIL BIT (COPY 0)
OPF10	OPCODE FIL BIT (COPY 1)
PL.SL00-PL.SL70	BIT 0-7 OF THE PLANE SELECT LEADS FOR THE MICROSTORE (EACH PLANE SELECT ENABLES A 512- BY 32-WORD BLOCK)
P00	CLOCK PHASE P0 (GROUND ACTIVE)
P01	CLOCK PHASE P1 (POSITIVE ACTIVE)
P10	CLOCK PHASE P1 (GROUND ACTIVE)
P11	CLOCK PHASE P1 (POSITIVE ACTIVE)
P21	CLOCK PHASE P2 (POSITIVE ACTIVE)
P31	CLOCK PHASE P3 (POSITIVE ACTIVE)
RARPH0	PARITY HIGH OF THE RETURN ADDRESS REGISTER
RAR001-RAR111	BITS 0-11 OF THE RAR REGISTER
RU00	RETURN ADDRESS RESISTOR UPDATE FLIP-FLOP (COPY 0)
RU10	RETURN ADDRESS RESISTOR UPDATE FLIP-FLOP (COPY 1)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SERC.CC0	STORE ERROR C RECALLING IN THE INVOCATION OF THE COMPLEMENT CORRECTION MICROSUBROUTINE
SIRPH0	PARITY HIGH OF SIR'S (SIR0 IF IFF=0, SIR1 IF IFF=1)
SIR080-SIR150	BITS 08-15 OF THE SIRS (SIR0 IF IFF=0, SIR1 IF IFF=1)
SSMINT0A	MICROINTERPRET BIT (BIT 11 OF THE SS)
SSSTP0B	STOP FLIP-FLOP BIT (BIT 14 OF THE SS)
TEST.DR0	CONTROL SIGNAL THAT INDICATES OR IS BEING TESTED
TR100	TR1 FLIP-FLOP COPY 0
TR110	TR1 FLIP-FLOP COPY 1
TR200	TR2 FLIP-FLOP COPY 0
TR210	TR2 FLIP-FLOP COPY 1
TSIFF0	TEST SET ACCESS POINT, I FLIP-FLOP OUTPUT
TSLNOP0	TEST SET ACCESS POINT, LOAD A NEW OPCODE
UTLFRZ0	UTILITY FREEZE LEAD (INHIBIT LOADS OF NEW OPCODES)
XPT0	PARITY OF X FIELD OF THE IB REGISTER
XT3.6800-XT3.6850	OUTPUT OF 3 OUT OF 6 TRANSLATOR ATTACHED TO X FIELD OF IB REGISTER
YPT0	PARITY OF Y FIELD OF IB REGISTER
YT3.6800-YT3.6850	OUTPUT OF 3 OUT OF 6 CODE TRANSLATOR ATTACHED TO Y FIELD OF IB REGISTER

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 3A

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PART OF FS 1

MICROCONTROL

SYMBOL NO. 1

MICROCONTROL B3

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B3	02-33	FA1018	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		003			SIROPB70	4A5
		201			TLINTRP0	3H5
		301			INVB1	3G9
OR10A	I	202	4/3		OR10	3A4
ELNOP10A	0I	100	1/5 1/4		TLNOP00	3H7
ELNOP10B	0	307	1/6,4/3 6/4,7/7		LNOP.IB0	3H6
ERAMAR00	0I	203	1/2,1/3		TALL00	3H2
F104L10B	I	311	1/13		F104L10	4A2
F304R70B	I	312	1/13		F304R70	4A2
GBAL2TB0	0	008	1/5		GBHE20	2G7
GB080	0I	207	2/3		RARGB080	9H3
GB090	0I	007	2/3		RARGB090	9H2
GB100	0I	306	2/3		RARGB100	8H4
GB110	0I	208	2/3		RARGB110	8H3
GB120	0I	108	2/3		RARGB120	7H3
GB130	0I	309	2/3		RARGB130	7H3
GB140	0I	210	2/3		RARGB140	6H2
GB150	0I	010	2/3		RARGB150	6H2
GB160	0I	308	2/2		RARGB160	5H2
GB170	0I	009	2/2		RARGB170	5H2
GB180	0I	209	2/2		RARGB180	4H5
GB190	0I	109	2/2		RARGB190	4H4
IB010	I	205	4/14	202	IB.Y.B10	9A0
IB020	I	305	4/13	202	IB.Y.B20	8A4
IB030	I	206	4/12	202	IB.Y.B30	8A0
IB050	I	105	4/10	202	IB.X.B10	9A0
IB060	I	006	4/9	202	IB.X.B20	8A5
IB070	I	106	4/8	202	IB.X.B30	8A1
IFF01	I	001	1/5		IFF11	3A7
INTPRSB0	I	103	5/3		INTRP10	3A3
MARP10	I	101	1/5		INVB0	3A9
MO.ZRU00	I	012	1/5		CLR.RU00	3A0
MDSBSIR0	OT	300	1/4		SIB.SIR0	3H3
MOX.RAR0	I	005	1/4		X.RAR0	8A1
MOY.RAR0	I	304	1/4		Y.RAR0	8A0
MPS070	I	113	12/8		MPSNA000	2A8
MPS090	I	313	12/8		MPSNA010	2A7
MPS110	I	014	12/8		MPSNA020	2A7
MPS130	I	214	12/8		MPSNA030	2A6
MPS150	I	315	12/8		MPSNA040	2A5
MPS170	I	016	12/7		MPSNA050	2A4
MPS190	I	216	12/7		MPSNA060	2A4
MPS210	I	116	12/7		MPSNA070	2A3
MPS230	I	316	12/7		MPSNA080	2A2
MPS250	I	017	12/7		MPSNA090	2A1
MPS270	I	217	12/7		MPSNA100	2A1
MPS290	I	117	12/7		MPSNA110	2A0
OPF10	I	102	1/4		OPF10	4A0
P00	I	212	8/3		P00	4A3
P21	I	213	8/3		P21	3A0
P31	I	013	8/3		P31	3A3
RAR001	0	219	1/3		RARB001	9H3
RAR011	0	118	1/3,1/8		RARB011	9H1
RAR021	0	318	1/3,1/8		RARB021	8H4
RAR031	0	019	1/3,1/8		RARB031	8H2
RAR041	0	215	1/3,1/8		RARB041	7H4
RAR051	0	015	1/2,1/8		RARB051	7H1

SYMBOL NO. 1 (CONT)

MICROCONTROL B3

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B3	02-33	FA1018	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
RAR061	0	314	1/2,1/8		RARB061	6H3
RAR071	0	114	1/2,1/8		RARB071	6H0
RAR081	0	018	1/2,1/8		RARB081	5H3
RAR091	0	218	1/2,1/8		RARB091	5H0
RAR101	0	317	1/2,1/8		RARB101	4H5
RAR111	0	115	1/2,1/8		RARB111	4H1
RU00	0	107	1/5	202	RU00	3H0
SIR080	I	104	4/15	202	SIROPB00	9A3
SIR090	I	204	4/14	202	SIROPB10	9A1
SIR100	I	004	4/13	202	SIROPB20	8A5
SIR110	I	303	4/12	202	SIROPB30	8A2
SIR120	I	011	4/11	202	SIROPB40	7A4
SIR130	I	310	4/10	202	SIROPB50	7A0
SIR140	I	110	4/9	202	SIROPB60	6A3
SSMINT0A	I	302	5/11		MINTI0	3A5
TEST.DR0	OT	112	1/5		MAL20	3G8
T104L10B	I	211	1/11		T104L10	4A1
T304R70B	I	111	1/11		T304R70	4A1
UTLFR20	I	002	5/8		UTLFRZ10	3A4
3T054E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054E	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 2

MICROCONTROL B2

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B2	02-34	FA1017	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		307			SIROPB70	5A5
0.GBH0	I	214	1/4		0.GBHI0	4A0
0.GBL0	I	007	1/4		0.GBLI0	4A4
ELINTRP0	I	105	1/8		LINTRP0	6A4
ELNOP00A	I	306	1/5		LNOP0	5A2
EMDCOLC0	I	212	1/5		COL120	3A1
EMDROW70	I	114	1/5		ROW70	3A0
ERAMAR00	I	014	1/1		RAR.MAR0	5A3
ERAR.FN0	I	313	2/6		RAR.FNI0	4A4
ERU1	I	314	4/2		ERUI1	3A2
FRE20	I	305	7/19		FREZI0	5A1
GBPH0	OT	111	2/2		0.GBL0	7H6
GBPL0	OT	311	2/2		0.GBH0	7H6
GB050	OT	210	2/4		0.GB050	4G7
GB060	OT	115	2/4		0.GB060	4H5
GB070	OT	116	2/4		0.GB070	4H4
GB130	OT	010	2/3		0.GB130	4G7
GB140	OT	315	2/3		0.GB140	4H5

SYMBOL NO. 2 (CONT)

MICROCONTROL B2

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B2	02-34	FA1017	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
GB150	OT	216	2/3		0.GB150	4H3
GB160	OT	316	2/2		0.GB160	4H3
GB170	OT	017	2/2		0.GB170	4H3
GB180	OT	217	2/2		0.GB180	4H2
GB190	OT	117	2/2		0.GB190	4H1
MAR051A	0	100	1/8,12/5 12/6,12/7 12/8		MARB51A	6H6
MAR051B	0	202	12/1,12/2 12/3,12/4		MARB51B	6H6
MAR051C	0	002	12/13,12/14 12/15,12/16		MARB51C	6H6
MAR051D	0	301	12/9,12/10 12/11,12/12		MARB51D	6H5
MAR061A	0	101	1/8,12/5 12/6,12/7 12/8		MARB61A	6H4
MAR061B	0	201	12/1,12/2 12/3,12/4		MARB61B	6H4
MAR061C	0	001	12/13,12/14 12/15,12/16		MARB61C	6H3
MAR061D	0	300	12/9,12/10 12/11,12/12		MARB61D	6H3
MAR071A	0	102	1/8,12/5 12/6,12/7 12/8		MARB71A	6H2
MAR071B	0	204	12/1,12/2 12/3,12/4		MARB71B	6H2
MAR071C	0	004	12/13,12/14 12/15,12/16		MARB71C	6H1
MAR071D	0	303	12/9,12/10 12/11,12/12		MARB71D	6H1
MAR081A	0	103	1/8,12/5 12/6,12/7 12/8		MARB81A	5G9
MAR081B	0	203	12/1,12/2 12/3,12/4		MARB81B	5G9
MAR081C	0	003	12/13,12/14 12/15,12/16		MARB81C	5G9
MAR081D	0	302	12/9,12/10 12/11,12/12		MARB81D	5G8
MAR091	0	104	1/8		MARB091	7H5
MAR101	0	006	1/8		MARB101	7H5
MAR111	0	206	1/8		MARB111	7H4
MPS050	I	005	12/8		MPSXXCA0	7A6
MPS170	I	317	12/7		MPSNA050	2A7
MPS190	I	018	12/7		MPSNA060	2A6
MPS210	I	218	12/7		MPSNA070	2A5
MPS230	I	118	12/7		MPSNA080	2A4
MPS250	I	318	12/7		MPSNA090	2A3
MPS270	I	019	12/7		MPSNA100	2A2
MPS290	I	219	12/7		MPSNA110	2A1
MRFSMAR0	I	205	7/19		MRF0	6A1
NA50	0	312	2/2,2/6	202	TNA.B050	4H6
NA60	0	016	2/2,2/6	202	TNA.B060	4H6
NA70	0	112	2/2,2/6	202	TNA.B070	4H5
OPF00	I	012	1/5		OPF10	5A1
PL.SL00	0	209	12/5,12/6 12/7,12/8		PL.SL0.0	7H2
PL.SL10	0I	309	12/5,12/6		PL.SL1.0	7H2
PL.SL20	0I	109	12/1,12/2 12/3,12/4		PL.SL2.0	7H2
PL.SL30	0I	009	12/1,12/2		PL.SL3.0	7H1
PL.SL40	0I	208	12/13,12/14 12/15,12/16		PL.SL4.0	7H1

SYMBOL NO. 2 (CONT)

MICROCONTROL B2

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B2	02-34	FA1017	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
PL.SL50	0I	108	12/13,12/14		PL.SL5.0	7H1
PL.SL60	0I	308	12/9,12/10 12/11,12/12		PL.SL6.0	7H0
PL.SL70	0I	008	12/9,12/10		PL.SL7.0	7H0
P01	I	015	8/3		P01	2A1
P10	I	113	8/3		P10	5A0
RAR051	I	110	1/1		RARB0511	4A6
RAR061	I	310	1/1		RARB0611	4A6
RAR071	I	011	1/1		RARB0711	4A4
RAR081	I	211	1/1		RARB0811	5A7
RAR091	I	013	1/1		RARB0911	5A6
RAR101	I	213	1/1		RARB1011	5A4
RAR111	I	215	1/1		RARB1111	5A3
SERC.CC0	I	106	4/2		ERC.CCI0	7A8
SIR130	I	207	4/10	202	SIROPB50	6A6
SIR140	I	107	4/9	202	SIROPB60	6A4
SSSTP0B	I	304	5/8		STOP0	6A0
3T054E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054E	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 1

SYMBOL(S) 1 2

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

BELL LABORATORIES

SD-1C900-01

B1CA

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12/01/77

PART OF FS 1

MICROCONTROL

SYMBOL NO. 3

MICROCONTROL B1

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B1	02-35	FA1016	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
0.GBH0	I	218	1/4		0.GBHI0	4A0
0.GBL0	I	118	1/4		0.GBLI0	4A0
ELINTRP0	I	219	1/8		LINTRP0	5A2
ELNOP00A	I	207	1/5		LNOP0	5A2
EMDCOLB0	I	209	1/5		COL110	6A0
EMDCOLC0	I	009	1/5		COL120	6A0
EMDROW10	I	109	1/5		ROW10	6A1
EMDROW70	I	110	1/5		ROW70	3A0
ERAMAR00	I	007	1/1		RAR.MAR0	5A1
ERAR.FN0	I	107	2/6		RAR.FNI0	4A3
ERU1	I	202	4/2		ERUI1	3A2
FREZ0	I	301	7/19		FREZI0	5A3
GB000	OT	013	2/4		0.GB000	4G7
GB010	OT	113	2/4		0.GB010	4H7
GB020	OT	315	2/4		0.GB020	4H4
GB030	OT	211	2/4		0.GB030	4H4
GB040	OT	001	2/4		0.GB040	4H1
GB080	OT	213	2/3		0.GB080	4G7
GB090	OT	313	2/3		0.GB090	4H6
GB100	OT	016	2/3		0.GB100	4H5
GB110	OT	011	2/3		0.GB110	4H0
GB120	OT	100	2/3		0.GB120	4H1
IB000	I	311	4/15	202	IB.Y.B00	6A6
IB010	I	112	4/14	202	IB.Y.B10	6A4
IB020	I	312	4/13	202	IB.Y.B20	5A8
IB030	I	210	4/12	202	IB.Y.B30	5A5
IB040	I	012	4/11	202	IB.X.B00	6A7
IB050	I	212	4/10	202	IB.X.B10	6A4
IB060	I	309	4/9	202	IB.X.B20	5A8
IB070	I	010	4/8	202	IB.X.B30	5A5
MARP10	I	101	1/5		MARP1.0	6A7
MAR001A	0	003	12/5,12/6 12/7,12/8		MARB01A	6H6
MAR001B	0	203	12/1,12/2 12/3,12/4		MARB01B	6H6
MAR001C	0	103	12/13,12/14 12/15,12/16		MARB01C	6H7
MAR001D	0	303	12/9,12/10 12/11,12/12		MARB01D	6H7
MAR011A	0	004	1/8,12/5 12/6,12/7 12/8		MARB11A	6H3
MAR011B	0	204	12/1,12/2 12/3,12/4		MARB11B	6H4
MAR011C	0	304	12/13,12/14 12/15,12/16		MARB11C	6H4
MAR011D	0	104	12/9,12/10 12/11,12/12		MARB11D	6H4
MAR021A	0	106	1/8,12/5 12/6,12/7 12/8		MARB21A	5H7
MAR021B	0	306	12/1,12/2 12/3,12/4		MARB21B	5H8
MAR021C	0	206	12/13,12/14 12/15,12/16		MARB21C	5H8
MAR021D	0	006	12/9,12/10 12/11,12/12		MARB21D	5H8
MAR031A	0	005	1/8,12/5 12/6,12/7 12/8		MARB31A	5H4
MAR031B	0	205	12/1,12/2 12/3,12/4		MARB31B	5H4

SYMBOL NO. 3 (CONT)

MICROCONTROL B1

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B1	02-35	FA1016	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
MAR031C	0	105	12/13,12/14 12/15,12/16		MARB31C	5H5
MAR031D	0	305	12/9,12/10 12/11,12/12		MARB31D	5H5
MAR041A	0	114	1/8,12/5 12/6,12/7 12/8		MARB41A	5H2
MAR041B	0	214	12/1,12/2 12/3,12/4		MARB41B	5H2
MAR041C	0	014	12/13,12/14 12/15,12/16		MARB41C	5H2
MAR041D	0	115	12/9,12/10 12/11,12/12		MARB41D	5H3
MPS050	I	201	12/8		MPSXXCA0	7A4
MPS070	I	217	12/8		MPSNA000	2A6
MPS090	I	117	12/8		MPSNA010	2A5
MPS110	I	317	12/8		MPSNA020	2A4
MPS130	I	018	12/8		MPSNA030	2A3
MPS150	I	302	12/8		MPSNA040	2A1
MRF.STP0	I	308	1/6		STP.MRF0	5A3
NA00		314			TNA.B000	4G8
NA10	0	015	2/2,2/6		TNA.B010	4H6
NA20	0	215	2/2,2/6	202	TNA.B020	4H5
NA30	0	310	2/2,2/6	202	TNA.B030	4H3
NA40	0	300	2/2,2/6	202	TNA.B040	4H2
P01	I	318	8/3		P01	2A1
P10	I	019	8/3		P10	4A1
RAR001	I	017	1/1		RARB00I1	4A8
RAR011	I	316	1/1		RARB01I1	4A5
RAR021	I	116	1/1		RARB02I1	4A5
RAR031	I	216	1/1		RARB03I1	4A2
RAR041	I	102	1/1		RARB04I1	4A2
SERC.CC0	I	111	4/2		ERC.CCI0	7A1
SIR080	I	307	4/15	202	SIROPB00	6A6
SIR090	I	008	4/14	202	SIROPB10	6A3
SIR100	I	208	4/13	202	SIROPB20	5A7
SIR110	I	108	4/12	202	SIROPB30	5A3
SIR120	I	002	4/11	202	SIROPB40	5A2
3T054E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054E	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 4

MICROCONTROL B4

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B4	06-32	FA1019	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
BR0PH0	I	113	2/2	202	BR.PH0	5A2
BR0PL0	I	213	2/2	202	BR.PL0	5A0
BR1000	I	301	2/8	202	B0.TSTI0	4A8
CARH11	I	109	2/6		CARHI1	4A2
CARL11	I	209	2/7	202	CARLI1	4A4
CF10		300			CF10	5H8
COPNA1	0	018	1/6		COPNA1	3H3
0.GBH0	0	019	1/2,1/3 1/6		OAT.GBH0	2H6
0.GBL0	0	219	1/2,1/3 1/6		OAT.GBL0	2H6
OMLOGB0	I	207	2/4	202	OML.GBI0	4A1
OR10A	I	007	4/3		OR10	5A6
OS10		101			OS10	6H6
ELNOP10A	I	009	1/1		LNOP0	3A7
ENMCSGB0	0	004	1/5,1/6		MCS.GB0B	3G8
FL2.AD10	I	003	2/6		FL2OI0	4A5
FN1ADLG0	I	202	2/6		ADDLI0	4A2
FN1ADSH0	I	002	2/6		ADDSI0	4A4
F104RI0	I	110	1/13		F104R10	2A6
F104R40	I	210	1/13		F104R40	2A6
F104R80	I	112	1/13		F104R80	2A5
F204LC0B	I	116	1/13		F204LC0	2A4
F204L30B	I	212	1/13		F204L30	2A7
F204RA0B	I	111	1/13		F204RA0	2A8
F204RC0C	I	211	1/13		F204RC0	2A8
F204R30C	I	015	1/13		F204R30	2A4
F204R50C	I	215	1/13		F204R50	2A4
F204R60C	I	012	1/13		F204R60	2A7
F204R90B	I	311	1/13		F204R90	2A5
F304L00	I	011	1/13		F304L00	2A6
F304LE0	I	310	1/13		F304LE0	2A5
F304L70	I	309	1/13		F304L70	3A8
GBAL2T10	I	005	6/3		BALL2T0	6A3
GB010	OT	303	2/4		CF1.GB0	5H6
GB030	OT	308	2/4		DS1.GB0	6H7
GB050	OT	103	2/4		TR11.GB0	5H1
GB070	OT	203	2/4		TR21.GB0	5H2
GB090	OT	204	2/3		DR1.GB0	5H6
GB110	OT	107	2/3		RU1.GB0	3G8
GB130	OT	307	2/3		IFF1.GB0	3H6
GB150	OT	108	2/3		OPF1.GB0	3H5
IFF11	0	008	1/8,4/3 4/5,11/1 11/2,11/3		IFF11	3H6
INTPRSB0	I	306	5/3		INTRPI0	4A7
IODSIOL0	I	206	10/1	202	I.OIOI0	4A7
IOTR1N0	I	312	10/2		IOMSGNI0	5A4
IOTR2M0	I	013	10/2	202	IOMSGMI0	5A3
MD.DET10	0	218	6/3		MDDET0	6H0
MD.SOR10	0	102	4/3		ST.DR0	5H5
MD.TCH0	0	100	6/5		TEST.I00	5H4
MD.ZDR10	0	302	4/3		CL.DR0	5H5
MD.ZRU10	0	317	1/6,1/8		CLR.RU0	2H3
MDFLZT10	0	118	2/8		MD.FLZ0	2H3
MDSBSIR0	OT I	217	1/1 11/1,11/2 11/3		SIB.SIR0	2H4
MDTMARP0	0	017	1/6		TOMARP0	2H4
MDX.RAR0	0	117	1/1		EX.MAR0	2H2

SYMBOL NO. 4 (CONT)

MICROCONTROL B4

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B4	06-32	FA1019	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
MDY.RAR0	0	318	1/1		EY.MAR0	2H1
MS110	I	305	5/11		CMSI0	6A0
OPF10	0	208	1/1,4/3		OPF10	3H5
P01	I	205	8/3		P01	3A1
P11	I	010	8/3		P11	3A0
P21	I	104	8/3		P21	6A1
RU10	I	106	1/8		RU10	3A8
TR110		201			TR110	5H1
TR210		001			TR210	5H2
T104L10B	I	214	1/11		T104L10	2A2
T204LC0B	I	304	1/11		T204LC0	2A1
T204L30B	I	316	1/11		T204L30	2A0
T204RA0B	I	315	1/11		T204RA0	2A1
T204RC0C	I	115	1/11		T204RC0	2A0
T204R30C	I	014	1/11		T204R30	2A3
T204R50C	I	313	1/11		T204R50	2A3
T204R90B	I	016	1/11		T204R90	2A2
T304RB0B	I	216	1/11		T304RB0	2A2
XPT0	I	006	1/7	202	XPTI0	3A2
YPT0	I	105	1/7	202	YPTI0	3A3
3T058F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V058F	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 1
SYMBOL(S) 3 4

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B1CB

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12/01/77

PART OF FS 1

MICROCONTROL

SYMBOL NO. 5

MICROCONTROL B6

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B6	06-35	FA1021	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
BROPH0	I	218	2/2	202	BRPH0	8A3
BROPL0	I	118	2/2	202	BRPL0	8A2
BR0000	I	110	2/4	202	B0.TSTI0	6A7
CARH01	I	019	2/2		CARHI1	6A1
CARL01	I	317	2/3		CARLI1	6A2
CF00	O	215			CF00	10H2
OR00A	I	105	4/1		OR00	10A0
OS00	O	312		202	OS00	7H3
ELNOP00A	OT	208	1/8		TEXSIR00	3H4
	I		1/2,1/3			
	I	006	1/5		LNOP0	8A8
ELNOP10A	O	209	1/1		TEXSIR10	2H6
EMOCOLB0	OI	309	1/3		TC11.0	4H2
EMDCOLC0	OI	109	1/6		TC12.0	4H2
			1/2,1/3			
EMDROW10	OI	106	1/3		TR10	4G7
EMOROW70	OT	301	1/6		TR70	4H4
	I		1/2,1/3			
ENMCSGB0	I	305	1/4		MCS.GB0	8A0
FL2.A000	I	211	2/2		FL2OI0	6A4
FNOADLGG	I	011	2/2		ADDLI0	6A1
FNOADSH0	I	310	2/2		ADDSI0	6A2
GBAL2TA0	I	013	2/6		BALL2TA0	7A5
GBAL2TB0	I	213	1/1		BALL2TB0	7A5
GB000	OT	316	2/4		CF0.GB0	10H2
GB020	OT	112	2/4		OS0.GB0	7H2
GB040	OT	116	2/4		TR10.GB0	8H2
GB060	OT	216	2/4		TR20.GB0	8H3
	I	306	2/4		GB.06I0	7A6
GB070	I	002	2/4		GB.07I0	7A6
GB080	OT	117	2/3		OR0.GB0	10H1
GB100	OT	016	2/3		RU0.GB0	8H1
GB120	OT	315	2/3		IFF0.GB0	7H1
GB140	OT	115	2/3		OPF0.GB0	7H1
IFF01	O	014	1/1,4/1		IFF01	8G8
			4/8,4/9			
			4/10,4/11			
			4/12,4/13			
			4/14,4/15			
INTPRSB0	I	210	5/3		INTRPI0	6A6
IODSIOL0	I	010	10/1	202	I.OIOI0	6A5
IOTR1N0	I	201	10/2		IOMSGI0	8A5
IOTR2M0	I	018	10/2	202	IOMMSGI0	8A4
MARP10	OT	311	1/8		TMAR0	9H6
	I		1/1,1/3			
MD.SOR00	O	108	4/1		SET.OR0	10H3
MD.2OR00	O	009	4/1		CLR.OR0	10H4
MD.2RU00	O	308	1/1		CLR.RU0	4H0
MDERCRT0	OT	217	7/19		ERCC.RT0	4H1
	I		1/6,4/2			
MDFL2T00	O	113	2/4		MD.FL200	6H4
MPS000	I	203	12/8		MPSFR000	3A8
MPS020	I	204	12/8		MPST0000	2A8
MPS040	I	103	12/8		MPSFR010	3A7
MPS060	I	104	12/8		MPST0010	2A7
MPS080	I	101	12/8		MPSFR020	3A6
MPS100	I	007	12/8		MPST0020	2A6
MPS120	I	300	12/8		MPSFR030	3A5
MPS140	I	303	12/8		MPST0030	2A5
MPS160	I	100	12/7		MPSFR040	3A4

SYMBOL NO. 5 (CONT)

MICROCONTROL B6

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B6	06-35	FA1021	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MPS180	I	207	12/7		MPST0040	2A4
MPS200	I	001	12/7		MPSFR050	3A2
MPS220	I	008	12/7		MPST0050	2A3
MPS240	I	003	12/7		MPSFR060	3A1
MPS260	I	111	12/7		MPST0060	2A1
MPS280	I	202	12/7		MPSFR070	3A0
MPS300	I	004	12/7		MPST0070	2A0
OPF00	O	313	1/2,4/1		OPF00	8G7
P01	I	206	8/3		P01	7A7
P31	I	304	8/3		P31	5A0
RU00	I	318	1/1	202	RU00	8A1
TEST.OR0	OT	017	1/1		TTST.OR0	9H8
	I		4/2			
TR100	O	015		202	TR100	8H2
TR200	O	214		202	TR200	8H4
TSIFF0	O	314			TSIFF0	8G8
3T058F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0635B	GRD	005			GRD005	2H2
	GRD	102			GRD102	2H2
	GRD	107			GRD107	2H1
	GRD	200			GRD	
	GRD	205			GRD205	2H1
	GRD	302			GRD302	2H2
	GRD	307			GRD307	2H1
3VG0635T	GRD	012			GRD012	2H1
	GRD	114			GRD114	2H1
	GRD	212			GRD212	2H1
	GRD	319			GRD	
3V058F	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 6

MICROCONTROL B8

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B8	02-31	FA1023	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		002			MS0C	3G8
		005			MPTA1	3H5
		105			MARP0C	3H5
COPNA1	I	117	1/4		ECOPNAI1	2AG
D.GBH0	I	215	1/4		DAT.GBH0	2A2
D.GBL0	I	216	1/4		DAT.GBL0	2A1
DATA0	I	116	1/8		DATA0	3A5
EFET.CK0	I	316	1/8		FETCH0	3A4
ELNOP10B	I	211	1/1		LNOP00	2A5
EMDCOLC0	O	301	1/5		MS0B	3G9
EMOROW70	OT	101	1/5		MS0A	3G9
ENMCSGB0	I	214	1/4		MCS.GBI0	3A6

SYMBOL NO. 6 (CONT)

MICROCONTROL B8

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B8	02-31	FA1023	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
EN2040	I	113	1/8		EN204I0	2A3
ERAMAR10	I	011	1/8		ALL000	2A7
ERMARPT0	O	003	5/2		MARP.CK0	3H1
ERU1	I	201	4/2		ERUI1	4A8
GBPH0	OT	019	2/2		DAL.PH0	4G8
	OT	314	2/2		MCS.GB0B	3G7
GBPL0	OT	015	2/2		MCS.GB0A	3G7
	OT	118	2/2		DAL.PL0	4G7
GB160	OT	114	2/2		MARP0A	3G6
GB170	OT	014	2/2		MARP0B	3G6
GB180	OT	102	2/2		ERU0A	3G8
GB190	OT	202	2/2		ERU0B	3G7
IBPL.ER0	O	219	1/8	202	IBPL.ER0	4H1
IBPL0	I	115	4/5	202	IB.PLI0	4A2
MD.2RU10	I	312	1/4		CL.RU0	2A1
MDERCRT0	I	300	1/5		ERCC.RT0	2A8
MDTMARP0	I	217	1/4		TOMARP0	3A1
MPS010	I	315	12/8		MPSXPTA0	4A4
MPS310	I	016	12/7		MPSXPNA0	4A4
MRF.STP0	O	205	1/3,4/9		MRF.STP0	3H2
MRFSMAR0	I	304	7/19		MRFI0	3A2
MSPH0	I	107	5/4	202	MSB0	3A2
MS110	I	313	5/11		CMSI0	3A3
MS130	I	001	5/9		MSI0	3A8
P01	I	110	8/3		P01	4A2
P11	I	017	8/3		P11	4A6
P21	I	317	8/3		P21	3A1
RARPH0	I	310	1/8		RARPI0	2A8
SERC.CC0	I	100	4/2		SERCCCI0	2A3
SIRPH0	I	111	4/5	202	IB.PH0	2A7
SIR150	I	311	4/8	202	IB.BA0	2A6
SSSTP0B	I	307	5/8		STOPI0	3A2
TSLNOP0	O	302			TSLNOP0	2H5
XPT0	I	213	1/7	202	X.PT0	4A1
YPT0	I	013	1/7	202	Y.PT0	4A0
3T054E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054E	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 1
SYMBOL(S) 5 6

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	DWG SIZE C2	ISSUE 7D
			B1CC

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PART OF FS 1

MICROCONTROL

SYMBOL NO. 7

MICROCONTROL B5

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B5	06-19	FA1020	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		116			F304L00	7H0
		211			IA10	3A8
FN0ADLG0	I	115	2/2		FNB30	2A2
FN0ADP10	I	016	2/2		FNB10	2A3
FN0ADSH0	I	315	2/2		FNB20	2A2
FN0B0L10	I	314	2/2		FNB40	2A1
FN0BDL20	I	219	2/2		FNB50	2A1
FN0B0L40	I	019	2/2		FNB60	2A0
FN0B0L80	I	318	2/2		FNB70	2A0
FNOPT0	O	316	1/8		FNPT0	2H1
F104L40	I	307	1/13		IA50	3A9
F104R20	I	004	1/13		F104R20	7A2
F1D4R40	I	303	1/13		F1D4R40	7A1
F304LD0	I	003	1/13		F304LDI0	7A0
F304L70	I	108	1/13		IA40	3A9
GBPH0	DT	018	2/2		TBPHN0	7H1
GBPL0	DT	216	2/2		TBPLN0	7H2
GB000	DT	104	2/4		TB00N0B	8G5
GB010	DT	105	2/4		TB01N0B	8G4
GB020	DT	106	2/4		TB02N0B	8G3
GB030	DT	207	2/4		TB03N0B	8G2
GB040	DT	312	2/4		TB04N0B	8G1
GB050	DT	313	2/4		TB05N0B	8G0
GB060	DT	214	2/4		TB06N0B	7G9
GB070	DT	215	2/4		TB07N0B	7G8
GB080	DT	204	2/3		TB08N0B	7G7
GB090	DT	304	2/3		TB09N0B	7G7
GB100	DT	206	2/3		TB10N0B	7H6
GB110	DT	306	2/3		TB11N0B	7H5
GB120	DT	311	2/3		TB12N0B	7H5
GB130	DT	013	2/3		TB13N0B	7H4
GB140	DT	014	2/3		TB14N0B	7H3
GB150	DT	015	2/3		TB15N0B	7H3
IB0D0	I	009	4/15	202	IB.Y00	2A7
IB010	I	209	4/14	202	IB.Y10	2A7
IB020	I	109	4/13	202	IB.Y20	2A6
IB030	I	309	4/12	202	IB.Y30	2A6
IB040	I	010	4/11	202	IB.X00	2A5
IB050	I	210	4/10	202	IB.X10	2A5
IB060	I	110	4/9	202	IB.X20	2A4
IB070	I	310	4/8	202	IB.X30	2A4
MS090	I	103	5/13		MAC0	5B1
SSSTP0B	I	203	5/8		STDP0	5B1
T2D4L50A	I	011	1/11		IA2D	3A8
T2D4L60A	I	111	1/11		IA00	3A7
T3D4LB0A	I	308	1/11		IA30	3A8
XPT0	D	208	1/4,1/6	202	XPT0	2H5
XT3.6B00	D	301	1/11,1/13	202	XT3.6B00	5G7
XT3.6B10	O	002	1/11,1/13	202	XT3.6B10	5G7
XT3.6B2D	D	202	1/11,1/13	202	XT3.6B20	5G6
XT3.6B30	O	100	1/11,1/13	202	XT3.6B30	5G6
XT3.6B40	D	117	1/11,1/13	202	XT3.6B40	5H2
XT3.6B50	O	218	1/11,1/13	202	XT3.6B50	5H3
YPT0	O	008	1/4,1/6	202	YPT0	2H7
YT3.6B00	O	300	1/11,1/13	202	YT3.6B00	6G7
YT3.6B10	O	001	1/11,1/13	202	YT3.6B10	6G7
YT3.6B20	D	201	1/11,1/13	202	YT3.6B20	6G6
YT3.6B30	O	101	1/11,1/13	202	YT3.6B30	6G6
YT3.6B40	O	317	1/11,1/13	202	YT3.6B40	6H2
YT3.6B50	D	118	1/11,1/13	202	YT3.6B50	6H3

SYMBOL NO. 7 (CONT)

MICROCONTROL B5

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B5	06-19	FA1020	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062B	GRD	0GD		203	GRD	
3T062B	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0619B	GRD	005			GRD005	2H4
	GRD	102			GRD102	2H3
	GRD	107			GRD107	2H3
	GRD	200			GRD	
	GRD	205			GRD205	2H3
	GRD	302			GRD302	2H2
3VG0619T	I	217			FNB00	2A3
	GRD	012			GRD012	2H4
	GRD	017			GRD017	2H4
	GRD	112			GRD112	2H3
	GRD	114			GRD114	2H3
	GRD	212			GRD212	2H3
	GRD	319			GRD	
3V062A	PWR	000	14/8		+3	
	PWR	119	14/8		+3	
3V062B	PWR	000	(X)14/8	203	+3	
	PWR	119	(X)14/8	203	+3	

SYMBOL NO. 8

MICROCONTROL B7

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B7	02-32	FA1022	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
DATA0	O	306	1/6		DATA0	5G7
DR00A	I	013	4/1		DR00	6A1
EFET.CK0	D	204	1/6		MA.FET0	5G7
ELINTRP0	D	302	1/2,1/3		TLINTRP0	6H6
ELMINT0	D	115	4/8,4/9 4/10,4/11 4/12,4/13 4/14,4/15		LMINT10	6G8
ELNOP00A	DT	202	1/5		TLNOP10	6G7
ELNOP00B	O	102	4/1,4/5 4/8,4/9 4/10,4/11 4/12,4/13 4/14,4/15		SIR.IB0	6G7
EN2D40	O	104	1/6		CONTRL0	5G8
ER.FNPT0	D	105	5/2		FNP.ER0	4H2
ER.IBPL0	D	205	5/2		IBPL.ER0	4H5
ERAMAR10	O	303	1/6		TALL010	6H5
ERMARMT0	D	301	5/2		MPSM0	5H3
ERU1	I	005	4/2		FRE20	5A6
FNOPT0	I	305	1/7		FN.PT0	4A2
GBPH0	I	213	2/2		PHID	5A4
IBPL.ER0	I	106	1/6	202	IBPT.CK0	4A5
IFF11	I	306	1/4		IFF11	6A2
INTPRSB0	I	109	5/3		INTRPI0	6A1

SYMBOL NO. 8 (CONT)

MICROCONTROL B7

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B7	02-32	FA1022	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MARP10	DT	004	1/5		TCA.MI10	6H5
MAR011A	I	317	1/3		MARB01I1	2A8
MAR021A	I	018	1/3		MARB02I1	2A7
MAR031A	I	218	1/3		MARB03I1	2A6
MAR041A	I	017	1/3		MARB04I1	2A6
MAR051A	I	217	1/2		MARB05I1	2A5
MAR061A	I	117	1/2		MARB06I1	2A4
MAR071A	I	315	1/2		MARB07I1	2A4
MAR081A	I	016	1/2		MARB08I1	2A3
MAR091	I	216	1/2		MARB09I1	2A2
MAR101	I	015	1/2		MARB10I1	2A2
MAR111	I	215	1/2		MARB11I1	2A1
MD.ZRU10	I	209	1/4		CLR.RU10	5A1
MPS030	I	107	12/8		MPSXXCB0	5A7
MPS050	I	207	12/8		MPSXXCA0	5A7
MPS070	I	312	12/8		MPSNA000	3A0
MPS090	I	112	12/8		MPSNA010	3A1
MPS110	I	212	12/8		MPSNA020	3A1
MPS130	I	012	12/8		MPSNA030	3A2
MPS150	I	311	12/8		MPSNA040	3A2
MPS170	I	111	12/7		MPSNA050	3A3
MPS190	I	211	12/7		MPSNA060	3A3
MPS210	I	011	12/7		MPSNA070	3A4
MPS230	I	310	12/7		MPSNA080	3A4
MPS250	I	110	12/7		MPSNA090	3A5
MPS270	I	210	12/7		MPSNA100	3A5
MPS290	I	010	12/7		MPSNA110	3A6
MPS310	I	113	12/7		MPSXPNA0	5A6
MRFSMAR0	I	007	7/19		CL.MINT0	6A9
MS100	I	009	5/12		CMSI0	5A3
NA20400	O	100	6/3		B204.00	4G8
NA20410	O	300	2/2,2/6 6/3		B204.10	4G7
NA2D420	O	001	2/2,2/6 2/9		B2D4.20	4H7
NA2D430	O	201	2/9		B204.30	4H6
P01	I	208	8/3		P01	6A0
P10	I	008	8/3		P10	5A4
P21	I	308	8/3		P21	5A0
P31	I	307	8/3		P31	5A2
RARPH0	D	101	1/6		RARP0	5H5
RAR011	I	316	1/1		RARB01I1	2A8
RAR021	I	116	1/1		RARB02I1	2A7
RAR031	I	314	1/1		RARB03I1	2A7
RAR041	I	114	1/1		RARB04I1	2A6
RAR051	I	219	1/1		RARB05I1	2A5
RAR061	I	019	1/1		RARB06I1	2A5
RAR071	I	318	1/1		RARB07I1	2A4
RAR081	I	118	1/1		RARB08I1	2A3
RAR091	I	214	1/1		RARB09I1	2A3
RAR101	I	014	1/1		RARB10I1	2A2
RAR111	I	313	1/1		RARB11I1	2A1
RU10	O	002	1/4		RU10	5H2
SSMINT0A	I	003	5/11		MINTI0	6A2
SSSTP0B	I	108	5/8		STDPI0	5A6
T1D4L10B	I	103	1/11		T1D4L10	5A4
T2D4LC0B	I	006	1/11		T2D4LC0	4A4
T2D4R60C	I	206	1/11		T2D4R60	4A4
T3D4R70B	I	203	1/11		T3D4R70	5A5

SYMBOL NO. 8 (CONT)

MICROCONTROL B7

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MC B7	02-32	FA1022	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
UTLFR20	I	309	5/8		UTLFR2I0	6A3
3T054E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054E	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 1
SYMBOL(S) 7 8

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	DWG SIZE C2	ISSUE 7D
			B1CD

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PART OF FS 1

MICROCONTROL

SYMBOL NO. 9

MISCELLANEOUS DECODER
PART B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MISCDECB	06-06	FA1034	0	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
F204L30B	I	316	1/13		F204L30	6A1
F204L31C	0	IC	7/20		F204L31C	5H1
F204RA0B	I	210	1/13		F204RA0	6A4
F204RA1A	0	IC	7/6,7/20		F204RA1A	6H4
F204RC0C	I	017	1/13		F204RC0	6A2
F204R60C	I	217	1/13		F204R60	6A7
F204R90B	I	108	1/13		F204R90	6A5
F204R91	0	IC	7/6,7/20		F204R91	6H4
ICP20B	0	IC	7/7		P20B	6H1
MD0IOCH0	0	110	10/1,10/5 10/9 TO CONN CKT		MD1000	6H6
MD1CHTN0	0	204	10/1,10/5 10/9 TO CONN CKT		MD1010	6H6
MD2CHTM0	0	318	10/1,10/5 10/9 TO CONN CKT		MD1020	6H4
MD3CHC0	0	118	10/1,10/5 10/9 TO CONN CKT		MD1030	6H3
MD4STCH0	0	317	6/5,10/2 10/6,10/10 TO CONN CKT		MD1040	5H5
MD5EIOS0	0	117	10/1,10/5 10/9 TO CONN CKT		MD1050	5H5
MD6RAI00	0	218	10/2,10/6 10/10 TO CONN CKT		MD1060	5H3
MD7SPA0	0	018	TO CONN CKT		MD1070	5H3
P21	I	010	8/3		P21	6A2
T104R80	I	019	1/11		T104R80	6A1
T304LE0	I	219	1/11		T304LE0	6A1
T304L70	I	201	1/11		T304L70	5A2

SYMBOL NO. 10

MISCELLANEOUS DECODER
PART E

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MISCDECE	02-23	FA1046	B	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
F204LCS0	0	302	6/3		F204LC10	6H1
F204LC0B	I	110	1/13		F204LC0	6A1
F204RA0B	I	002	1/13		F204RA0	6A1
F204R90B	I	310	1/13		F204R90	6A0
IF204LC1	0	IC	4/2		F204LC1	6B6
IF204RA1	0	IC	4/2		F204RA1	6B6
MD.BRPT0	0	303	8/4		MDR6C70	6H4
MDA.BD0A	OT	IC203	4/2		TSERCB0B	6G1
MDA.BD0B	OT	IC103	4/2		TSERCB0A	6G2
MDDI1SD0	0	003	11/1,11/2 11/3		MDR6C60	6H2
MDDK1SD0	0	102	11/1,11/2 11/3		MDR6C50	6H5
MDGD010A	OT	IC104	4/2		TSERCG0A	6G4

SYMBOL NO. 10 (CONT)

MISCELLANEOUS DECODER
PART E

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MISCDECE	02-23	FA1046	B	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
MDGD010B	OT	IC204	4/2		TSERCG0B	6G3
MD2010K0	0	202	11/1,11/2 11/3		MDR6C40	6H5
T104R80	I	301	1/11		T104R80	6A0
T304LB0B	I	001	1/11		T304LB0	6A5
T304L00	I	201	1/11		T304L00	6A4
T304LE0	I	101	1/11		T304LE0	6A3
T304L70	I	305	1/11		T304L70	6A2

SYMBOL NO. 11

TO DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TDECODER	06-34	FA1045	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
MPS020	I	216	12/8		MPS000	4A7
MPS060	I	116	12/8		MPS010	4A6
MPS100	I	316	12/8		MPS020	4A2
MPS140	I	017	12/8		MPS030	4A2
MPS180	I	217	12/7		MPS040	3A6
MPS220	I	117	12/7		MPS050	3A6
MPS260	I	317	12/7		MPS060	3A2
MPS300	I	018	12/7		MPS070	3A2
MS120	I	318	5/10		MS10	2A1
P01	I	218	8/3		IP01	2A2
P31	I	118	8/3		IP31	2A1
T104L10A	0	104	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		104L10A	5G0
T104L10B	0	313	1/1,1/4 1/8,1/12 1/14,2/1 2/5,4/1 4/3,6/1		104L10B	5G5
T104L20A	0	204	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		104L20A	5G0
T104L20B	0	014	1/12,1/14 2/1,2/5 4/1,4/3 6/1		104L20B	5G8
T104L40	0	103	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		104L40	5G1
T104L80	0	304	5/4,5/5 5/6,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14,6/1		104L80	5G1
T104R10	0	306	2/2,2/3 2/4,2/6 2/7,2/8 6/1,9/4		104R10	6G2

SYMBOL NO. 11 (CONT)

TO DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TDECODER	06-34	FA1045	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
T104R20	0	106	2/2,2/3 2/4,2/7 2/8,6/1 11/1,11/2 11/3		104R20	6G2
T104R40	0	307	2/2,2/3 2/4,2/7 2/8,6/1 11/1,11/2 11/3		104R40	6G3
T104R80	0	107	1/9,1/10 1/12,1/14 6/1		104R80	6G3
T204LA0A	0	309	6/1,7/8 7/11,7/12 7/13,7/14 7/15,7/16 7/17,7/18		204LA0A	5G2
T204LA0B	0	006	6/1,7/6 7/9,7/10		204LA0B	5G5
T204LC0A	0	109	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		204LC0A	5G1
T204LC0B	0	212	1/4,1/8 4/1,4/2 4/3,4/6 4/7,6/1		204LC0B	5G5
T204L30A	0	310	5/4,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14,6/1		204L30A	5G3
T204L30B	0	012	1/4,4/1 4/3,5/5 5/6,6/1 7/20		204L30B	5G6
T204L50A	0	110	1/7,3/1 3/2,3/3 3/4,3/5 3/6,3/7 3/8,3/9 6/1		204L50A	5G3
T204L50B	0	213	6/1		204L50B	5G6
T204L60A	0	209	1/7,3/1 3/2,3/3 3/4,3/5 3/6,3/7 3/8,3/9 6/1		204L60A	5G2
T204L60B	0	113	6/1		204L60B	5G7
T204L90A	0	009	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		204L90A	5G2
T204L90B	0	206	4/6,4/7 6/1,9/2 9/3		204L90B	5G6
T204RA0A	0	311	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		204RA0A	6G4
T204RA0B	0	215	1/4,4/1 4/2,4/3 6/1,7/6		204RA0B	7G3
T204RC0A	0	111	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		204RC0A	6G3

SYMBOL NO. 11 (CONT)

TO DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TDECODER	06-34	FA1045	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
T204RC0B	0	315	6/1,7/8 7/11,7/12 7/13,7/14 7/15,7/16 7/17,7/18		204RC0B	7G2
T204RC0C	0	115	1/4,4/1 4/3,6/1 7/6,7/9 7/10		204RC0C	7G3
T204R30A	0	208	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		204R30A	6G5
T204R30B	0	114	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		204R30B	7G6
T204R30C	0	016	1/4,4/1 4/3,4/6 4/7,6/1 9/2,9/3		204R30C	7G6
T204R50A	0	008	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		204R50A	6G5
T204R50B	0	015	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		204R50B	7G5
T204R50C	0	314	1/4,4/1 4/3,4/6 4/7,6/1		204R50C	7G5
T204R60A	0	211	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		204R60A	6G4
T204R60B	0	112	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/1		204R60B	7G4
T204R60C	0	312	1/8,4/6 4/7,6/1		204R60C	7G5
T204R90A	0	011	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		204R90A	6G4
T204R90B	0	013	1/4,6/1 7/6,9/2 9/3		204R90B	7G3
T304LB0A	0	010	1/7,2/2 2/3,2/4 2/6,2/7 2/8,6/1		304LB0A	5G4
T304LB0B	0	214	1/10,1/12		304LB0B	5G8

PART OF FS 1
SYMBOL(S) 9 10 11

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

BELL LABORATORIES
SD-1C900-01
B1CE

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12/01/77

PART OF FS 1

MICROCONTROL

SYMBOL NO. 11 (CONT)

TO DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TDECODER	06-34	FA1045	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			1/14,6/1			
T304LD0	0	004	1/10,1/12 1/14,2/2 2/4,2/6 2/8,6/1		304LD0	5G4
T304LE0	0	303	1/9,1/10 6/1,9/4 11/1,11/2 11/3		304LE0	5G3
T304L70	0	210	1/9,1/10 2/2,2/3 2/4,2/6 2/7,2/8 6/1		304L70	5G4
T304RB0A	0	108	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		304RB0A	6G6
T304RB0B	0	019	1/4,2/1 2/5,4/1 4/3,5/5 5/6,6/1		304RB0B	7G4
T304R00A	0	207	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		304R00A	6G6
T304RD0B	0	305	1/12.1/14 2/1,2/5 6/1		304R00B	7G7
T304RE0A	0	007	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,4/1 4/3,6/1		304RE0A	6G5
T304RE0B	0	105	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,5/5 5/6,6/1		304RE0B	7G6
T304R70A	0	308	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/1		304R70A	6G6
T304R70B	0	219	1/1,1/8 2/1,2/5 6/1		304R70B	7G4
T404L0	0	005	6/1		404LC	5G7
T404R0	0	205	2/2,2/6 6/1		404R0	7G2
XT3.6B00	I	002	1/7	202	IBT000	4A8
XT3.6B10	I	202	1/7	202	IBT010	4A5
XT3.6B20	I	102	1/7	202	IBT020	4A4
XT3.6B30	I	302	1/7	202	IBT030	4A1
XT3.6B40	I	003	1/7	202	IBT040	3A6
XT3.6B50	I	203	1/7	202	IBT050	3A4
YT3.6B00	I	301	1/7	202	IBTS000	4A9
YT3.6B10	I	101	1/7	202	IBTS010	4A5
YT3.6B20	I	201	1/7	202	IBTS020	4A4
YT3.6B30	I	001	1/7	202	IBTS030	4A1
YT3.6B40	I	300	1/7	202	IBTS040	3A7
YT3.6B50	I	100	1/7	202	IBTS050	3A4
3T058F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	

SYMBOL NO. 11 (CONT)

TO DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TDECODER	06-34	FA1045	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058F	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V058F	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 12

MISCELLANEOUS DECODER
PART C

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MISCDECC	02-19	FA1030	C	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F204LC0B	I	109	1/13		FL3.LC0	7A0
F204L30B	I	206	1/13		FR8.L30	7A4
F204RA0B	I	309	1/13		F204RA0	7A0
F204R60C	I	006	1/13		FLO.R60	7A4
F204R90B	I	010	1/13		FLE.R90	7A5
MD.BRTI0	0	204	8/4		MDR02C40	7G6
MD.IMTC0	0	004	6/4,7/19		MDR02C30	7G6
MD.SBAK0	0	203	6/4		MDR47C50	7G1
MD.SBTC0	OT I	304	7/19,9/4 5/11,8/4		MDR13C10	7G8
MD.SDIS0	OT	205	7/20		MDR13C30	7G7
MD.SSTP0	0	302	9/4 7/19		MDR47C30	7G2
MD.STSW0	OT I	003	8/4 7/19		MDR47C40	7G2
MD.S10B0	0	303	7/4,7/5		MDR02C20	7G6
MD.S20B0	0	005	7/1,7/4 7/5		MDR13C20	7G7
MDOML1C0	0	104	5/4,5/5 5/6,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14		MDR02C50	7G4
MDIDSW00	OT I	202	7/19 9/1		MDR47C20	7G3
MDINCPR0	0	305	8/4		MDR13C50	7G5
MDINCTC0	0	105	8/4		MDR13C40	7G5
MDIODRB0	0	103	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9		MDR02C10	7G8
T104L10B	I	011	1/11		T104L10	7A2
T104L20B	I	209	1/11		T104L20	7A3
T104R80	I	110	1/11		T104R80	7A1
T304LB0B	I	310	1/11		T304LB0	7A1
T304LD0	I	100	1/11		T304LD0	7A2
T304R00B	I	009	1/11		T304R00	7A3
T8304RB1	I	IC	5/6		T304RB1	7A3

SYMBOL NO. 13

FROM DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FDECODER	06-33	FA1011	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F104L10A	0	104	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		104L10A	5G0
F104L10B	0	313	1/1,4/31 6/2,11/1 11/2,11/3		104L10B	5G5
F104L20A	0	204	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		104L20A	5G0
F104L20B	0	014	4/11,4/12 6/2,9/4 11/1,11/2 11/3		104L20B	5G8
F104L40	0	103	1/7,3/1 3/2,3/3 3/4,3/5 3/6,3/7 3/8,3/9 6/2		104L40	5G1
F104L80	0	304	5/4,5/5 5/6,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14,6/2		104L80	5G1
F104R10	0	306	1/4,2/2 2/3,2/4 2/6,2/7 2/8,6/2		104R10	6G2
F104R20	0	106	1/7,2/2 2/3,2/4 2/6,2/7 2/8,6/2		104R20	6G2
F104R40	0	307	1/4,1/7 2/2,2/3 2/4,6/2		104R40	6G3
F104R80	0	107	1/4,1/14 2/2,2/6 6/2		104R80	6G3
F204LA0A	0	309	4/15,6/2 7/8,7/11 7/12,7/13 7/14,7/15 7/16,7/17 7/18		204LA0A	5G2
F204LA0B	0	006	6/2,7/6 7/9,7/10		204LA0B	5G5
F204LC0A	0	109	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		204LC0A	5G1
F204LC0B	0	212	1/4,1/10 1/12,2/1 2/5,4/1 4/3,4/6 4/7,6/2		204LC0B	5G5
F204L30A	0	310	5/4,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14,6/2		204L30A	5G3
F204L30B	0	012	1/4,1/9 1/12,1/14 2/1,2/5 5/5,5/6 6/2		204L30B	5G6
F204L50A	0	110	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204L50A	5G3

SYMBOL NO. 13 (CONT)

FROM DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FDECODER	06-33	FA1011	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F204L50B	0	213	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204L50B	5G6
F204L60A	0	209	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204L60A	5G2
F204L60B	0	113	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204L60B	5G7
F204L90A	0	009	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		204L90A	5G2
F204L90B	0	206	4/1,4/2 4/3,4/6 4/7,6/2 8/4,9/2 9/3		204L90B	5G6
F204RA0A	0	311	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204RA0A	6G4
F204RA0B	0	215	1/4,1/9 1/10,1/12 1/14,2/1 2/5,4/1 4/3,6/2		204RA0B	7G3
F204RC0A	0	111	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204RC0A	6G3
F204RC0B	0	315	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		204RC0B	7G2
F204RC0C	0	115	1/4,1/9 2/1,2/5 4/6,4/7 6/2		204RC0C	7G3
F204R30A	0	208	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204R30A	6G5
F204R30B	0	114	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		204R30B	7G6
F204R30C	0	016	1/4,6/2 6/3,7/9		204R30C	7G6

PART OF FS 1
SYMBOL(S) 11 12 13

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B1CF

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PART OF FS 1

MICROCONTROL

SYMBOL NO. 13 (CONT)

FROM DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FDECODER	06-33	FA101I	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			7/10,8/4			
F204R50A	0	008	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204R50A	6G5
F204R50B	0	015	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		204R50R	7G5
F204R50C	0	314	1/4,4/6 4/7,6/2 6/3		204R30C	7G5
F204R60A	0	211	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204R60A	6G4
F204R60B	0	112	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,6/2		204R60B	7G4
F204R60C	0	312	1/4,1/9 1/12,4/6 4/7,6/2		204R60C	7G5
F204R90A	0	011	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		204R90A	6G4
F204R90B	0	013	1/4,1/9 1/10,1/12 2/1,2/5 6/2,9/2 9/3		204R90B	7G3
F304LB0A	0	010	2/2,2/3 2/4,6/2		304LB0A	5G4
F304LB0B	0	214	2/6,2/7 2/8,6/2		304LB0B	5G8
F304LD0	0	004	1/4,1/7 1/14,2/2 2/3,2/4 2/6,2/7 2/8,6/2		304LD0	5G4
F304LE0	0	303	1/4,1/14 2/2,2/3 2/4,2/6 2/7,2/8 6/2		304LE0	5G3
F304L70	0	210	1/4,1/7 2/2,2/3 2/4,2/6 2/7,2/8 6/2		304L70	5G4
F304RB0A	0	108	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		304RB0A	6G6
F304RB0B	0	019	4/10,6/2		304RB0B	7G4
F304RD0A	0	207	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		304RD0A	6G6
F304RD0B	0	305	6/2,11/1 11/2,11/3		304RD0B	7G7
F304RE0A	0	007	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,5/5 6/2		304RE0A	6G5

SYMBOL NO. 13 (CONT)

FROM DECODER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FDECODER	06-33	FA101I	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F304RE0B	0	105	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15,5/6 6/2		304RE0B	7G6
F304R70A	0	308	3/1,3/2 3/3,3/4 3/5,3/6 3/7,3/8 3/9,6/2		304R70A	6G6
F304R70B	0	219	1/1,4/5 6/2,9/4		304R70B	7G4
F404L0	0	005	6/2,6/3		404L0	5G7
F404R0	0	205	6/2		404R0	7G2
MPS000	I	216	12/8		MPS000	4A7
MPS040	I	116	12/8		MPS010	4A6
MPS080	I	316	12/8		MPS020	4A3
MPS120	I	017	12/8		MPS030	4A2
MPS160	I	217	12/7		MPS040	3A6
MPS200	I	117	12/7		MPS050	3A6
MPS240	I	317	12/7		MPS060	3A2
MPS280	I	018	12/7		MPS070	3A2
P01	I	218	8/3		IP01A	2A2
XT3.6B00	I	301	1/7	202	IBTS000	4A8
XT3.6B10	I	101	1/7	202	IBTS010	4A5
XT3.6B20	I	201	1/7	202	IBTS020	4A4
XT3.6B30	I	001	1/7	202	IBTS030	4A1
XT3.6B40	I	300	1/7	202	IBTS040	3A8
XT3.6B50	I	100	1/7	202	IBTS050	3A4
YT3.6B00	I	002	1/7	202	IBT000	4A8
YT3.6B10	I	202	1/7	202	IBT010	4A5
YT3.6B20	I	102	1/7	202	IBT020	4A4
YT3.6B30	I	302	1/7	202	IBT030	4A1
YT3.6B40	I	003	1/7	202	IBT040	3A7
YT3.6B50	I	203	1/7	202	IBT050	3A4
3T058F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0633T	I	118			IP3S1	2A1
	I	318			IP01	2A1
	GRD	319			GRD	
3V058F	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 14

MISCELLANEOUS DECODER
PART 0

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MISCDECO	02-20	FA1030	C	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F104R80	I	206	1/13		FR8.L30	7A4
F204L30B	I	109	1/13		FL3.LC0	7A0
F204RA0B	I	309	1/13		F204RA0	7A0
F304LD0	I	006	1/13		FL0.R60	7A4
F304LE0	I	010	1/13		FLE.R90	7A5
MD.S30B0	0	302	7/4,7/5		MDR47C30	7G2
MD.2ER0	0	304	9/4 5/1,5/2		MDR13C10	7G8
MD.2MIN0	OT I	005	7/19 5/11		MDR13C20	7G7
MD.2MS0	OT I	105	7/19,9/4 5/4,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14		MDR13C40	7G5
MD.ZPT0	OT I	305	7/20,9/4 8/4		MDR13C50	7G5
MDIOMCH0	OT I	204	7/19 9/1,9/4		MDR02C40	7G6
MOIOCC0	0	205	TO CONN CKT		MDR13C30	7G7
MDMCBTR0	0	202	9/4 9/1,9/2 9/3		MDR47C20	7G3
MDMCLST0	0	203	9/4		MDR47C50	7G1
MOMRFCC0	OT I	303	7/1 7/19		MDR02C20	7G6
MDPYMCH0	0	103	9/2		MDR02C10	7G8
MDRARFN0	0	003	2/2,2/6		MDR47C40	7G2
MDSTMCH0	0	104	9/1		MDR02C50	7G4
MOTMCH0	0	004	9/4		MDR02C30	7G6
T104L10B	I	011	1/11		T104L10	7A2
T104L20B	I	209	1/11		T104L20	7A3
T104R80	I	110	1/11		T104R80	7A1
T304LB0B	I	310	1/11		T304LB0	7A1
T304L00	I	100	1/11		T304L00	7A2
T304RD0B	I	009	1/11		T304RD0	7A3
T9304RB1	I	IC	5/5		T304RB1	7A3

PART OF FS 1
SYMBOL(S) 13 14

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	B1CG

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12/01/77

PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM I

FUNCTION PARTITIONING OF MICROCONTROL LOGIC

CIRCUIT OPERATION

THE MICROPROGRAM CONTROL IS THE SOURCE OF ALMOST ALL CONTROL AND SEQUENCING FUNCTIONS IN THE 3A CC. THE MAINTENANCE CHANNEL, THE I/O CHANNEL, AND THE PROCESSOR BUS CONTROLLER ARE THE MAJOR EXCEPTIONS. THESE ENTITIES ARE UNDER DIRECT MICROPROGRAM CONTROL AND THEIR OPERATIONS ARE USUALLY INITIATED AND TERMINATED BY MICROPROGRAM CONTROL OPERATIONS. THERE ARE TWO MAJOR OPERATIONS PERFORMED BY THE MICROPROGRAM CONTROL:

(1) DECODING AND HENCE ACTIVATING CONTROL FUNCTIONS THAT ARE ACCESSED FROM THE MICROPROGRAM STORE IN THE FORM OF CONTROL CONSTANTS.

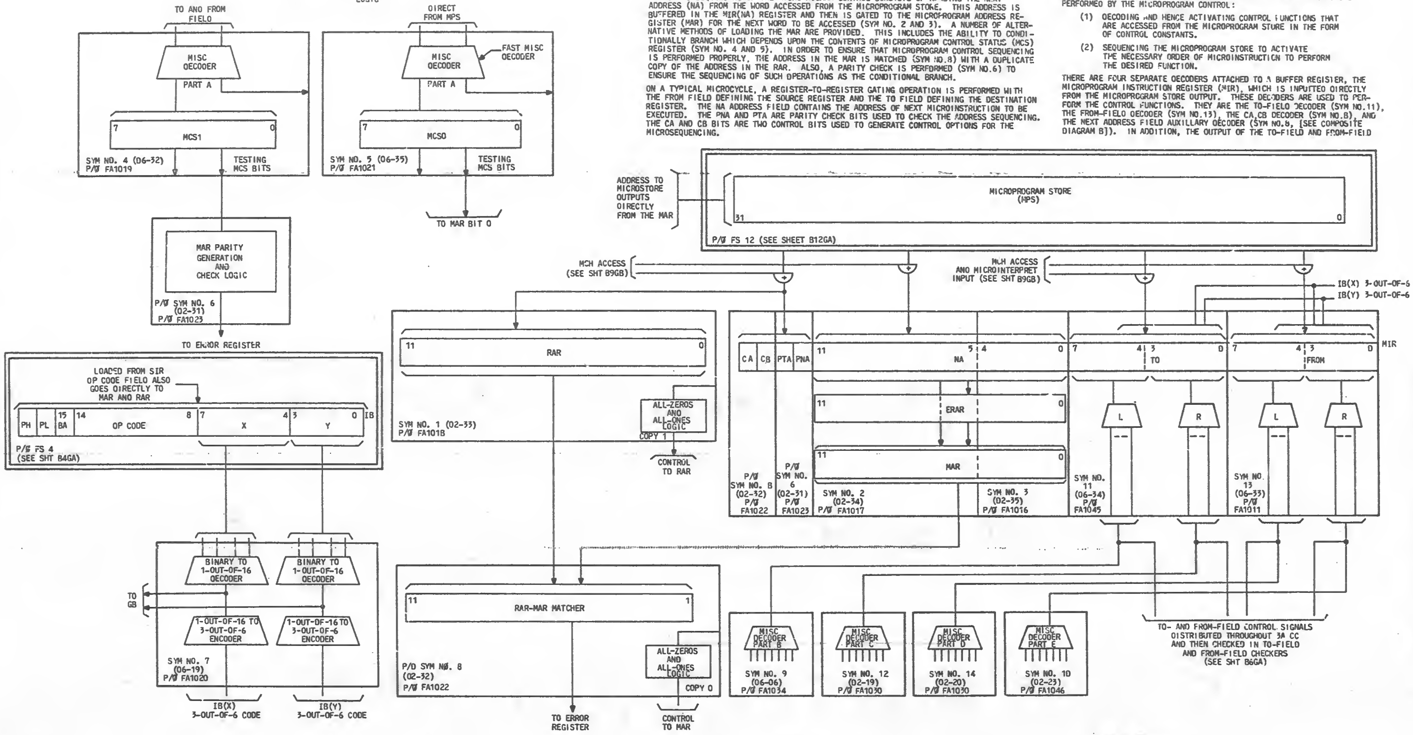
(2) SEQUENCING THE MICROPROGRAM STORE TO ACTIVATE THE NECESSARY ORDER OF MICROINSTRUCTION TO PERFORM THE DESIRED FUNCTION.

THERE ARE FOUR SEPARATE DECODERS ATTACHED TO A BUFFER REGISTER, THE MICROPROGRAM INSTRUCTION REGISTER (MIR), WHICH IS INPUTTED DIRECTLY FROM THE MICROPROGRAM STORE OUTPUT. THESE DECODERS ARE USED TO PERFORM THE CONTROL FUNCTIONS. THEY ARE THE TO-FIELD DECODER (SYM NO.11), THE FROM-FIELD DECODER (SYM NO.13), THE CA,CB DECODER (SYM NO.B), AND THE NEXT ADDRESS FIELD AUXILLARY DECODER (SYM NO.8, [SEE COMPOSITE DIAGRAM B]). IN ADDITION, THE OUTPUT OF THE TO-FIELD AND FROM-FIELD DECODERS GENERATE A MISCELLANEOUS DECODER MATRIX (SYM NO. 4, 5, 9, 10, 12 AND 14). SO ALL CONTROL CONSTANTS REQUIRED TO SELECT A TO OR FROM CONTROL POINT DO NOT HAVE TO RESIDE IN THE MICROPROGRAM STORE, A PAIR OF TRANSLATORS (SYM NO.7) IS PROVIDED BETWEEN THE X AND Y FIELDS IN THE IB REGISTER (SEE FS 4) AND THE TO-FIELD AND FROM-FIELD INPUTS TO THE MIR REGISTER.

CIRCUIT OPERATION (CONT)

THE BASIC SEQUENCING OF THE MICROPROGRAM CONTROL CONSISTS OF READING THE NEXT ADDRESS (NA) FROM THE WORD ACCESSED FROM THE MICROPROGRAM STORE. THIS ADDRESS IS BUFFERED IN THE MIR(NA) REGISTER AND THEN IS GATED TO THE MICROPROGRAM ADDRESS REGISTER (MAR) FOR THE NEXT WORD TO BE ACCESSED (SYM NO. 2 AND 3). A NUMBER OF ALTERNATIVE METHODS OF LOADING THE MAR ARE PROVIDED. THIS INCLUDES THE ABILITY TO CONDITIONALLY BRANCH WHICH DEPENDS UPON THE CONTENTS OF MICROPROGRAM CONTROL STATUS (MCS) REGISTER (SYM NO. 4 AND 5). IN ORDER TO ENSURE THAT MICROPROGRAM CONTROL SEQUENCING IS PERFORMED PROPERLY, THE ADDRESS IN THE MAR IS MATCHED (SYM NO.8) WITH A DUPLICATE COPY OF THE ADDRESS IN THE RAR. ALSO, A PARITY CHECK IS PERFORMED (SYM NO.6) TO ENSURE THE SEQUENCING OF SUCH OPERATIONS AS THE CONDITIONAL BRANCH.

ON A TYPICAL MICROCYCLE, A REGISTER-TO-REGISTER GATING OPERATION IS PERFORMED WITH THE FROM FIELD DEFINING THE SOURCE REGISTER AND THE TO FIELD DEFINING THE DESTINATION REGISTER. THE NA ADDRESS FIELD CONTAINS THE ADDRESS OF NEXT MICROINSTRUCTION TO BE EXECUTED. THE PNA AND PTA ARE PARITY CHECK BITS USED TO CHECK THE ADDRESS SEQUENCING. THE CA AND CB BITS ARE TWO CONTROL BITS USED TO GENERATE CONTROL OPTIONS FOR THE MICROSEQUENCING.



PART OF FS 1
COMPOSITE DIAGRAM 1

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B1GA

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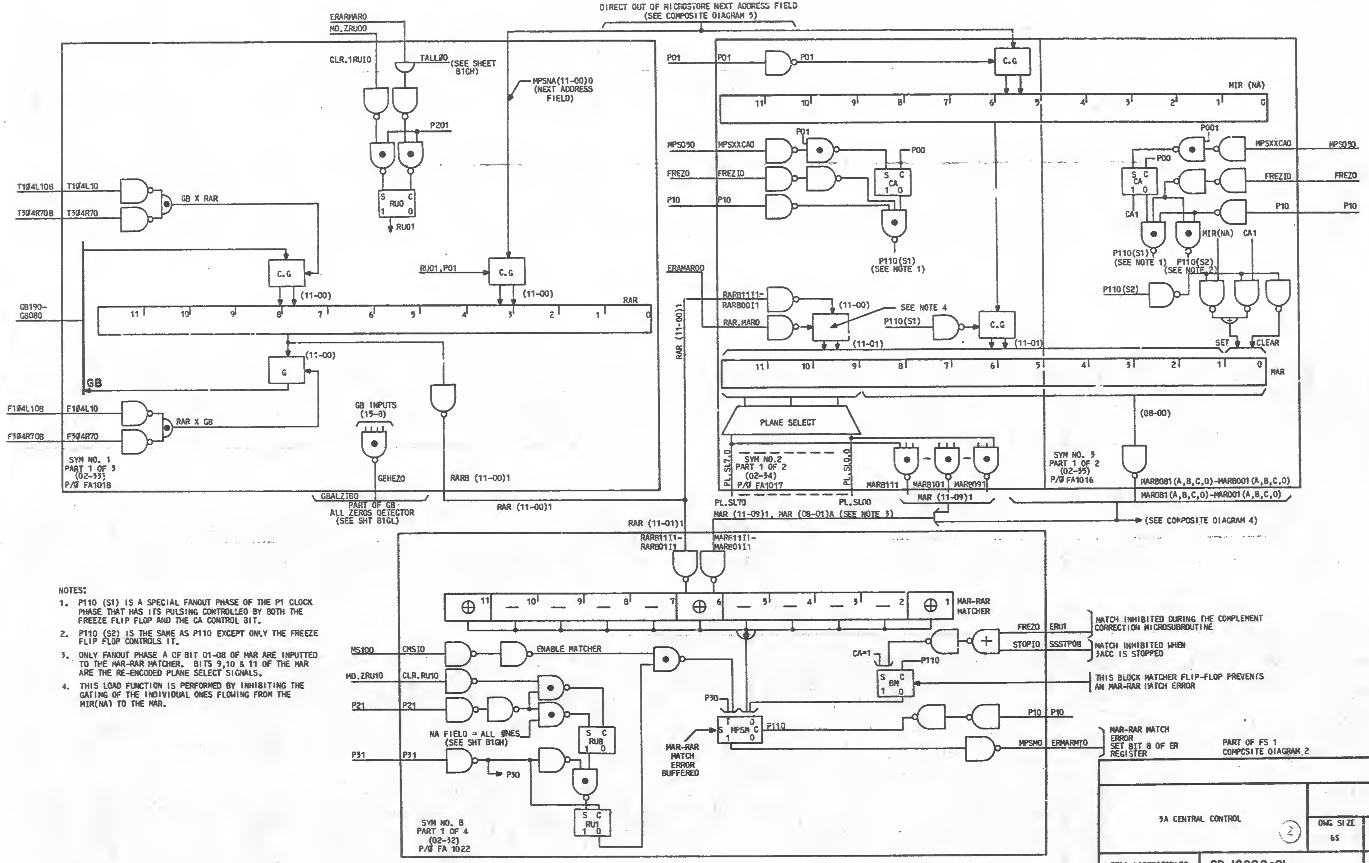
PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 2

BASIC MICROCONTROL ADDRESS SEQUENCING AND CHECK LOGIC

CIRCUIT OPERATION
(SEE SHEETS B1CC, B1GN, B1GP)



NOTES:

1. P110 (S1) IS A SPECIAL FANOUT PHASE OF THE P1 CLOCK PHASE THAT HAS ITS PULSING CONTROLLED BY BOTH THE FREEZE FLIP FLOP AND THE CA CONTROL BIT.
2. P110 (S2) IS THE SAME AS P110 EXCEPT ONLY THE FREEZE FLIP FLOP CONTROLS IT.
3. ONLY FANOUT PHASE A OF BIT 01-08 OF MAR ARE INPUTTED TO THE MAR-RAR MATCHER. BITS 9,10 & 11 OF THE MAR ARE THE RE-ENCODED PLANE SELECT SIGNALS.
4. THIS LOAD FUNCTION IS PERFORMED BY INHIBITING THE GATING OF THE INDIVIDUAL ONES FLOWING FROM THE MIR(NA) TO THE MAR.

PART OF FS 1
COMPOSITE DIAGRAM 2

3A CENTRAL CONTROL

②

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES

SD-1C900-01

B1GB

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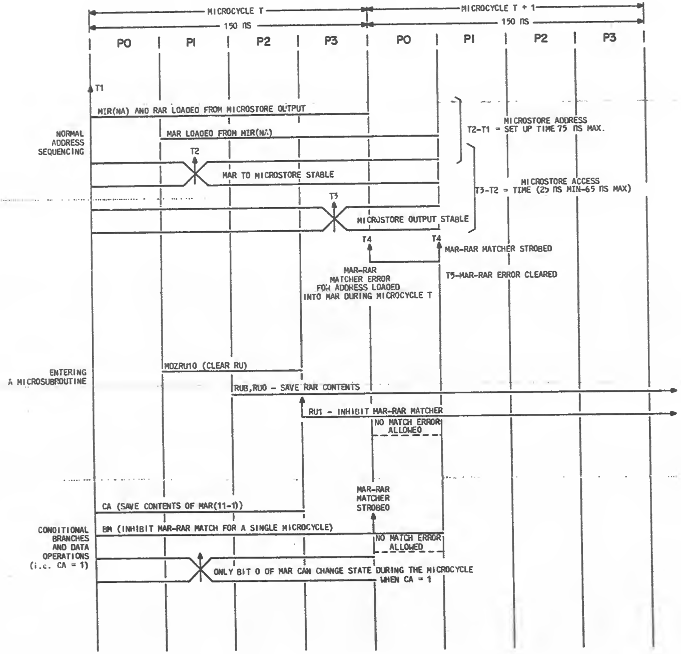
PART OF FS 1

MICROCONTROL

COMPOSITE DIAGRAM 3

BASIC TIMING OF MICROCONTROL ADDRESS
SEQUENCING AND CHECKING


MICROCYCLE T
MICROCYCLE T + 1
150 ns
150 ns
P0
P1
P2
P3
P0
P1
P2
P3
T1
MIR(NA) AND RAR LOADED FROM MICROSTORE OUTPUT
NORMAL ADDRESS SEQUENCING
MAR LOADED FROM MIR(NA)
T2
MAR TO MICROSTORE STABLE
T2-T1 = MICROSTORE ADDRESS SET UP TIME 75 ns MAX.
T3
MICROSTORE OUTPUT STABLE
T3-T2 = MICROSTORE ACCESS TIME (25 ns MIN-65 ns MAX)
T4
T4
MAR-RAR MATCHER STROBED
MAR-RAR MATCHER ERROR FOR ADDRESS LOADED INTO MAR DURING MICROCYCLE T
T5-MAR-RAR ERROR CLEARED
ENTERING A MICROSUBROUTINE
MOZRU10 (CLEAR RU)
RUB,RU0 - SAVE RAR CONTENTS
RU1 - INHIBIT MAR-RAR MATCHER
NO MATCH ERROR ALLOWED
MAR-RAR MATCHER STROBED
CA (SAVE CONTENTS OF MAR(11-1))
CONDITIONAL BRANCHES AND DATA OPERATIONS (i.e. CA = 1)
BM (INHIBIT MAR-RAR MATCH FOR A SINGLE MICROCYCLE)
NO MATCH ERROR ALLOWED
ONLY BIT 0 OF MAR CAN CHANGE STATE DURING THE MICROCYCLE WHEN CA = 1

CIRCUIT OPERATION

GENERAL OPERATION OF THE MICROPROGRAM CONTROL

MICROINSTRUCTIONS

THE BASIC MICROINSTRUCTION SET IS CENTERED AROUND A REGISTER-TO-REGISTER GATING OPERATION. IN ITS SIMPLEST FORM, THIS GATING FUNCTION IS THE SETTING OR CLEARING OF INDIVEDUAL FLIP-FLOPS. IN ORDER TO PERFORM THE GATING OPERATION, A TO-AND-FROM ENCODED CONTROL FIELD IS READ OUT OF THE MICROSTORE ON EACH MICROINSTRUCTION. THESE FIELDS ARE DECODED AND ARE USED TO ENABLE A SOURCE AND A DESTINATION REGISTER FOR THE NORMAL GATING COMMAND (SEE SHEET B6GA).

ON A TYPICAL MICROCYCLE, A SOURCE REGISTER IS SELECTED BY A FROM-FIELD CONTROL CONSTANT WHICH RESULTS WHEN THIS REGISTER IS GATED ONTO A COMMON GATING BUS (GB). ON THIS SAME MICROCYCLE, THE CONTENTS OF THE GB ARE ENABLED INTO A DESTINATION REGISTER BY A TO-FIELD CONSTANT. THE RESULT OF THIS TYPE OF ARCHITECTURE AND OPERATION IS THAT THE 3A CC BASICALLY CONSISTS OF A SET OF DATA AND STATUS REGISTERS WITH THE MICROPROGRAM CONTROL PROVIDING THE ABILITY TO GATE ONE TO ANOTHER. WHEN ARITHMETIC LOGIC OR OTHER NON-GATING FUNCTIONS ARE REQUIRED, COMBINATIONAL LOGIC IS ATTACHED TO THE OUTPUT OF SOME OF THE REGISTERS (SEE FS 2) AND THEN THE OUTPUT OF THIS LOGIC IS GATED VIA MICROPROGRAM CONTROL TO A DESTINATION REGISTER.

SEQUENCING

IN THE MICROPROGAM CONTROL, EACH TIME A WORD IS READ OUT OF THE MICROSTORE, AN ADDRESS IS INCLUDED AS IS THE MICROINSTUCTION TO BE PERFORMED. THE ADDRESS IS THEN USED TO TRANSFER TO NEXT MICROINSTRUCTION IN A PARTICULAR SEQUENCE. IN ORDER TO PROVIDE A FLEXIBLE AND EFFICIENT MICROCONTROL DESIGN, A NUMBER OF OPTIONS ARE PROVIDED FOR SEQUENCING THE MICROCONTROL. THE OPTIONS OR ALTERNATIVE WAYS THAT THE NEXT ADDRESS (NA) CAN BE OBTAINED IN A MICROINSTRUCTION SEQUENCED ARE AS FOLLOWS:

1. THE INITIAL MICROINSTRUCTION OF A MACHINE OPERATION CODE IS INTIATED BY HAVING THE MICROCONTROL SITTING IN A MICROLOOP WAITING FOR THE MAIN MEMORY TO FETCH AN INSTRUCTION. THE LOOP IS EXITED WHEN THE MAIN MEMORY FETCH IS COMPLETED AND THE RESULT OF THE FETCH IS GATED INTO THE MICROSTORE ADDRESS REGISTER (MAR) STARTING THE MICROINSTRUCTION SEQUENCE FOR THAT OP CODE.
2. ON A NUMBER OF MICROINSTRUCTIONS, IT IS DESIRABLE TO OBTAIN DATA CONSTANTS FROM THE MICROSTORE. IT IS ADVANTAGEOUS TO STORE THIS DATA IN THE NA FIELD AND TO OBTAIN THE NEXT ADDRESS BY INCREMENTING THE PREVIOUS CONTENTS OF THE MAR. THREE DIFFERENT USES OF THIS TYPE OF OPERATION ARE IMPLEMENTED AS FOLLOWS:
    - A. TO OBTAIN DATA CONSTANTS. DATA CONSTANTS, FOR EXAMPLE, CAN BE USED TO GENERATE TARGET ADDRESSES IN MAIN MEMORY, FOR INTERRUPT PROCESSING OR FOR GENERATING MATCH CONSTANTS TO TEST FOR UNIQUE BIT PATTERNS IN THE DML LOGIC.
    - B. TO OBTAIN ADDITIONAL CONTROL CONSTANTS. THE MAIN USE OF THIS IS THE SIMULTANEOUS LOADING OF THE CONTROL STATES INTO THE DML WITH A NORMAL MICROINSTRUCTION LOADING OF THE OPERAND FIELDS.
    - C. TO LOAD THE RETURN ADDRESS REGISTER (RAR) THAT IS USED IN CONJUNCTION WITH THE MICROCONTROL TO IMPLEMENT SUBROUTINE RETURNS. THIS ALSO REDUCES THE AMOUNT OF MICROCODE NEEDED.
3. TO CONDITIONALLY TRANSFER ON A NUMBER OF STATUS BITS. THIS ALLOWS CONVENIENT TESTING OF VARIOUS MACHINE STATES SUCH AS ADDER OVERFLOWS FROM THE DML OR TO LOOP WAITING FOR A COMPLETION SIGNAL. THE LATTER IS MOST USEFUL FOR PROVIDING THE ASYNCHRONOUS TIMING BETWEEN THE PROCESSOR AND PERIPHERAL UNITS.

CIRCUIT OPERATION (CONT)

4. THE ABILITY TO INDEX INTO MICROSTORE IS PROVIDED BY "OR"ING A 4-BIT BINARY FIELD INTO THE ADDRESS IN THE MAR. INDEXING EFFECTIVELY UTILIZES THE MICROSTORE BY PROVIDING AN EFFICIENT METHOD OF EXTRACTING DATA OR CONTROL FROM TABLE STRUCTURES IN THE MICROPROGRAM STORE.
5. INTERRUPTS ARE INITIATED BY JAMMING A HARDWIRED ADDRESS INTO THE MAR. THIS ADDRESS POINTS TO A MICROINSTRUCTION SEQUENCE WHICH INTERROGATES VARIOUS MACHINE STATES AND THEN DETERMINES WHAT ACTION IS TO BE TAKEN. THIS FEATURE SIMPLIFIES WHAT WOULD OTHERWISE BE A COMPLICATED AND DIFFICULT LOGIC TO CHECK. IT ALSO PROVIDES A HIGHLY FLEXIBLE AND EASILY MODIFIED INTERRUPT STRUCTURE.
6. THE MAINTENANCE RESET FUNCTION (MRF) ALSO RESULTS IN A HARDWIRED ADDRESS BEING JAMMED INTO THE MAR. THE MRF RESULTS IN THE EXECUTION OF A SEQUENCE OF MICROINSTRUCTION THAT WILL INITIALIZE THE 3A CC. DEPENDING UPON THE STATE OF THE MACHINE, THE MICROCODE INITIALIZATION MAY CONSIST OF INITIALIZATION OF ONLY A FEW REGISTERS TO THE LOADING OF THE MAIN STORE FROM THE TAPE UNIT.

EXECUTION RATE

THE MICROCONTROL IS DESIGNED AROUND A HIGH-SPEED PROGRAMMABLE READ-ONLY MEMORY (PROM) WHICH HAS A MINIMUM ACCESS TIME OF 25ns AND A MAXIMUM ACCESS TIME OF 65ns. THE MINIMUM CYCLE TIME OF MICROINSTRUCTION SEQUENCE IS DETERMINED BY THIS ACCESS TIME PLUS THE TIME NECESSARY TO CALCULATE THE ADDRESS OF THE WORD TO BE ACCESSED AND/OR THE MAXIMUM TIME TO EXECUTE EACH MICROINSTRUCTION. THE DESIGN OF THE PROCESSOR HAS BEEN IMPLEMENTED USING THE 1A FAMILY OF LOGIC WITH A TYPICAL GATE DELAY OF 5-7 ns. THE USE OF THE 1A GATE TECHNOLOGY AND THE 25-TO-65ns PROM RESULTS IN A MICROCYCLE EXECUTION TIME OF 150ns WHICH IS FIXED BY THE 3A CC CLOCK (SEE FS B).

PART OF FS 1
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

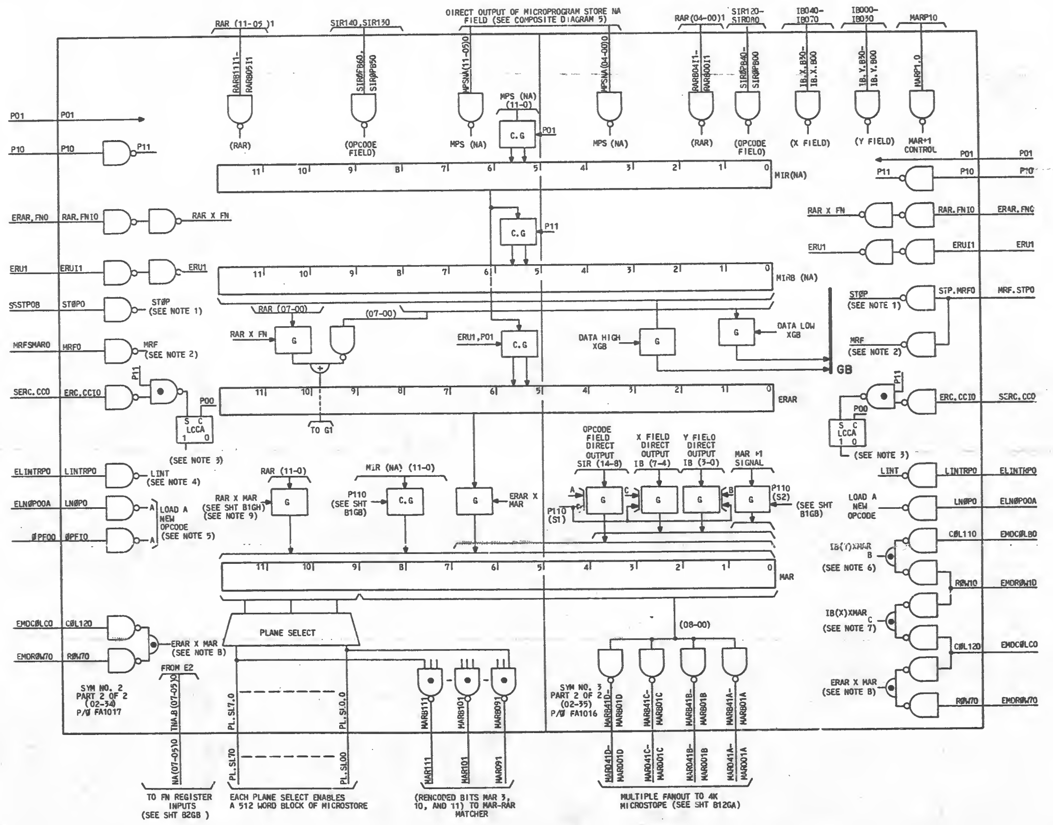
BIGC

PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 4

ADDITIONAL CONTROL LOGIC TO LOAD THE MAR AND TO OBTAIN DATA FROM THE MICROSTORE



CIRCUIT OPERATION
(SEE SHEETS B1GN, B1GP)

NOTES:

1. LOAD MAR WITH STOP ADDRESS CONSTANT 0(0377).
2. LOAD MAR WITH MRF ADDRESS CONSTANT 0(0277).
3. LOAD MAR WITH COMPLEMENT CORRECTION STARTING ADDRESS 0(0777). [SEE SHEET 011].
4. LOAD MAR WITH INTERRUPT STARTING ADDRESS 0(0120).
5. LOAD MAR OPCODE FIELD FROM THE SIR AND IF ØPF = 0, JAM BIT 8 = 1,
   IF ØPF = 1, JAM BIT 11 = 1.
6. LOAD MAR (3-0) WITH IB X FIELD.
7. LOAD MAR (3-0) WITH IB X FIELD.
8. LOAD MAR FROM THE ERAR (EXIT COMPLEMENT CORRECTION MICROSUBROUTINE).
9. LOAD MAR FROM THE RAR (EXIT FROM A NORMAL MICROSUBROUTINE).

PART OF FS 1
COMPOSITE DIAGRAM 4

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B1GD

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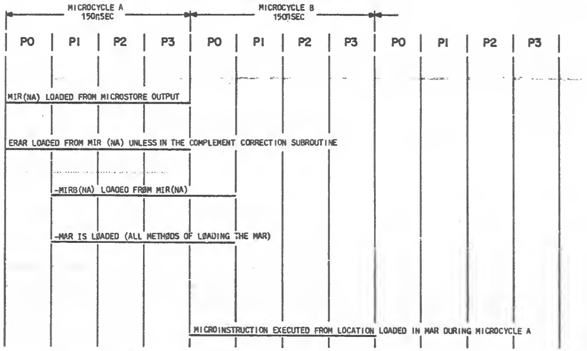
PART OF FS 1
MICROCONTROL

CIRCUIT OPERATION
(SEE SHEET B1GN,B1GP)

COMPOSITE DIAGRAM 5
MICROSTORE OUTPUT ASSIGNMENT

FUNCTION (MIR)	MICROPROGRAM STORE OUTPUT (NETNAME)
CA	MPS050
CB	MPS030
PTA	MPS010
PNA	MPS310
NA11	MPS290
NA10	MPS270
NA09	MPS250
NA08	MPS230
NA07	MPS210
NA06	MPS190
NA05	MPS170
NA04	MPS150
NA03	MPS130
NA02	MPS110
NA01	MPS090
NA00	MPS070
TO 7	MPS300
TO 6	MPS260
TO 5	MPS220
TO 4	MPS180
TO 3	MPS140
TO 2	MPS100
TO 1	MPS060
TO 0	MPS020
FROM 7	MPS280
FROM 6	MPS240
FROM 5	MPS200
FROM 4	MPS160
FROM 3	MPS120
FROM 2	MPS080
FROM 1	MPS040
FROM 0	MPS000

COMPOSITE DIAGRAM 6
BASIC TIMING OF THE MICROCONTROL REGISTERS
MIR(NA),MIRB(NA),ERAR AND THE MAR


MICROCYCLE A
150nSEC
MICROCYCLE B
150nSEC
P0
P1
P2
P3
P0
P1
P2
P3
P0
P1
P2
P3
MIR(NA) LOADED FROM MICROSTORE OUTPUT
ERAR LOADED FROM MIR (NA) UNLESS IN THE COMPLEMENT CORRECTION SUBROUTINE
-MIRB(NA) LOADED FROM MIR(NA)
-MAR IS LOADED (ALL METHODS OF LOADING THE MAR)
MICROINSTRUCTION EXECUTED FROM LOCATION LOADED IN MAR DURING MICROCYCLE A

PART OF FS 1
COMPOSITE DIAGRAM 5,6

3A CENTRAL CONTROL
DWG SIZE 6S
ISSUE 4A
BELL LABORATORIES
SD-1C900-01
B1GE

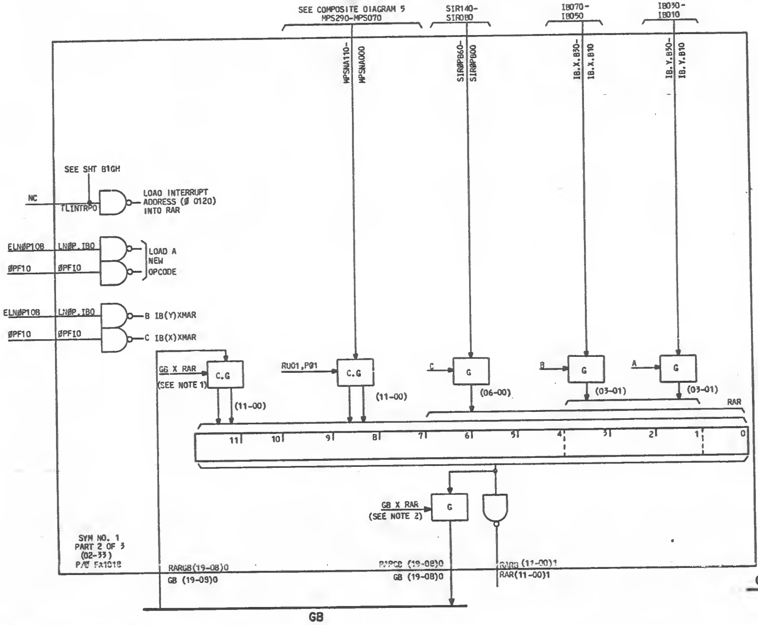
PART OF FS 1

MICROCONTROL

CIRCUIT OPERATION
(SEE SHEETS 31GN, B1GP)

COMPOSITE DIAGRAM 7

RETURN ADDRESS REGISTER

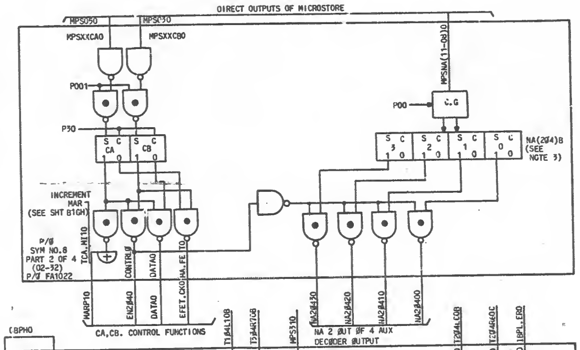


NOTES:

1. GBPHO IS GATED INTO THE RAR REGISTER FROM THE BUS TO MAINTAIN GOOD PARITY. THIS ALLOWS THE RAR TO BE LOADED WITH A MICROSUBROUTINE RETURN ADDRESS. NOTE THAT THE GATING PATH FROM THE RAR TO THE GB DOES NOT MAINTAIN PARITY.
2. THIS FLIP FLOP INHIBITS THE IB PARITY CHECK AND THE FN PARITY CHECK DURING CYCLES WHEN THE IB IS BEING LOADED OR THE FN IS BEING CLEARED.
3. THESE FOUR BITS CONTAIN THE SAME DATA THAT IS BUFFERED IN THE MIR(NA) BITS 11-8.

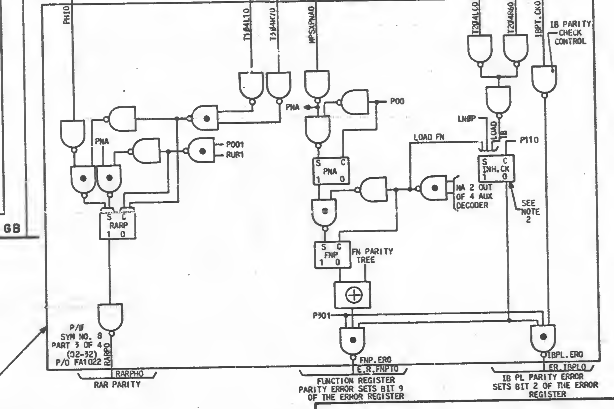
COMPOSITE DIAGRAM 8

CA,CB, DECODER AND NA FIELD AUXILIARY DECODER



COMPOSITE DIAGRAM 9

RAR PARITY, IB AND REGISTER PARITY CHECKS



3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B1GF

PART OF FS 1
COMPOSITE DIAGRAM 7,8,9

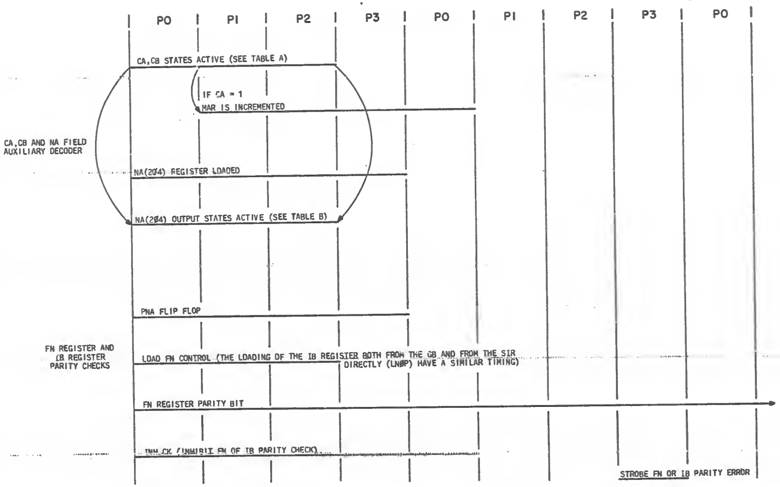
PART OF FS 1

MICROCONTROL

CIRCUIT OPERATION
(SEE SHEETS 81GN, 81GP)

COMPOSITE DIAGRAM 10

CA,CB AND NA FIELD AUXILIARY DECODER TIMING AND
FN REGISTER AND IB REGISTER PARITY CHECK TIMING



P0
P1
P2
P3
P0
P1
P2
P3
P0
CA,CB STATES ACTIVE (SEE TABLE A)
IF CA = 1
MAR IS INCREMENTED
CA,CB AND NA FIELD AUXILIARY DECODER
NA(204) REGISTER LOADED
NA(204) OUTPUT STATES ACTIVE (SEE TABLE B)
PNA FLIP FLOP
FN REGISTER AND IB REGISTER PARITY CHECKS
LOAD FN CONTROL (THE LOADING OF THE IB REGISTER BOTH FROM THE GB AND FROM THE SIR DIRECTLY (LN0P) HAVE A SIMILAR TIMING)
FN REGISTER PARITY BIT
INH CK (INHIBIT FN OF IB PARITY CHECK)
STROBE FN OR IB PARITY ERROR

COMPOSITE DIAGRAM 11

ASSIGNMENTS OF CA,CB DECODER AND THE
NA FIELD AUXILIARY DECODER

TABLE A

CA,CB	FUNCTION
00	NULL
01	MAIN MEMORY INSTRUCTION FETCH
10	MICROCONTROL DATA OPERATION
11	ENABLE NA FIELD AUXILIARY DECODER

TABLE B

NA(204) NA11	NA10	NA09	NA08	FUNCTION
0	1	1	0	LOAD THE FUNCTION REGISTER FROM MIR NA(7-1)
1	0	0	1	I/0 GB PARITY DIVERT
1	1	0	0	I/0 DML MATCH DIVERT
1	0	1	0	TURN OFF GB PARITY CHECK FOR A MICROCYCLE
0	1	0	1	SPARE
0	0	1	1	SPARE

PART OF FS 1
COMPOSITE DIAGRAM 10,11

3A CENTRAL CONTROL

②

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES

SD-1C900-01

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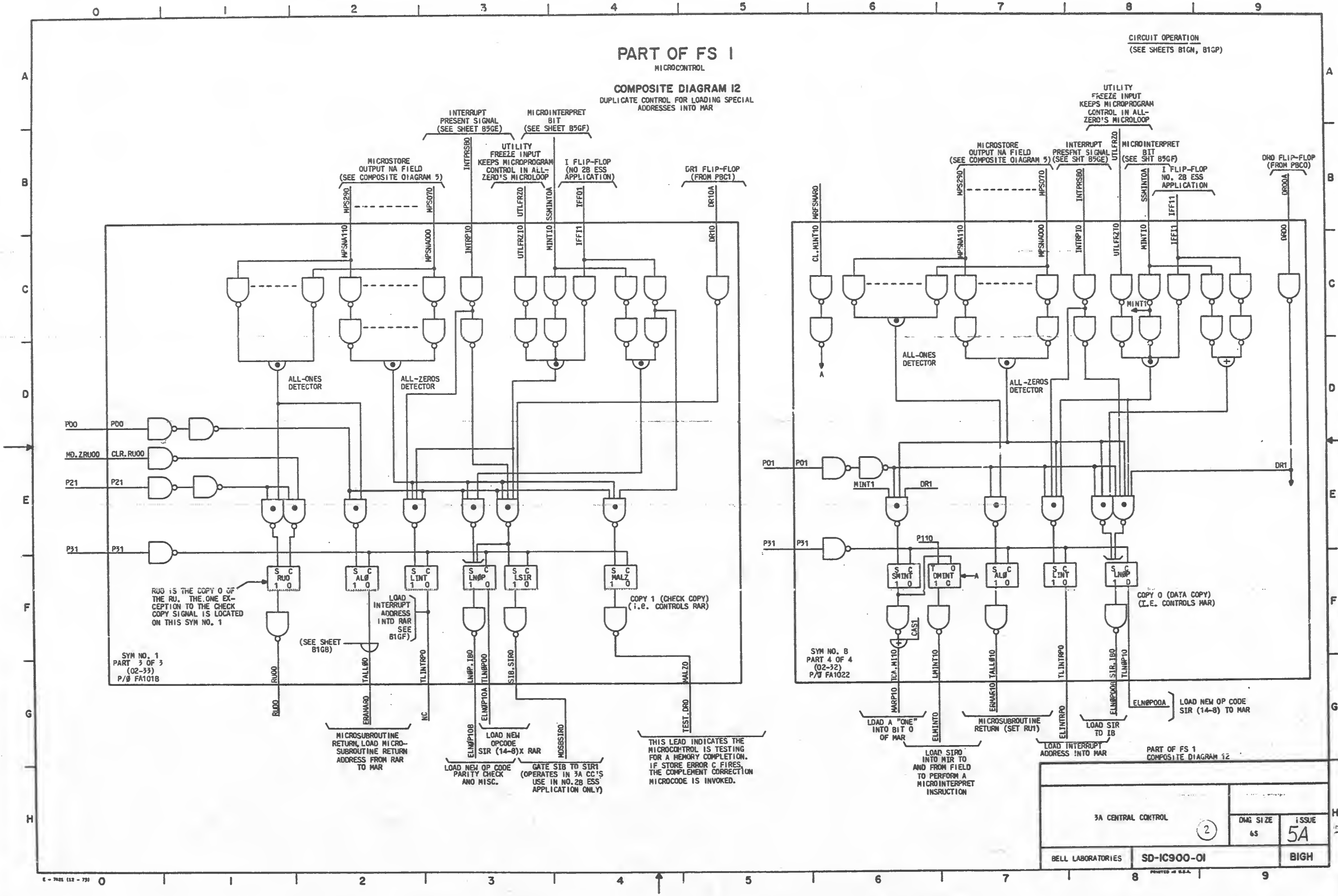
PART OF FS 1

MICROCONTROL

COMPOSITE DIAGRAM 12

DUPLICATE CONTROL FOR LOADING SPECIAL ADDRESSES INTO MAR

CIRCUIT OPERATION
(SEE SHEETS B1GN, B1GP)



0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
G
H
INTERRUPT PRESENT SIGNAL (SEE SHEET B5GE)
MICROINTERPRET BIT (SEE SHEET B5GF)
UTILITY FREEZE INPUT KEEPS MICROPROGRAM CONTROL IN ALL-ZERO'S MICROLOOP
MICROSTORE OUTPUT NA FIELD (SEE COMPOSITE DIAGRAM 5)
I FLIP-FLOP (NO 2B ESS APPLICATION)
DR1 FLIP-FLOP (FROM PBC1)
MPS290
MPS070
INTPRSB0
UTLFRZ0
SSMINT0A
IFF01
DR10A
MPSNA110
MPSNA000
INTRPI0
UTLFRZI0
MINTI0
IFFI1
DR10
ALL-ONES DETECTOR
ALL-ZEROS DETECTOR
P00
MD.ZRU00
CLR.RU00
P21
P31
S C RU0 1 0
S C ALØ 1 0
S C LINT 1 0
S C LNØP 1 0
S C LSIR 1 0
S C MALZ 1 0
RU0 IS THE COPY 0 OF THE RU. THE ONE EXCEPTION TO THE CHECK COPY SIGNAL IS LOCATED ON THIS SYM NO. 1
LOAD INTERRUPT ADDRESS INTD RAR SEE B1GF)
(SEE SHEET B1GB)
COPY 1 (CHECK COPY) (i.e. CONTROLS RAR)
SYM NO. 1 PART 3 OF 3 (02-33) P/Ø FA101B
RU00
TALLØ0
TLINTRP0
LNØP.IB0
TLNØP00
SIB.SIR0
MALZ0
ERAMAR0
NC
ELNØP10B
ELNØP10A
MOSBSIR0
TEST.DR0
MICROSUBROUTINE RETURN, LOAD MICRO-SUBROUTINE RETURN ADDRESS FROM RAR TO MAR
LOAD NEW OPCODE SIR (14-8)X RAR
LOAD NEW OP CODE PARITY CHECK AND MISC.
GATE SIB TO SIR1 (OPERATES IN 3A CC'S USE IN NO.2B ESS APPLICATION ONLY)
THIS LEAD INDICATES THE MICROCONTROL IS TESTING FOR A MEMORY COMPLETION. IF STORE ERROR C FIRES, THE COMPLEMENT CORRECTION MICROCODE IS INVOKED.
UTILITY FREEZE INPUT KEEPS MICROPROGRAM CONTROL IN ALL-ZERO'S MICROLOOP
MICROSTORE OUTPUT NA FIELD (SEE COMPOSITE DIAGRAM 5)
INTERRUPT PRESENT SIGNAL (SEE SHT B5GE)
MICROINTERPRET BIT (SEE SHT B5GF)
I FLIP-FLOP NO. 2B ESS APPLICATION
DR0 FLIP-FLOP (FROM PBC0)
MRFSMAR0
CL.MINT10
MPS290
MPS070
INTPRSB0
UTLFRZ0
SSMINT0A
IFF11
DR00A
MPSNA110
MPSNA000
INTRPI0
UTLFRZ10
MINTI0
IFFI1
DR00
MINT1
A
ALL-ONES DETECTOR
ALL-ZEROS DETECTOR
P01
MINT1
DR1
P110
P31
S C SMINT 1 0
T 0 DMINT 1 C
S C ALØ 1 0
S C LINT 1 0
S C LNØP 1 D
COPY 0 (DATA COPY) (I.E. CONTROLS MAR)
CAS1
SYM NO. B PART 4 OF 4 (02-32) P/Ø FA1022
TCA.MI10
LMINT10
TALLØ10
TLINTRP0
SIR.IB0
TLNØP10
MARP10
ELMINT0
ERMAR10
ELINTRP0
ELNØP00B
ELNØP00A
LOAD A "ONE" INTO BIT 0 OF MAR
LOAD SIR0 INTO MIR TO AND FROM FIELD TO PERFORM A MICROINTERPRET INSRUCTION
MICROSUBROUTINE RETURN (SET RU1)
LOAD INTERRUPT ADDRESS INTO MAR
LOAD SIR TO IB
LOAD NEW OP CODE SIR (14-8) TO MAR

PART OF FS 1
COMPOSITE DIAGRAM 12

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES
SD-1C900-01
B1GH

E-7021 (12-73)

PRINTED IN U.S.A.

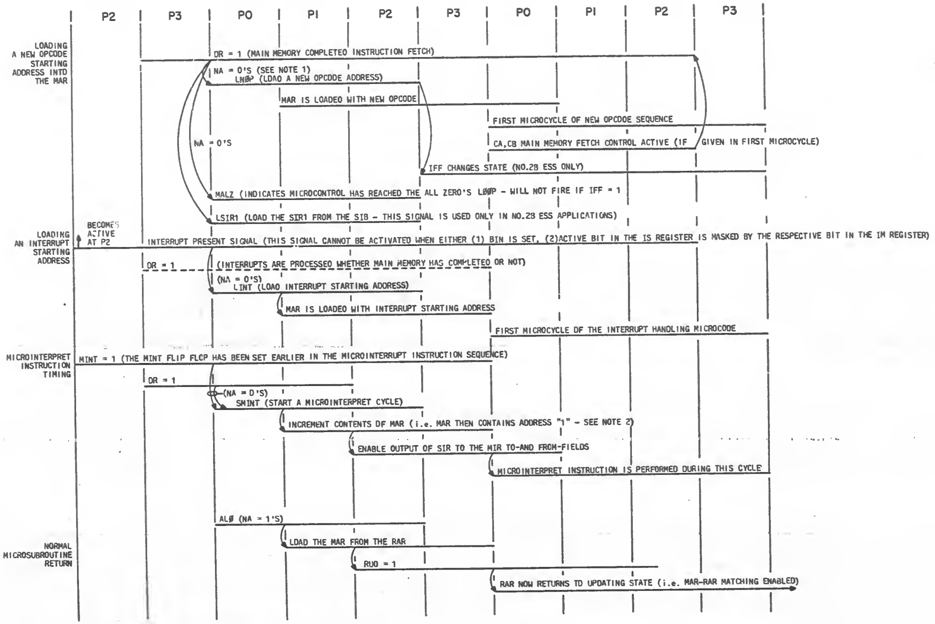
PART OF FS 1

MICROCONTROL

CIRCUIT OPERATION
(SEE SHEETS BIGN, B1GP)

COMPOSITE DIAGRAM 13

TIME DIAGRAM FOR CONTROL FUNCTIONS
THAT LOAD SPECIAL ADDRESSES IN THE MAR



P2
P3
P0
P1
P2
P3
P0
P1
P2
P3
LOADING A NEW OPCODE STARTING ADDRESS INTO THE MAR
DR = 1 (MAIN MEMORY COMPLETED INSTRUCTION FETCH)
NA = 0'S (SEE NOTE 1)
LNØP (LOAD A NEW OPCODE ADDRESS)
MAR IS LOADED WITH NEW OPCODE
FIRST MICROCYCLE OF NEW OPCODE SEQUENCE
NA = 0'S
CA,CB MAIN MEMORY FETCH CONTROL ACTIVE (IF GIVEN IN FIRST MICROCYCLE)
IFF CHANGES STATE (NO.2B ESS ONLY)
MALZ (INDICATES MICROCONTROL HAS REACHED THE ALL ZERO'S LØØP - WILL NOT FIRE IF IFF = 1
LSIR1 (LOAD THE SIR1 FROM THE SIB - THIS SIGNAL IS USED ONLY IN NO.2B ESS APPLICATIONS)
LOADING AN INTERRUPT STARTING ADDRESS
BECOMES ACTIVE AT P2
INTERRUPT PRESENT SIGNAL (THIS SIGNAL CANNOT BE ACTIVATED WHEN EITHER (1) BIN IS SET, (2)ACTIVE BIT IN THE IS REGISTER IS MASKED BY THE RESPECTIVE BIT IN THE IM REGISTER)
DR = 1
(INTERRUPTS ARE PROCESSED WHETHER MAIN MEMORY HAS COMPLETED OR NOT)
(NA = 0'S)
LINT (LOAD INTERRUPT STARTING ADDRESS)
MAR IS LOADED WITH INTERRUPT STARTING ADDRESS
FIRST MICROCYCLE OF THE INTERRUPT HANDLING MICROCODE
MICROINTERPRET INSTRUCTION TIMING
MINT = 1 (THE MINT FLIP FLOP HAS BEEN SET EARLIER IN THE MICROINTERRUPT INSTRUCTION SEQUENCE)
DR = 1
(NA = 0'S)
SMINT (START A MICROINTERPRET CYCLE)
INCREMENT CONTENTS OF MAR (i.e. MAR THEN CONTAINS ADDRESS "1" - SEE NOTE 2)
ENABLE OUTPUT OF SIR TO THE MIR TO-AND FROM-FIELDS
MICROINTERPRET INSTRUCTION IS PERFORMED DURING THIS CYCLE
NORMAL MICROSUBROUTINE RETURN
ALØ (NA = 1'S)
LOAD THE MAR FROM THE RAR
RUO = 1
RAR NOW RETURNS TO UPDATING STATE (i.e. MAR-RAR MATCHING ENABLED)

NOTES:

1. NA = 0'S ⟹ MICROPROGRAM CONTROL HAS COMPLETED THE PREVIOUS SEQUENCE OF MICROINSTRUCTIONS AND IS READY TO START ANOTHER SEQUENCE. THE MICROCONTROL WILL LOOP AT THE ALL ZEROS LOCATION IN THE MICROPROGRAM STORE IF THE STARTING ADDRESS OF THE NEXT SEQUENCE IS NOT YET AVAILABLE.

2. STARTING AT ADDRESS "1" A SEQUENCE OF MICROCODE WILL DETERMINE WHETHER THIS IS A SINGLE CYCLE MICROINTERPRET (I.E. CLEAR THE MINT FLIP FLOP) OR A MULTIPLE CYCLE MICROINTERPRET INSTRUCTION. (IF SO, THE ABOVE TIMING SEQUENCE WILL BE REPEATED WHEN THE DR = 1 AND THE NA = 0'S.)

PART OF FS 1
COMPOSITE DIAGRAM 13

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

BIGJ

E - 7421 (12 - 73)

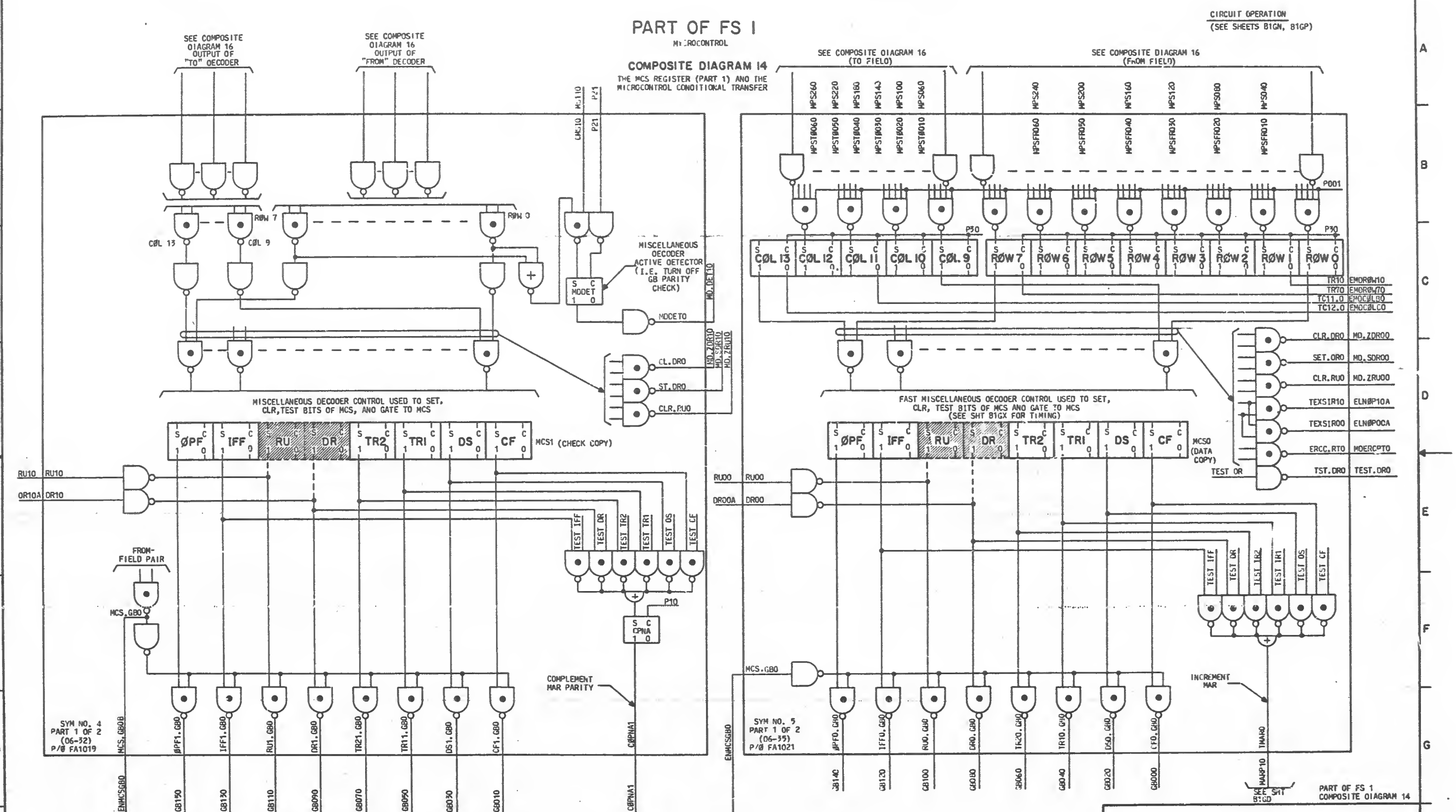
PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 14

THE MCS REGISTER (PART 1) AND THE MICROCONTROL CONDITIONAL TRANSFER

CIRCUIT OPERATION
(SEE SHEETS B1GN, B1GP)



PART OF FS 1
COMPOSITE DIAGRAM 14

3A CENTRAL CONTROL	DWG SIZE 65	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B1GK

PRINTED IN U.S.A.

E-7521 (12-73)

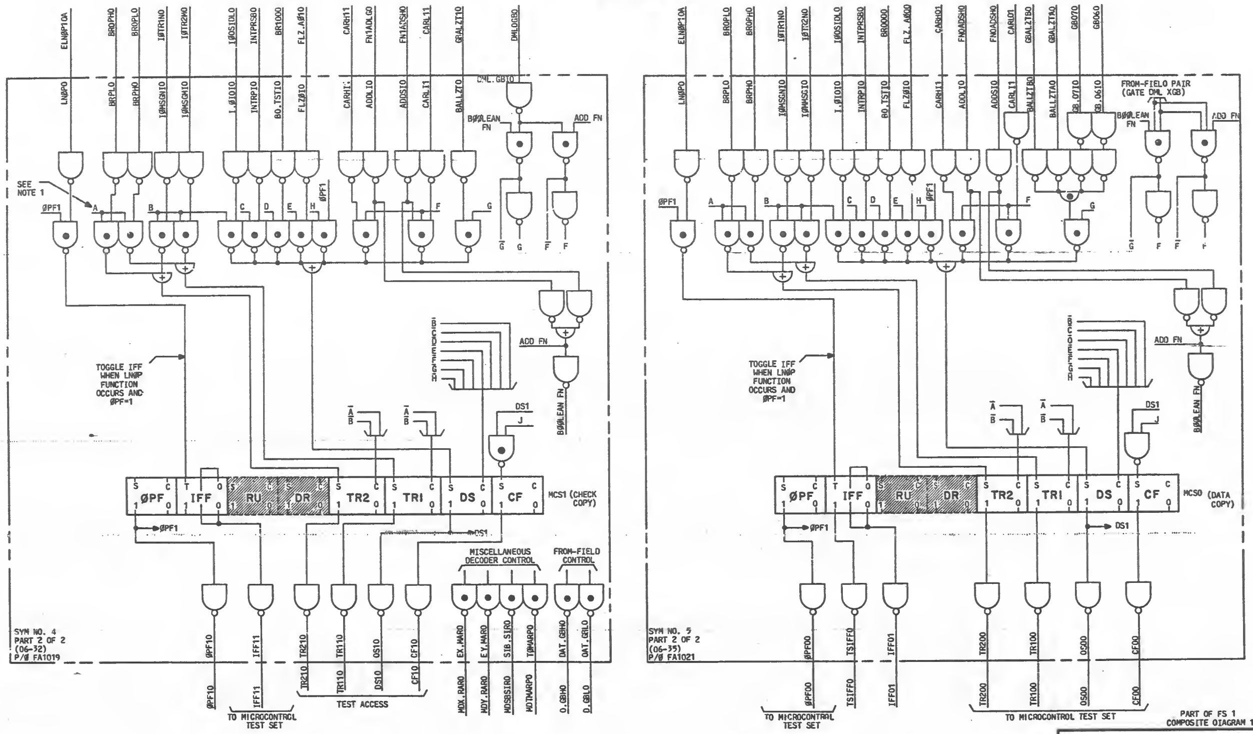
PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM I5

THE MCS REGISTER (PART 2)

CIRCUIT OPERATION
(SEE SHEETS B1GN, B1GP)



PART OF FS 1
COMPOSITE DIAGRAM 15

NOTES:

1. SEE COMPOSITE DIAGRAM 16 FOR DEFINITION OF A, B, C ETC. $\bar{A}$ IS THE COMPLEMENT OF A.

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B1GL

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PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 16

ASSIGNMENT AND CONTROL DECODING(MOSTLY MISC. DECODER)
PERFORMED ON MCS LOGIC PACKS

CIRCUIT OPERATION
(SEE SHEET BIGN,BIGP)

FUNCTION		NETNAME OF FUNCTION IF ON THE BACKPLANE		TO FIELD		FROM FIELD		MPS 4-OF-8 CODE FA1021 (06-35)																
				NETNAME (PIN NO.)		NETNAME (PIN NO.)		TO FIELD									FROM FIELD							
MNEMONIC	DESCRIPTION	COPY 1 (FA1019 06-32) PIN NO.	COPY 0 (FA1021 06-35) PIN NO.	FA1019 (06-32)				NETNAME (PIN NO.)	MPS300 (004)	MPS260 (111)	MPS220 (008)	MPS180 (207)	MPS140 (303)	MPS100 (007)	MPS060 (104)	MPS020 (204)	MPS280 (202)	MPS240 (003)	MPS200 (001)	MPS160 (100)	MPS120 (300)	MPS080 (101)	MPS040 (103)	MPS000 (203)
SOPF	SET OPF	—	—	T204L30B (316)	T204RC0C (115)	F304LD0 (011)	F104R80 (112)		0	0	1	1	1	1	0	0	1	1	0	1	1	0	0	0
ZOPF	CLEAR OPF	—	—	T204LC0B (304)	T204RC0C (115)	F304LD0 (011)	F104R80 (112)		1	1	0	0	1	1	0	0	1	1	0	1	1	0	0	0
(TOPF)	OPF CANNOT BE TESTED DIRECTLY	—	—	—		—			—				—				—				—			
SI	SET I BIT	—	—	T104L10B (214)	T304R80B (216)	F304LD0 (011)	F104R80 (112)		0	0	0	1	1	0	1	1	1	1	0	1	1	0	0	0
ZI	CLEAR I BIT	—	—	T204LC0B (304)	T204RA0B (315)	F304LD0 (011)	F104R80 (112)		1	1	0	0	1	0	1	0	1	1	0	1	1	0	0	0
TI	TEST I BIT	—	—	T204LC0B (304)	T204R90B (016)	F304LD0 (011)	F104R80 (112)		1	1	0	0	1	0	0	1	1	1	0	1	1	0	0	0
(SRU)	SET BY NA ALL-ONES DETECTOR	ERAMAR10 (OUT-PUTS FROM FA1022)	ERAMAR00 (OUT-PUTS FROM FA1018)	—		—			—				—				—				—			
ZRU	CLEAR RU	M0.ZRU10 (317)	MD.ZRU00 (308)	T104L10B (214)	T304R80B (216)	F304LE0 (310)	F104R80 (112)		0	0	0	1	1	0	1	1	1	1	1	0	1	0	0	0
(TRU)	RU CANNOT BE TESTED DIRECTLY	—	—	—		—			—				—				—				—			
SDR	SET DR	M0.SDR10 (102)	MD.SDR00 (108)	T104L10B (214)	T304R80B (216)	F204L30B (212)	F204R90B (311)		0	0	0	1	1	0	1	1	0	0	1	1	1	0	0	1
ZDR	CLEAR DR	M0.ZDR10 (302)	MD.ZDR00 (009)	T104L10B (214)	T304R80B (216)	F204L30B (212)	F204RA0B (111)		0	0	0	1	1	0	1	1	0	0	1	1	1	0	1	0
TDR	TEST DR	—	—	T204LC0B (304)	T204RC0C (115)	F304LE0 (310)	F104R80 (112)		1	1	0	0	1	1	0	0	1	1	1	0	1	0	0	0
STR1	SET TR1	—	—	T204LC0B (304)	T204RA0B (315)	F204L30B (212)	F204R90B (311)		1	1	0	0	1	0	1	0	0	0	1	1	1	0	0	1
ZTR1	CLEAR TR1	—	—	T204LC0B (304)	T204RA0B (315)	F204L30B (212)	F204RA0B (111)		1	1	0	0	1	0	1	0	0	0	1	1	1	0	1	0
TTR1	TEST TR1	—	—	T204L30B (316)	T204RC0C (115)	F204L30B (212)	F204R60C (012)		0	0	1	1	1	1	0	0	0	0	1	1	0	1	1	0
STR2	SET TR2	—	—	T204LC0B (304)	T204R90B (016)	F204L30B (212)	F204R90B (311)		1	1	0	0	1	0	0	1	0	0	1	1	1	0	0	1
ZTR2	CLEAR TR2	—	—	T204LC0B (304)	T204R90B (016)	F204L30B (212)	F204RA0B (111)		1	1	0	0	1	0	0	1	0	0	1	1	1	0	1	0
TTR2	TEST TR2	—	—	T204L30B (316)	T204RC0C (115)	F304LE0 (310)	F104R80 (112)		0	0	1	1	1	1	0	0	1	1	1	0	1	0	0	0
SDS	SET DS	—	—	T204LC0B (304)	T204RC0C (115)	F204L30B (212)	F204R90B (311)		1	1	0	0	1	1	0	0	0	0	1	1	1	0	0	1
ZDS	CLEAR DS	—	—	T204LC0B (304)	T204RC0C (115)	F204L30B (212)	F204RA0B (111)		1	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
TDS	TEST DS	—	—	T204LC0B (304)	T204RA0B (315)	F204L30B (212)	F204R60C (012)		1	1	0	0	1	0	1	0	0	0	1	1	0	1	1	0
SCF	SET CF	—	—	T204L30B (316)	T204RC0C (115)	F204L30B (212)	F204R90B (311)		0	0	1	1	1	1	0	0	0	0	1	1	1	0	0	1
ZCF	CLEAR CF	—	—	T204L30B (316)	T204RC0C (115)	F204L30B (212)	F204RA0B (111)		0	0	1	1	1	1	0	0	0	0	1	1	1	0	1	0
TCF	TEST CF	—	—	T204LC0B (304)	T204R90B (016)	F204L30B (212)	F204R60C (012)		1	1	0	0	1	0	0	1	0	0	1	1	0	1	1	0
DS=>CF [J]	GATE DS TO CF	—	—	T204LC0B (304)	T204RC0C (115)	F204L30B (212)	F204R60C (012)		1	1	0	0	1	1	0	0	0	0	1	1	0	1	1	0
OPF=>DS [H]	GATE OPF TO DS	—	—	T204L30B (316)	T204RC0C (115)	F204LC0B (116)	F204R90B (311)		0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	1
TPAR [A]	TEST PARITY BIT IN BR	—	—	T204LC0B (304)	T204RA0B (315)	F204L30B (212)	F204RC0C (211)		1	1	0	0	1	0	1	0	0	0	1	1	1	1	0	0
TCH [B]	TEST I/O CHANNEL	MD.TCH0 (100)	—	T104L10B (214)	T304R80B (216)	F204L30B (212)	F204RC0C (211)		0	0	0	1	1	0	1	1	0	0	1	1	1	1	0	0
TINT [C]	TEST FOR INTERRUPTS	—	—	T204LC0B (304)	T204RC0C (115)	F204L30B (212)	F204RC0C (211)		1	1	0	0	1	1	0	0	0	0	1	1	1	1	0	0
TBR0 [D]	TEST BIT 0 OF BR	—	—	T204L30B (316)	T204RC0C (115)	F204L30B (212)	F204RC0C (211)		0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
TFLZ [E]	TEST FOR LOW ZERO IN AR	MDFLZT10 (118)	MDFLZT00 (113)	T104L10B (214)	T304R80B (216)	F204L30B (212)	F204R60C (012)		0	0	0	1	1	0	1	1	0	0	1	1	0	1	1	0
ERAR=>MAR	PERFORM AN ERROR MICROSUBROUTINE RETURN BY GATING ERAR=>MAR	—	—	T204LC0B (304)	T204R90B (016)	F204LC0B (116)	F204RA0B (111)		1	1	0	0	1	0	0	1	1	1	0	0	1	0	1	0
TY	—	MDY.RAR0 (318)	—	T204LC0B (304)	T204RA0B (315)	F304LE0 (310)	F104R80 (112)		1	1	0	0	1	0	1	0	1	1	1	0	1	0	0	0
TX	—	MDX.RAR0 (117)	—	T204LC0B (304)	T204R90B (016)	F304LE0 (310)	F104R80 (112)		1	1	0	0	1	0	0	1	1	1	1	0	1	0	0	0
SIB=>SIR1	—	MDSBSIR0 (217)	—	T204LC0B (304)	T204R90B (016)	F204L30B (212)	F204RC0C (211)		1	1	0	0	1	0	0	1	0	0	1	1	1	1	0	0
TMARP	—	MDTMARP0 (017)	—	T204LC0B (304)	T204R90B (016)	F204LC0B (116)	F204R90B (311)		1	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1
MCS=>GB	—	ENMCSGB0 (004)	—	—		F104L70 (309)	F304R40 (210)		—				—				0	1	1	1	0	1	0	0
MIRH12=>GB	—	0.GBH0 (019)	—	—		F304LE0 (310)	F104R10 (110)		—				—				1	1	1	0	0	0	0	1
MIRL8=>GB	—	0.GBL0 (219)	—	—		F304LE0 (310)	F304R40 (210)		—				—				1	1	1	0	0	1	0	0
DML=>GB [F+G]	—	—	—	—		DMLOGB0 (207)			—				—				1	0	1	1	0	1	0	0
EXEC	LOADS A NEW OP CODE WITH SERVICING INTERRUPTS	—	ELNOP00A (208) ELNOP10A (209)	T104L10B (214) T104L10B (214)	T304R80B (216) T304R80B (216)	F204LC0B (116) F204LC0B (116)	F204R90B (311) F204R90B (311)		0 0	0 0	0 0	1 1	1 1	0 0	1 1	1 1	1 1	1 1	0 0	0 0	1 1	0 0	0 0	1 1

PART OF FS 1
COMPOSITE DIAGRAM 16

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	DWG SIZE 6S
		ISSUE 5A
		BIGM

PART OF FS 1

MICROCONTROL

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2-16

CIRCUIT OPERATION

NORMAL ADDRESS SEQUENCING

COMPOSITE DIAGRAM 2 AND 4 DETAIL THE ADDRESS SEQUENCING AND THE ASSOCIATED ADDRESS MATCH CHECK LOGIC OF THE MIR (NA), THE MAR, AND THE RAR. IN EVERY MICROCYCLE THE CONTENTS OF THE NA FIELD OF THE MICROPROGRAM STORE OUTPUT ARE GATED INTO THE MIR(NA) BY CLOCK PHASE P0 (SEE COMPOSITE DIAGRAM 2). IF THE RU0 FLIP-FLOP IS SET, THIS SAME ADDRESS FIELD IS GATED TO THE RAR REGISTER. AT CLOCK PHASE P1, THE MIR(NA) IS GATED TO THE MAR OF THE CLOCK SIGNALS (I.E., P110(S1) AND P110(S2)) AND ARE NOT INHIBITED BY THE CA BIT CONTROL OR THE FREEZE FUNCTION. ONCE THE ADDRESS IS IN THE MAR, IT OUTPUTS DIRECTLY TO THE MICROPROGRAM STORE WHERE IT IS USED TO ACCESS THE NEXT WORD TO BE EXECUTED. IN ADDITION, THE OUTPUT OF THE MAR IS INPUTTED TO THE MAR-RAR MATCHER TOGETHER WITH THE OUTPUT OF THE RAR. NOTE THAT THE MATCHER CHECKS FOR ONLY BITS 1-11 OF THE ADDRESS. BIT 0 IS VERIFIED BY THE MAR PARITY CHECKS (SEE BIGT). THE OUTPUT OF THE MATCHER IS STROBED BY CLOCK PHASE P3 UNLESS THE RU1 FLIP-FLOP IS CLEARED. NOTE THAT RU0 AND RU1 ARE JUST DUPLICATED COPIES OF THE SAME FUNCTION. THEREFORE, WHEN RU0 IS CLEARED, THE RAR IS NOT BEING UPDATED WITH AN ADDRESS FROM THE MICROPROGRAM STORE OUTPUT AND HENCE THE MATCHER MUST BE DISABLED.

THE TYPICAL AND MOST FREQUENT METHOD OF OBTAINING THE NEXT ADDRESS TO LOAD INTO THE MAR IS VIA THE MIR(NA) REGISTER. ANOTHER COMMON METHOD IS TO USE THE PREVIOUS ADDRESS IN THE MAR AND INCREMENT IT BY ONE. THIS METHOD IS SIMPLIFIED BY FORCING ALL INSTANCES THAT USE THIS TECHNIQUE TO BE LOCATED IN A MICROPROGRAM STORE LOCATION THAT HAS AN EVEN ADDRESS. IN THIS MANNER, TO INCREMENT THE OLD ADDRESS, A ONE NEED ONLY BE JAMMED INTO BIT POSITION ZERO WHICH WILL CONTAIN A ZERO BY DEFINITION. THE MECHANISM TO SAVE THE PREVIOUS CONTENTS OF THE MAR AND THEN TO INCREMENT OR ADD ONE TO IT IS VIA THE CA CONTROL BIT. WHEN THE CA SIGNAL IS READ OUT OF THE MICROPROGRAM STORE AND IT IS ACTIVE, THE CA FLIP-FLOP IS SET (SEE COMPOSITE DIAGRAM 2). THIS CELL INHIBITS THE P1 CLOCK PHASE THAT IS USED TO GATE THE MIR(NA) TO THE MAR. AS A RESULT, THE CONTENTS OF THE BITS (1-11) OF THE MAR ARE PRESERVED. THE CA BIT IS THEN USED TO JAM THE ONE BIT ZERO OF THE MAR. A VERY IMPORTANT CHARACTERISTIC ABOUT THE P1 GATING OF THE MIR(NA) TO THE MAR WHICH THE CA BIT IS ABLE TO CONTROL, IS THAT FOR NORMAL ADDRESSING SEQUENCING, THIS GATING PATH IS ALWAYS ENABLED EXCEPT FOR CASES WHERE THE CA BIT IS SET. AS WILL BE DESCRIBED LATER IN THIS SECTION, THIS FEATURE HAS A NUMBER OF ADVANTAGES.

MICROSUBROUTINES (AND THE CA BIT)

WHEN THE NEXT ADDRESS FOR THE MAR DOES NOT HAVE TO BE PROVIDED FROM THE NA FIELD OF THE MICROPROGRAM STORE, A NUMBER OF OTHER USES ARE MADE OF THE DATA FIELD. ONE USE OF THE NA FIELD IS TO LOAD THE RAR REGISTER WITH AN ARBITRARY RETURN ADDRESS FOR MICROSUBROUTINES. THE LOADING OF THE RAR IS PERFORMED IF A NORMAL ADDRESS SEQUENCING CYCLE IS TAKING PLACE. WHEN THE DATA IS IN THE RAR, THE RU FLIP-FLOP IS CLEARED BY A MISCELLANEOUS DECODER CROSSPOINT. WHEN THE RU IS CLEARED, THE RETURN ADDRESS IS SAVED IN THE RAR AND THE RU BEING CLEARED DISABLES THE MAR-RAR MATCHER FOR THE DURATION OF THE MICROSUBROUTINE. THE STARTING ADDRESS OF THE MICROSUBROUTINE IS THEREFORE THE CONTENTS OF THE MAR+1 AT WHICH THE RETURN ADDRESS HAS BEEN STORED. FOR EXAMPLE, IF X IS THE LOCATION IN THE MICROPROGRAM STORE WHERE THE RETURN ADDRESS Y IS LOCATED, THEN X WOULD HAVE TO BE AN EVEN ADDRESS AND THE STARTING ADDRESS OF THE MICROSUBROUTINE WOULD BE X+1. NOTE THAT LOCATION X WOULD ALSO CONTAIN A MISCELLANEOUS DECODER THAT WOULD CLEAR THE RU FLIP-FLOP.

WHEN THE MICROSUBROUTINE IS TO BE EXITED, ALL ONES ARE PLACED IN THE NA FIELD OF THE LAST WORD OF THE MICROSUBROUTINE. THIS ADDRESS CONSTANT IS A UNIQUE ONE AND A HARDWARE DETECTOR CALLED THE ALL-ONES DETECTOR IS USED TO DETECT ITS PRESENCE. WHEN THE ALL-ONES DETECTOR FIRES, IT LOADS THE CONTENTS OF THE RAR TO THE MAR. IT PERFORMS THIS LOAD FUNCTION BY INHIBITING THE GATING OF THE INDIVIDUAL ONES FLOWING FROM THE MIR(NA) TO THE MAR. AS WAS POINTED OUT, THE MIR(NA) TO MAR IS ALWAYS ENABLED DURING CLOCK PHASE P1 UNLESS THE CA BIT IS SET. IF AN ERROR OCCURS IN THE NA FIELD ALL-ONES DETECTOR, THE ALL-ONES CONSTANT WILL END UP IN MAR AND SINCE THIS LOCATION IN THE MICROPROGRAM STORE CONTAINS INVALID CONTENTS, A CHECK CIRCUIT WILL FIRE (I.E., TO AND FROM DECODER CHECKER WILL INDICATE AN ERROR). THE ACTIVATION OF THE ALL-ONES DETECTOR ALSO RESULTS IN THE SETTING OF THE RU FLIP-FLOP SO THAT THE RAR RETURNS TO BEING UPDATED ON EVERY MICROCYCLE WITH THE NA FIELD FROM THE MICROPROGRAM STORE. AS A RESULT, THE MAR-RAR MATCHER IS RE-ENABLED. AS INDICATED IN COMPOSITE DIAGRAM 2, THE RU, AS WELL AS THE ALL-ONES DETECTOR THAT SET IT, IS DUPLICATED TO PROVIDE ERROR DETECTION ON THIS CIRCUITRY. THE USE OF THE RUB FLIP-FLOP SHOWN IN SYMBOL NO. 3 IS TO PROVIDE THE NECESSARY TIMING ON THE SETTING OR CLEARING OF RU1 TO GUARANTEE A VALID MATCH WHEN ENTERING OR EXITING A MICROSUBROUTINE.

CIRCUIT OPERATION (CONT)

FOR THE CASE WHERE THE CA=1 AND A MICROSUBROUTINE IS NOT ENTERED, THE MAR-RAR MATCHER WOULD FIRE INDICATING AN ERROR SINCE THE MAR CONTAINS THE OLD MAR CONTENTS PLUS ONE AND THE RAR CAN CONTAIN AN ARBITRARY DATA CONSTANT. THEREFORE THE CA BIT ITSELF MUST INHIBIT THE MAR-RAR MATCHER FOR THE SINGLE MICROCYCLE DURING WHICH THE CA BIT IS ACTIVE.

AUXILIARY CONTROL

THE NA FIELD ALSO GENERATES SOME ADDITIONAL OR AUXILIARY CONTROL FUNCTIONS. THESE CONTROL FUNCTIONS PROVIDE SOME ADDITIONAL FEATURES TO MICROPROGRAM CONTROL BY PROVIDING SIMULTANEOUS CONTROL FUNCTIONS WITH THE NORMAL TO- AND FROM-FIELD CONTROL SOURCES. THE MOST FREQUENTLY USED OF THESE FEATURES IS THE ABILITY TO LOAD THE FUNCTION (FN) REGISTER IN THE DML LOGIC SIMULTANEOUSLY WITH A NORMAL REGISTER-TO-REGISTER GATING OPERATION.

DATA

ANOTHER COMMON USE OF THE NA FIELD IS TO PROVIDE DATA CONSTANTS. THE DATA IS GATED THROUGH THE MIR(NA) REGISTER TO THE MIRB(NA). THE LATTER REGISTER IS USED TO PROVIDE BUFFERING OF THE DATA FOR ONE CLOCK PHASE LONGER THAN IT WOULD BE IF BUFFERED BY THE MIR(NA) ONLY. THE DATA FIELD HAS A MAXIMUM OF 12 BITS IN WIDTH AND CAN BE GATED ONTO THE LOW 8 BITS OF THE GB OR THE UPPER 12 BITS (8-19). THE PARITY FOR THE DATA FIELD IS PROVIDED BY THE PNA BIT WITH A ONE JAMMED INTO THE PARITY FIELD THAT CONTAINS ZEROS. FOR EXAMPLE, IF THE DATA IS GATED ONTO THE LOW 8 BITS OF THE GB, THE PL BIT=PNA AND THE PH BIT=1. TO PROVIDE A 16- OR 20-BIT DATA CONSTANT, TWO DATA OPERATIONS ARE REQUIRED AND THE RESLUTS ARE PIECED TOGETHER IN THE DML LOGIC. NOTE THAT DATA CONSTANTS CAN ONLY BE FORMED IN EVEN ADDRESS LOCATION BECAUSE OF THE OPERATION OF THE CA CONTROL BIT TO OBTAIN THE ADDRESS OF THE MICROINSTRUCTION FOLLOWING THE DATA CONSTANT.

THE AUXILIARY DECODER IS ATTACHED TO THE UPPER FOUR BITS OF THE NA FIELD (BITS 8-11, SEE COMPOSITE DIAGRAM 8) AND ITS SIX POSSIBLE CONTROL STATES ARE DEFINED IN TABLE B, SHEET B1GG. NOTE THAT THE AUXILIARY DECODER IS ENABLED BY ONE OF THE STATES OF THE CA,CB DECODER. AS SHOWN IN COMPOSITE DIAGRAM 4, THE FN IS THEN LOADED FROM BITS 1-7 OF THE NA FIELD OF THE MIR(NA) DURING AN AUXILIARY CONTROL MICROCYCLE. THE GATING PATH FROM THE MIRB(NA) TO THE FN REGISTER IS PERFORMED OVER A DEDICATED PATH (I.E., ONLY ONE SOURCE REGISTER AND ONLY ONE DESTINATION REGISTER) AND AS A RESULT THE GATING PATH NEED ONLY BE ENABLED AT ONE POINT. THE ENABLING IS PERFORMED WITHIN THE DML FOR THIS OPERATION. THE ARRIVAL OF THE DATA IN THE FN REGISTER IS CHECKED BY A PARITY CHECK BIT. THE PARITY FOR DATA FIELD IS PROVIDED BY THE PNA BIT AND THIS PNA BIT IS LOADED INTO A BUFFER FLIP-FLOP WHEN THE FN IS LOADED (SEE COMPOSITE DIAGRAM 17) AND THE OUTPUT OF THIS PARITY TREE IS CHECKED AGAINST THE FN PARITY BIT.

AN ANOMOLY OF THE FN PARITY CHECK IS THAT BIT ZERO OF THE FN REGISTER IS NOT EQUIPPED. THEREFORE, BIT 0 OF THE MIRN(NA) IS NOT USED FOR THE FN. IN ADDITION, BIT 0 OF THE PARITY TREE IS TIED TO GROUND (SEE COMPOSITE DIAGRAM 17) AND HENCE AS FAR AS THE PARITY TREE IS CONCERNED, BIT 0 IS A ONE. THEREFORE, INSTEAD OF THE NORMAL ODD PARITY, THE PNA BIT THAT COVERS THE NA FIELD FOR THE LOADING OF THE FN REGISTER IS REQUIRED TO GENERATE EVEN PARITY SO THAT THE FN REGISTER PARITY CHECK WILL GIVE CORRECT RESULTS. NOTE THAT BITS 8-11 OF THE NA FIELD FOR AUXILIARY CONTROL CONTAIN A 2-OUT-OF-4 CODE AND HENCE DO NOT EFFECT THE PARITY FIELD WHEN LOADING THE LOW BITS OF THE NA FIELD INTO THE FN REGISTER.

FOR MAINTENANCE PURPOSES ONLY THE RAR CAN BE LOADED OVER THE GATING PATH FROM THE OUTPUT OF THE MIRB(NA) TO THE FN REGISTER. AS SHOWN IN COMPOSITE DIAGRAM 4 AND ON SHEET B2GB, THE MISCELLANEOUS DECODER THAT ENABLES THIS MAINTENANCE PATH MUST ENABLE BOTH THE RAR TO THE GATING PATH AND THE GATING PATH INTO THE FN REGISTER.

CONDITIONAL BRANCHES

AS DESCRIBED IN DETAIL IN THE SECTION OF THE MICROPROGRAM CONTROL STATUS (MCS) REGISTER (SEE SHEET B1GK), THE KEY STATUS INFORMATION BITS FOR THE MICROPROGRAM CONTROL ARE MAINTAINED IN THE MCS REGISTER. THE ABILITY TO CONDITIONAL BRANCH ON THESE BITS IS PROVIDED. THE CONDITIONAL BRANCH LOGIC IS IMPLEMENTED IN A VERY SIMILAR MANNER AS THE CA BIT LOGIC THAT INCREMENTS THE MAR. THAT IS, CONDITIONAL BRANCHES MUST OCCUR ON EVEN WORD BOUNDARIES AND THE CONDITIONAL BRANCH GATES THE MCS BIT THAT IS BEING TESTED INTO BIT 0 OF THE MAR. THUS, IF A CONDITIONAL BRANCH IS LOCATED AT LOCATION Y, Y MUST CONTAIN AN EVEN ADDRESS X IN ITS NA FIELD. THE CONDITIONAL BRANCH WILL THEN GO TO X+1 IF THE MCS BIT IS A ONE OR TO X IF THE MCS BIT IS ZERO. THE CONDITIONAL BRANCH RESULTS IN A MISCELLANEOUS DECODER CROSSPOINT ENABLING THE SELECTED MCS BIT ONTO A COMMON CONTROL SIGNAL (SEE COMPOSITE DIAGRAM 14). IF THIS CONTROL SIGNAL IS ACTIVE, IT IS GATED INTO THE MAR (SEE COMPOSITE DIAGRAM 4) AT CLOCK PHASE P1.

CIRCUIT OPERATION (CONT)

INDEXING

THE ABILITY TO GATE THE X OR Y FIELDS OF THE IB REGISTER DIRECTLY INTO THE MAR BITS 0-3 IS PROVIDED. THIS GATING OPERATION "OR"S THE CONTENTS OF THE RESPECTIVE X OR Y FIELD WITH THE CONTENTS OF THE MIR(NA) REGISTER INTO THE MAR AT CLOCK PHASE P1. THEREFORE, TABLES IN THE MICROPROGRAM STORE MUST BEGIN ON 16-, 8-, 4-, OR 2-WORD BOUNDARIES IF THE INDEX COMMAND IS TO BE USED IN OTHER WORDS, A 16-WORD TABLE WOULD BE STARTED AT LOCATION X, WHERE X WOULD HAVE ZEROS IN THE LOW FOUR BITS OF ITS ADDRESS. THE FINAL STAGE OF DECODING FOR THE "FAST" MISCELLANEOUS DECODER CONTROL SIGNALS THAT GATE THE X AND Y FIELDS INTO THE MAR IS LOCATED ON THE CIRCUIT PACK THAT CONTAINS THE MAR (SEE COMPOSITE DIAGRAM 4).

LOADING A NEW OP CODE (NO. 3A CC INSTRUCTIONS)

EACH MACROLEVEL INSTRUCTION IS PERFORMED BY LOADING THE OP CODE (OPERATION CODE) FOR THAT INSTRUCTION FETCHED FROM THE MAIN STORE (SEE FS 4) INTO THE MAR. THEN A SEQUENCE OF MICROINSTRUCTIONS WILL FOLLOW THAT WILL INTERPRET OR EXECUTE THAT OP CODE. AT THE TERMINATION OF THE SEQUENCE OF MICROINSTRUCTION ALL-ZEROS IS PLACED IN THE NA FIELD. AN ALL-ZEROS DETECTOR IS THEN USED TO DETECT THIS ADDRESS CONSTANT. IF THIS DETECTOR IS ACTIVE AND THE SIR REGISTER CONTAINS THE NEXT OP CODE TO BE EXECUTED, THE OP CODE FIELD FROM THE SIR IS LOADED INTO THE MAR. THE PRESENCE OF THE OP CODE IN THE SIR IS SIGNIFIED BY THE DR (DATA READY)=1. IF THE DR=0, THE OP CODE FIELD OF THE SIR IS NOT LOADED ONTO THE MAR. INSTEAD, THE NORMAL GATING FROM THE MIR(NA) TO THE MAR RESULTS IN ALL-ZEROS BEING PLACED IS THE MAR FOR THE NEXT ADDRESS. AT THE ALL ZERO'S LOCATION, ALL ZERO'S ARE IN THE NA FIELD. THE RESULT IS THAT THE MICROPROGRAM CONTROL WILL LOOP AT THE ALL-ZERO'S LOCATION UNTIL THE DR=1.

IF THE DR=1 AND THE ALL-ZERO'S DETECTOR FIRES THE LNØP (LOAD NEW OP CODE) FLIP-FLOP WILL BE ACTIVATED (SEE COMPOSITE DIAGRAM 12). IT IS THE OUTPUT OF THIS LNØP FLIP-FLOP THAT LOADS THE OP CODE FIELD OF THE SIR INTO THE MAR. IT ALSO LOADS THE SIR INTO THE IB REGISTER AND THE OP CODE FIELD INTO THE RAR.

FOR TESTING PURPOSES, IT IS POSSIBLE TO STOP THE INSTRUCTION PROCESSING WITHIN A 3A CC. THIS FUNCTION IS PERFORMED BY THE UTILITY-FREEZE FUNCTION THAT IN ESSENCE INHIBITS THE ALL-ZERO'S DETECTOR AND HENCE HOLDS THE MICROPROGRAM CONTROL IN THE ALL-ZERO'S LOOP. CAUTION MUST BE EXERCISED IN USING THIS FUNCTION BECAUSE THE PROGRAM TIMER WILL TIME OUT IF NOT INHIBITED OR THE REAL TIME CAPABILITY OF THE SYSTEM WILL BE ADVERSELY EFFECTED.

THE OP CODE FIELD IN THE SIR REGISTER IS 7 BITS IN WIDTH (BITS 8-15) AND, AS SUCH, PROVIDES THE ABILITY TO GENERATE 128 DISTINCT OP CODE ENTRY POINTS. THE OP CODE ENTRY POINTS ARE ORIGINATED AT LOCATION 256 IN THE MICROPROGRAM STORE AND THIS IS IMPLEMENTED BY JAMMING A ONE INTO BIT POSITION 8 OF THE MAR SIMULTANEOUSLY WITH THE LOADING OF THE OP CODE FIELD INTO BITS 0-6 OF THE MAR.

LOADING A NEW OP CODE (NO. 2B INSTRUCTIONS)

IN THE NO. 2B ESS APPLICATION, THE MAIN STORE IS 24 DATA BITS WIDE INSTEAD OF THE NORMAL 16 (SEE FS 11). THIS EXTRA WIDTH IS USED TO ACCOMODATE THE HALF WORD COMMAND STRUCTURE OF THE NO. 2 ESS PROGRAMMING LANGUAGE. WHEN THE 3A CC IS EMULATING THE NO. 2 ESS COMMANDS, A BIT CALLED THE OP CODE FIL (OPF) BIT IS ACTIVATED. THIS BIT DEFINES THE 3A CC TO BE IN THE NO. 2 EMULATION MODE AND, AS SUCH, A NUMBER OF SPECIAL FUNCTIONS ARE PERFORMED TO AID IN THE EMULATION. IN THIS MODE OF OPERATION THE MAR IS LOADED FROM ONE OF TWO SIR'S, SIR0 (THE NORMAL ONE), AND SIR1 (ADDED FOR 2B). THE DECISION AS TO WHICH ONE THE OPCODE IS LOADED FROM IS MADE BY THE IFF (SEE MCS REGISTER, COMPOSITE DIAGRAM 14). THE FUNCTION OF THE IFF IS TO "OR" THE SELECTED SIR ON TO A COMMON OUTPUT WHICH INPUTS TO THE MAR. THEN THE LNØP FUNCTION LOADS THE SIR OPCODE FIELD INTO THE MAR AT THE APPROPRIATE TIME. NOTE THAT IN THE LNØP FUNCTION THAT LOADS THE MAR, THERE IS NO DISTINCTION BETWEEN SIR0 OR SIR1. THERE ARE HOWEVER, A NUMBER OF UNIQUE FUNCTIONS THAT TAKE PLACE AS A RESULT OF THE LNØP FUNCTION, THE ØPF=1, AND STATE OF THE IFF.

(1) IF THE IFF=0, THE LNØP SIGNAL GATES THE SIB TO SIR1 (SEE SHEET B11GA). THIS IS PERFORMED VIA THE LSIR FLIP-FLOP (SEE COMPOSITE DIAGRAM 12).

(2) AS THE LNØP FUNCTION IS DEACTIVATED (I.E. TRAILING EDGE) THE IFF IS TOGGLED IF THE OPCODE FIL BIT (OPF) IS SET (SEE MCS REGISTER).

(3) IF THE IFF=1 AND HENCE THE NEXT OPCODE TO BE EXECUTED ORIGINATES FROM SIR1, THEN AN IFETCH IS NOT ISSUED TO THE MAIN STORE (MAS).

CIRCUIT OPERATION (CONT)

(4) WHEN THE OP CODE IS LOADED INTO THE MAR AND THE OPF=1, A ONE IS JAMMED INTO BIT 11 OF THE MAR INSTEAD OF BIT 8 AS IS THE CASE FOR THE NORMAL LNØP FUNCTION. THE RESULT IS THAT THE NO. 2B ESS APPLICATION HAS 128 OP CODE ENTRY POINTS STARTING AT ADDRESS 2048 IN THE MICROPROGRAM STORE.

ALL-ZERO'S DETECTOR (INTERRUPT SERVING)

THE ALL-ZERO CONSTANT IS PLACED AT THE END OF ALL MACROLEVEL INSTRUCTIONS. AT THE END OF AN INSTRUCTION, THE 3A CC IS NORMALLY ABLE TO SERVICE INTERRUPTS. IF THE SYSTEM SOFTWARE IS NOT IN A STATE TO ACCEPT INTERRUPTS, IT SETS THE BIN FLIP-FLOP (SEE SHEET B5G). IF INTERRUPTS HAVE NOT BEEN BLOCKED BY BIN, THE INTERRUPT PRESENT SIGNAL (NET INTPRS60) WILL BE ACTIVE IF AN INTERRUPT IS WAITING TO BE SERVICED. WHEN THE INTERRUPT PRESENT SIGNAL IS ACTIVE, IT INHIBITS THE LOADING OF A NEW OP CODE FROM SIR0 AND INSTEAD OF PERFORMING THAT OP CODE, THE INTERRUPT IS SERVICED. FOR THE NO. 2B ESS APPLICATION, INTERRUPTS ARE NOT SERVICED BETWEEN HALF-WORD COMMANDS. THEREFORE, IF THE IFF=1, THE INTERRUPT PRESENT SIGNAL DOES NOT BLOCK THE LOADING OF THE OP CODE FROM SIR1. AT THE END OF THE OP CODE OBTAINED FROM SIR1, HOWEVER, THE INTERRUPT IS IMMEDIATELY SERVICED.

INTERRUPTS ARE SERVICED BY THE LOADING OF A SPECIAL HARDWIRED ADDRESS INTO THE MAR. THIS ADDRESS IS GATED INTO THE MAR BY ACTIVATION OF THE LINT FLIP-FLOP SHOWN IN COMPOSITE DIAGRAM 12. THE OUTPUT OF THE LINT BIT IS THEN USED TO LOAD THE STARTING ADDRESS OF A SEQUENCE OF MICROCODE THAT WILL PERFORM THE INTERRUPT SERVICING. THIS ADDRESS IS Ø(0120) AND IT IS "OR"ED INTO THE MAR WITH THE CONTENTS OF THE MIR(NA) REGISTER WHICH WILL CONTAIN ALL ZERO'S.

COMPLEMENT CORRECTION MICROSUBROUTINE

AS DETAILED IN SHEET D11 AND D12, AN ABILITY TO JAM THE MAR TO A STARTING ADDRESS OF A MICROSUBROUTINE TO PERFORM A COMPLEMENT CORRECTION FUNCTION IS PROVIDED. WHEN THIS FUNCTION IS INVOKED, A MICROSUBROUTINE RETURN ADDRESS IS SAVED IN THE ERAR REGISTER BY THE ERU FLIP-FLOP. THIS IS DONE IN THE SAME MANNER AS THE NORMAL MICROSUBROUTINE WITH THE RAR AND THE RU FLIP-FLOP. THE COMPLEMENT CORRECTION ADDRESS IS Ø(0777) AND THIS ADDRESS IS JAMMED INTO THE MAR INDEPENDENTLY OF THE CONTENTS OF THE MIR(NA) REGISTER.

MAINTENANCE RESET FUNCTIONS (MRF)

FOR THE MAINTENANCE RESET FUNCTION OR IN OTHER WORDS FOR INITIALIZATION PURPOSES A SPECIAL STARTING ADDRESS CAN BE JAMMED INTO THE MAR INDEPENDENT OF THE PRESENT STATE OF THE MICROPROGRAM CONTROL. THIS ADDRESS IS THE START OF A SEQUENCE OF MICROCODE THAT WILL SAVE A FEW KEY REGISTERS IN THE 3A CC AND IT WILL THEN INITIALIZE THE 3A CC AS A FUNCTION OF THE SOURCE OF INITIALIZATION AS WELL AS THE PRESENT STATE OF 3A CC AND THE SYSTEM. SEE SHEET B7GG FOR A DESCRIPTION OF THE SOURCES OF INITIALIZATION AND HOW THEY INITIALIZE THE 3A CC HARDWARE TO PERMIT THE EXECUTION OF THE MRF MICROCODE.

FREEZE FUNCTION

THE MCH HAS THE ABILITY TO LOAD A MICROINSTRUCTION (LOW 16 BITS OF THE MIR) OR TO LOAD AN ADDRESS AND THE CONTROL BITS CA AND CB (HIGH 16 BITS OF MIR) WHEN THE STOP BIT IS SET. WHEN THE MCH DOES LOAD AN ADDRESS, IT IS GATED TO THE MAR VIA THE NORMAL P1 CLOCKING THAT GATES THE MIR(NA) TO THE MAR. ONCE IN MAR, THE MCH HAS THE ABILITY TO FREEZE THIS ADDRESS IN THE MAR SO THAT ON SUBSEQUENT MCH ORDERS, THE CONTENTS OF THAT MICROPROGRAM STORE WORD CAN BE ACCESSED OR READ BY THE MCH AND HENCE THE OTHER 3A CC. THE FREEZE FLIP-FLOP IS DESCRIBED ON SHEET B7GG. ITS OUTPUT IS USED TO INHIBIT THE P1 CLOCK VIA THE SAME METHOD AS THE CA BIT DOES, AS SHOWN IN COMPOSITE DIAGRAM 2. NOTE THAT UNLIKE THE CA BIT, THE FREEZE FLIP-FLOP INHIBITS THE P1 CLOCK PHASE FOR BIT 0 OF THE MAR. WHEN FREEZE FLIP-FLOP IS SET, THE STOP FLIP-FLOP MUST, OF COURSE, BE CLEARED.

PART OF FS 1

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
65	5A

BELL LABORATORIES | SD-1C900-01 | BIGN

PART OF FS 1

MICROCONTROL

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2-16 (CONT)

CIRCUIT OPERATION (CONT)

STOP ADDRESS

THE STOP FLIP-FLOP (SEE FS 5) IS USED TO DEFINE A STOP STATE FOR THE 3A CC WHEN AN ERROR HAS OCCURRED OR WHEN MAINTENANCE ACCESS TO THE MICROPROGRAM CONTROL IS REQUIRED. WHEN THE STOP FLIP-FLOP IS SET, ITS OUTPUT IS USED TO JAM A SPECIAL ADDRESS INTO THE MAR INDEPENDENTLY OF THE PRESENT STATE OF THE MICROPROGRAM CONTROL. THIS ADDRESS, 0 (0377), CONTAINS ALL ZEROS IN EVERY BIT POSITION OF THAT LOCATION. WHEN THE STOP FUNCTION IS ACTIVATED ALL MICROSEQUENCING IS TERMINATED AND ALL CHECK CIRCUITS THAT MIGHT GIVE ERRONEOUS ERROR OUTPUTS ARE INHIBITED. THE PLACING OF ALL-ZEROS IN THE STOP ADDRESS PERMITS THE MCH, WHEN THE MICROPROGRAM CONTROL IS STOPPED, TO PERFORM MICROINSTRUCTIONS. THAT IS, THE MCH CAN "OR" ONTO THE OUTPUT OF THE MICROPROGRAM STORE ON A SINGLE CYCLE BASIS HENCE, IT CAN PERFORM ANY MICROINSTRUCTION USING THE IDENTICAL CIRCUITRY USED TO BUFFER AND DECODE MICROINSTRUCTIONS. SEE FS 9 FOR ADDITIONAL DETAILS.

MICROINTERPRET

MICROINTERPRET IS A SPECIAL MACROLEVEL INSTRUCTION THAT ALLOWS MICROINSTRUCTIONS STORED IN THE MAS TO BE EXECUTED BY THE MICROPROGRAM CONTROL. THE MACROLEVEL INSTRUCTION BEGINS BY SETTING THE MINT (MICROINTERPRET MODE) FLIP-FLOP. THEN IT ISSUES A MAS REQUEST FOR THE NEXT SEQUENCIAL WORD IN THE MAS WHICH WILL BE A MICROINSTRUCTION (I.E. TWO 4-OUT-OF-8 CODES REPRESENTING TO- AND FROM-FIELD FUNCTIONS). WHEN THE MINT FLIP-FLOP IS SET, IT INHIBITS THE LNOP AND THE LINT FUNCTION (SEE COMPOSITE DIAGRAM 12). AS A RESULT, THE WORD FETCHED FROM THE MAS WILL NOT BE USED AS AN OP CODE AND NO INTERRUPTS WILL BE SERVICED. WHEN THE ALL-ZERO'S DETECTOR FIRES THE SMINT FLIP-FLOP WILL BE ACTIVATED (SEE COMPOSITE DIAGRAM 13). THE SMINT WILL ADD ONE TO THE ALL-ZERO'S ADDRESS AND THE MICROCONTROL WILL IN TURN ACCESS LOCATION "ONE". AT LOCATION "ONE", ALL ZERO'S ARE IN THE TO- AND FROM-FIELDS. DURING THE MICROCYCLE WHEN ADDRESS "ONE" IS BEING ACCESSED, THE OMINT FLIP-FLOP "OR"S THE CONTENTS OF SIR0 INTO THE TO- AND FROM-FIELDS OF THE MIR. AS A RESULT, A SINGLE MICROINTERPRET INSTRUCTION IS PERFORMED. IN THE NA FIELD OF ADDRESS "ONE", THE ADDRESS OF THE NEXT INSTRUCTION IN THE MICROINTERPRET SEQUENCE IS LOCATED. THIS ADDRESS IS THE START OF A SEQUENCE OF MICROCODE THAT DETERMINES WHETHER THIS IS A SINGLE CYCLE MICROINTERPRET OR A MULTIPLE CYCLE MICROINTERPRET OPERATION. IF IT IS A SINGLE CYCLE MICROINTERPRET, THE MINT BIT IS CLEARED AND THE NEXT WORD FETCHED FROM THE MAS WILL BE USED AS MACROLEVEL OPCODE. IF IT IS MULTIPLE CYCLE MICROINTERPRET, THE MINT FLIP-FLOP IS NOT CLEARED, THE MAS FETCH IS GIVEN AND THE PROCESS REPEATS ITSELF. IN THE MULTIPLE CYCLE CASE, THE LAST MICROINTERPRET INSTRUCTION OF THE SEQUENCE MUST CLEAR THE MINT FLIF-FLOP. NOTE THAT MICROINTERPRET INSTRUCTION CAN NOT BE PERFORMED FROM THE SIR1 OR WHILE THE 3A CC HAS THE OPF BIT=1, OR IN OTHER WORDS, IN THE NO. 2 ESS EMULATION MODE.

MICROPROGRAM CONTROL STATE (MCS) REGISTER

THE MCS REGISTER CONSISTS OF KEY STATUS FLIP-FLOPS THAT CONTROL MICROCODE EXECUTION FLOW. AS SHOWN IN COMPOSITE DIAGRAM 14, THE MCS IS DUPLICATED WITH THE MCS0 BEING USED AS THE DATA COPY. IN OTHER WORDS, IT IS USED TO CONTROL THE EXECUTION FLOW. MCS1 IS THE CHECK COPY AND IS USED TO INPUT THE CHECK CIRCUITS THAT ENSURE THE INTERGRITY OF THE EXECUTION FLOW. THE MOST IMPORTANT CHECK OF THE MCS REGISTER AND THE INPUTS THAT CONTROL IT, IS THE MAR PARITY CHECK (SEE SHEET 81GT). A BIT IN MCS REGISTER IS TYPICALLY TESTED BY DOING A CONDITIONAL BRANCH ON THAT BIT. THIS CONDITIONAL BRANCH CONSISTS OF GATING COPY 0 OF THE MCS BIT INTO THE MAR BIT 0. COPY 1 OF THE MCS BIT IS USED TO MODIFY THE MAR PARITY BIT ACCORDINGLY.

SINCE MCS0 MUST MODIFY THE MAR REGISTER, THE CONTROL THAT TESTS OR GATES THE MCS0 BIT TO THE MAR MUST TAKE PLACE BY CLOCK PHASE P1. THIS IS THE CLOCK PHASE THAT IS USED TO GATE TO THE MAR. TO PROVIDE THIS CONTROL, A SO CALLED "FAST MISCELLANEOUS DECODER" IS USED. THE FAST-MISCELLANEOUS DECODER IS SHOWN IN COMPOSITE DIAGRAM 14, SYMBOL NO. 5. IT CONSISTS OF DECODING THE DIRECT OUTPUTS OF THE TO- AND FROM-FIELDS FROM THE MICROPROGRAM STORE INTO ROWS AND COLUMNS OF THE MISCELLANEOUS DECODER MATRIX. NOTE THE COMPARISON WITH THE NORMAL TO AND FROM DECODING AND THE SUBSEQUENT DECODING OF THE DUPLICATE MISCELLANEOUS DECODER FUNCTION IN SYMBOL NO. 4. IN SYMBOL NO. 4, THE TO-AND-FROM-CONTROL INPUTS ARE OUTPUTS FROM THE TO- AND FROM-FIELD DECODERS AND HENCE ARE FIVE GATE DELAYS IN TIME AWAY FROM THE OUTPUT OF THE MICROPROGRAM STORE. THE FAST-MISCELLANEOUS DECODER MUST BUFFER THE OUTPUT OF THE MICROPROGRAM STORE IN THE ROW AND COLUMN FLIP-FLOP REGISTER SHOWN, SINCE THE OUTPUT OF THE MICROPROGRAM STORE IS ONLY STABLE FOR CLOCK PHASE P0. THE MISCELLANEOUS CONTROL IMPLEMENTED IN COMPOSITE DIAGRAM 15 PROVIDES DUPLICATE CONTROL FOR

CIRCUIT OPERATION (CONT)

EACH OF THE MCS BITS AND A NUMBER OF ASSOCIATED FUNCTIONS. FOR A COMPLETE LIST OF THESE FUNCTIONS AND A BRIEF DESCRIPTION SEE COMPOSITE DIAGRAM 16.

MOST OF THE CONTROL ASSOCIATED WITH THE MCS REGISTER IS SELF EVIDENT OR EXPLAINED IN COMPOSITE DIAGRAM 16, BUT THE DML X GB CONTROL NEEDS ADDITIONAL EXPLANATION. WHEN A DML FUNCTION IS PERFORMED (SEE FS 2) THE RESULT IS GATED TO THE GB. THERE ARE THREE CASES WHERE THE DML X GB DIRECTLY EFFECTS THE MCS REGISTER:

(1) IF A BOOLEAN FUNCTION IS ACTIVE (DEFINED AS NO ADD FUNCTIONS ACTIVE) THE GB WILL BE TESTED FOR ALL ZERO'S. IF THE GB=0'S, THEN THE DS BIT WILL BE SET.

(2) IF AN ADD SHORT IS PERFORMED, THE STATE OF THE OVER-~~FLOW SIGNAL~~ OF ~~BIT 15 OF THE ADDER WILL~~ BE GATED INTO THE DS.

(3) IF AN ADD LONG IS PERFORMED THE STATE OF THE OVERFLOW SIGNAL OF BIT 19 OF THE ADDER WILL BE GATED INTO THE DS.

NOTE THAT THE RU AND THE DR BITS OF THE MCS REGISTER DO NOT PHYSICALLY RESIDE ON SYMBOL NO. 4 AND 5. THEY ARE HOWEVER, DUPLICATED AND ARE ADDRESSED AND TESTED AS PART OF THE MCS REGISTER.

THE FOLLOWING IS A BRIEF DESCRIPTION OF THE FUNCTIONS OF THE MCS STATE.

CF - THE MICROPROGRAMMER CONVEYS THE RESULTS OF VARIOUS FUNCTIONS THAT ARE PERFORMED AS THE RESULT OF A MACROLEVEL COMMAND THROUGH THE CF. UNLESS DIRECTED TO PERFORM SUCH A FUNCTION AND HENCE POTENTIALLY CHANGE THE STATE OF THE CF, THE MICROPROGRAMMER MUST PRESERVE THE STATE OF THE CF.

DS - THE DS IS TO THE MICROPROGRAMMER AS THE CF IS TO THE MACROLEVEL PROGRAMMER. THE DS BUFFERS THE STATE OF MICROLEVEL FUNCTIONS SUCH AS ADDER OVERFLOWS, BIT TESTS, ETC.

TR1 AND TR2 - THESE TWO BITS ARE USED AS GENERAL PURPOSE STATUS BITS USE VIA THE MICROPROGRAMMER.

DR - THE DR IS USED TO INDICATE THAT THE MAIN STORE HAS COMPLETED A REQUESTED CYCLE.

RU - THE RU IS USED TO UPDATE THE RETURN ADDRESS REGISTER.

IFF - THE IFF IS USED FOR THE NO. 2B ESS APPLICATION TO SELECT WHICH SIR, SIR0 OF SIR1 IS TO BE USED AS THE SOURCE OF AN OPCODE FETCH FROM THE MAIN STORE.

OPF - THE OPF IS USED TO GENERATE AN ADDITIONAL 128 WORDS OF OPCODE ENTRY POINTS FOR THE NO. 2B ESS APPLICATION. THIS BIT, WHEN SET, DEFINES THE 3A CC TO BE IN THE NO. 2B ESS EMULATION MODE.

ERU - (SEE SHEET 011)
THE ERU IS USED TO UPDATE THE ERROR RETURN ADDRESS REGISTER.

PART OF FS 1

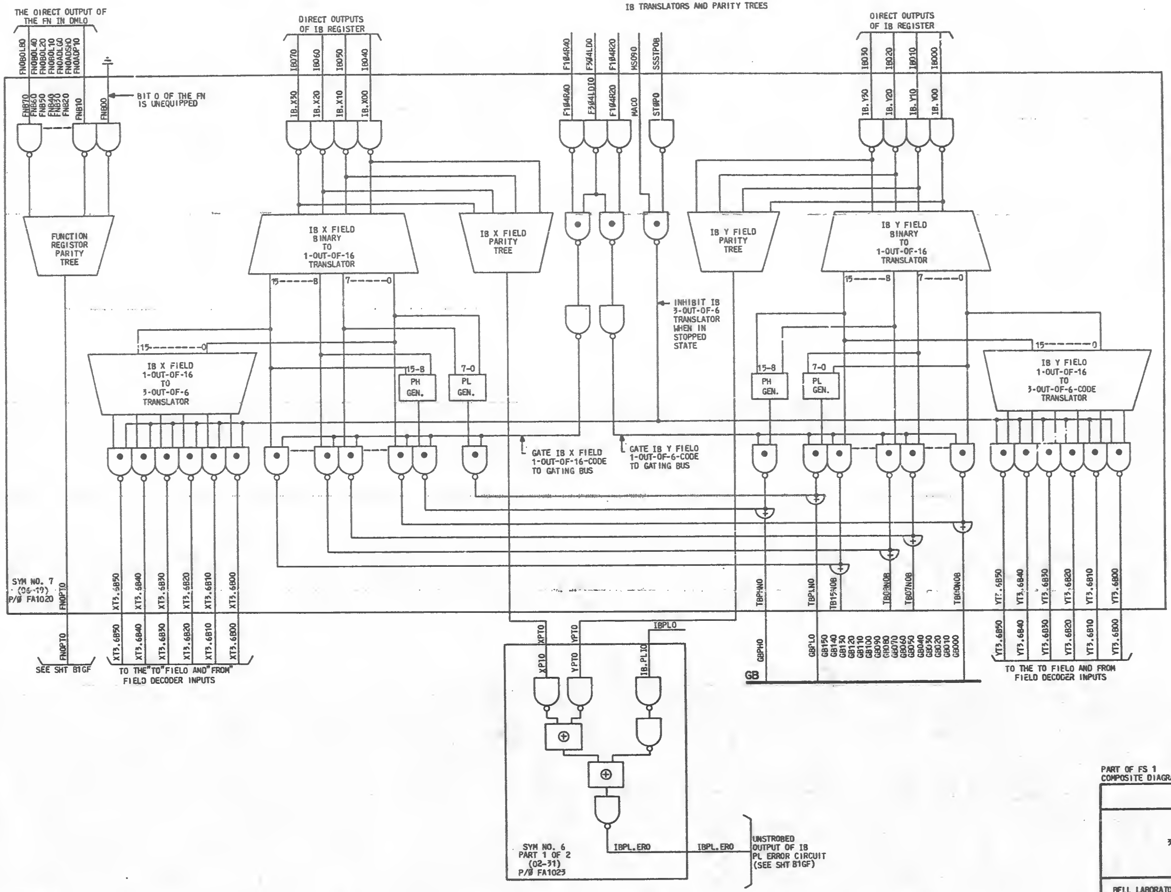
3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	BIGP

PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 17

IB TRANSLATORS AND PARITY TREES



CIRCUIT OPERATION

THE IB TRANSLATOR GENERATES 1-OUT-OF-16 AND A 3-OUT-OF-6 CODE FOR EACH OF THE BINARY 4 BIT FIELDS X AND Y IN THE IB REGISTER. THE 1-OUT-OF-16 CODE CAN BE GATED TO THE GB DIRECTLY SINCE PARITY IS PROVIDED ON THE 1-OUT-OF-16 OUTPUT FUNCTION. THE 3-OUT-OF-6 CODE PERMITS THE X AND Y OPERAND FIELDS IN THE IB TO BE USED IN CONJUNCTION WITH A 1-OUT-OF-2 CODE FROM THE MICROPROGRAM STORE TO DIRECTLY GENERATE A 4-OUT-OF-8 CODE USED BY THE TO AND FROM DECODERS TO PERFORM REGISTER GATING OPERATION (SEE SHEET B1GV AND B1GW).

THE IB PARITY TREE ENSURES THAT DATA GATED TO THE IB REGISTER IS CORRECT. NOTE THAT FOR MOST REGISTERS THE CHECK OF THE DATA WITHIN IT IS NOT MADE UNTIL THE REGISTER IS GATED ONTO THE GB. IN THE CASE OF THE IB, ITS DATA IS USED WITHOUT PLACING IT BACK OUT ONTO THE GB AND HENCE AN INTERNAL PARITY CHECK IS REQUIRED. THE FN REGISTER PARITY TREE IS USED TO ENSURE THE DATA PLACED IN THE FN REGISTER IS CORRECT AND THE CHECK IS REQUIRED FOR THE SAME REASON AS THE IB PARITY CHECK.

PART OF FS 1
COMPOSITE DIAGRAM 17

3A CENTRAL CONTROL	2	DWG SIZE 6S	ISSUE 4A
BELL LABORATORIES	SD-1C900-01		B1GR

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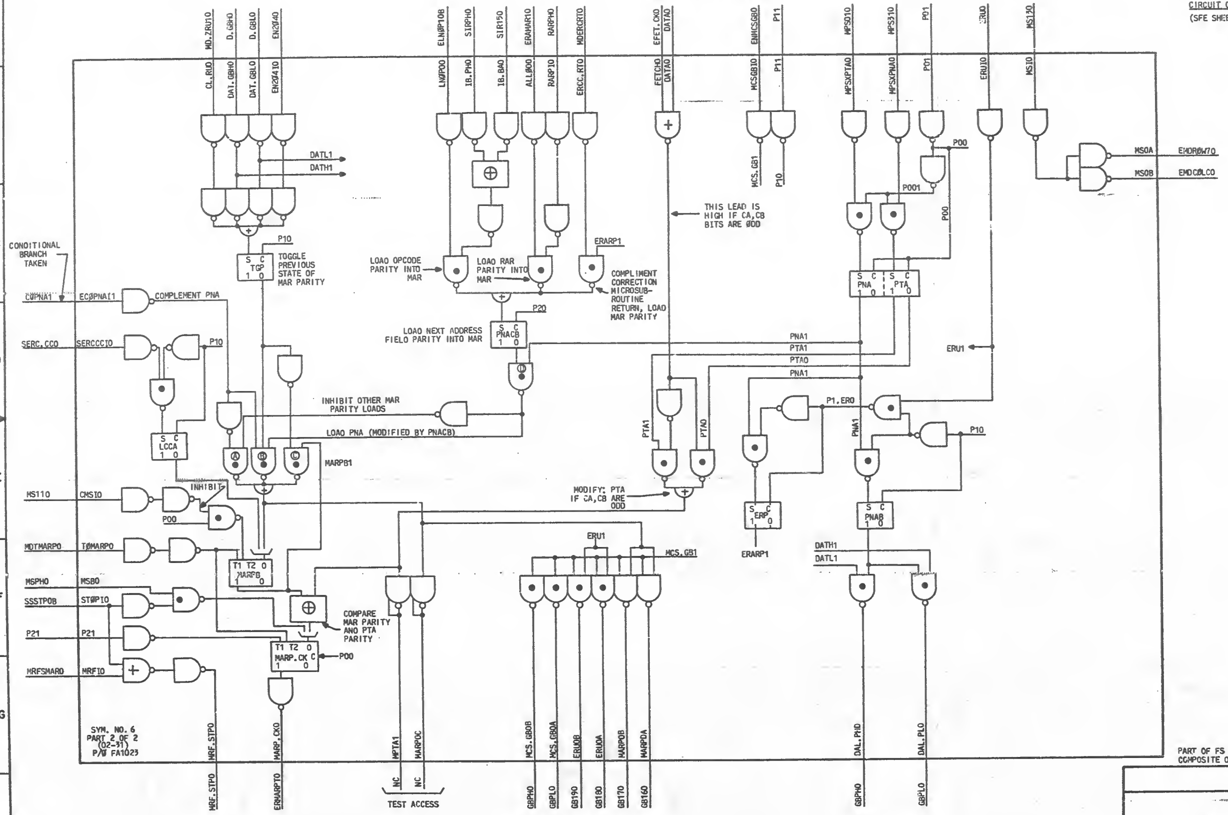
PART OF FS 1

MICROCONTROL

COMPOSITE DIAGRAM 18

MAR PARITY CIRCUIT AND CHECK

CIRCUIT OPERATION
(SFE SHEET B1GU)



PART OF FS 1
COMPOSITE DIAGRAM 18

3A CENTRAL CONTROL

②

DWG SIZE	ISSUE
6S	4A

BELL LABORATORIES

SD-1C900-01

BIGT

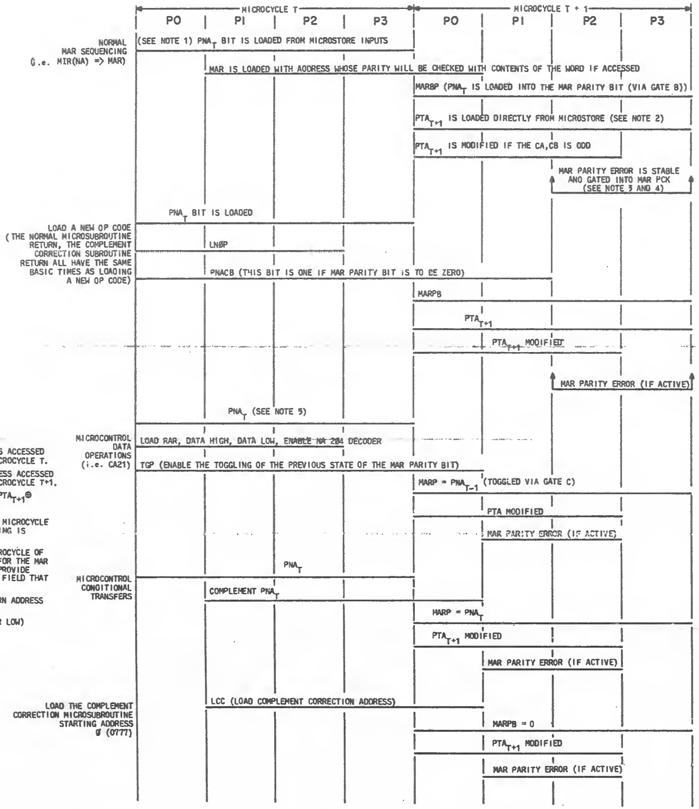
E-7021 (12-73)

PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 19

MAR PARITY CIRCUIT AND CHECK TIMING


MICROCYCLE T
MICROCYCLE T + 1
P0
P1
P2
P3
P0
P1
P2
P3
NORMAL MAR SEQUENCING (i.e. MIR(NA) => MAR)
(SEE NOTE 1) PNA_T BIT IS LOADED FROM MICROSTORE INPUTS
MAR IS LOADED WITH ADDRESS WHOSE PARITY WILL BE CHECKED WITH CONTENTS OF THE WORD IF ACCESSED
MARBP (PNA_T IS LOADED INTO THE MAR PARITY BIT (VIA GATE B))
PTA_T+1 IS LOADED DIRECTLY FROM MICROSTORE (SEE NOTE 2)
PTA_T+1 IS MODIFIED IF THE CA,CB IS ODD
MAR PARITY ERROR IS STABLE AND GATED INTO MAR PCK (SEE NOTE 3 AND 4)
LOAD A NEW OP CODE (THE NORMAL MICROSUBROUTINE RETURN, THE COMPLEMENT CORRECTION SUBROUTINE RETURN ALL HAVE THE SAME BASIC TIMES AS LOADING A NEW OP CODE)
PNA_T BIT IS LOADED
LNØP
PNACB (THIS BIT IS ONE IF MAR PARITY BIT IS TO BE ZERO)
MARPB
PTA_T+1
PTA_T+1 MODIFIED
MAR PARITY ERROR (IF ACTIVE)
MICROCONTROL DATA OPERATIONS (i.e. CA21)
PNA_T (SEE NOTE 5)
LOAD RAR, DATA HIGH, DATA LOW, ~~ENABLE NA 2Ø4~~ DECODER
TGP (ENABLE THE TOGGLING OF THE PREVIOUS STATE OF THE MAR PARITY BIT)
MARP = PNA_T-1 (TOGGLED VIA GATE C)
PTA MODIFIED
MAR PARITY ERROR (IF ACTIVE)
MICROCONTROL CONDITIONAL TRANSFERS
PNA_T
COMPLEMENT PNA_T
MARP = PNA_T
PTA_T+1 MODIFIED
MAR PARITY ERROR (IF ACTIVE)
LOAD THE COMPLEMENT CORRECTION MICROSUBROUTINE STARTING ADDRESS Ø (0777)
LCC (LOAD COMPLEMENT CORRECTION ADDRESS)
MARPB = 0
PTA_T+1 MODIFIED
MAR PARITY ERROR (IF ACTIVE)

NOTES:

1. PNA_T - PARITY FOR NEXT ADDRESS ACCESSED FROM THE MICROSTORE DURING MICROCYCLE T.
2. PTA_T+1 - PARITY FOR THIS ADDRESS ACCESSED FROM THE MICROSTORE DURING MICROCYCLE T+1.
3. FOR CORRECT OPERATION $PNA_T = PTA_{T+1} \oplus CA_{T+1} \oplus CB_{T+1} \oplus$
4. THE MAR PARITY ERROR OCCURS 1 MICROCYCLE AFTER THE ADDRESS IT IS CHECKING IS LOADED INTO THE MAR.
5. THE PNA BIT ACCESSED ON A MICROCYCLE OF A DATA OPERATION IS NOT USED FOR THE MAR PARITY CHECK. IT IS USED TO PROVIDE GOOD PARITY CHECK ON THE DATA FIELD THAT IS EITHER:
   a. LOADED INTO THE RAR (RETURN ADDRESS FOR A MICROSUBROUTINE)
   b. GATED ONTO THE GB (HIGH OR LOW)
   c. LOADED IN THE FN REGISTER

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 18 AND 19

EACH TIME A WORD IS READ OUT OF THE MICROSTORE BY LOADING AN ADDRESS INTO THE MAR, A PARITY CHECK IS PERFORMED TO INSURE THE PROPER ACCESSING. THE INCLUSION OF THIS PARITY CHECK ALSO PROVIDES THE ABILITY TO CHECK A NUMBER OF CONTROL SIGNALS THAT ARE REQUIRED TO SEQUENCE THE MICROSTORE ADDRESSING. THIS CIRCUITRY INCLUDES THE DUPLICATED COPIES OF THE MCS AND THE MISCELLANEOUS DECODERS CROSSPOINTS THAT MANIPULATE THESE BITS.

THE PARITY CHECK IS IMPLEMENTED VIA THE PNA AND PTA PARITY BITS READOUT OF THE MICROPROGRAM STORE ON EVERY MICROCYCLE. THE PNA BIT IS THE PARITY-NEXT ADDRESS AND IT IS TYPICALLY LOADED INTO THE MAR PARITY BIT (MARPB) IN EACH MICROCYCLE. WHEN THIS NEXT-ADDRESS IS ACCESSED, THE MAR PARITY BIT SHOULD EQUAL THE PTA BIT, PARITY THIS ADDRESS. THE PARITY CHECK IS SLIGHTLY MODIFIED TO INCLUDE A CHECK OF THE CA, CB BITS. THAT IS, THE MAR PARITY BIT SHOULD EQUAL PTA IF THE CA, CB BITS ARE EVEN. IT SHOULD NOT BE EQUAL TO PTA=1 IF CA, CB BITS ARE ODD (I.E., MAR PARITY=PTA + CA + CB).

AS INDICATED ON SHEET B1GD, THERE ARE A NUMBER OF WAYS OF LOADING ADDRESSES INTO THE MAR. WHEN THE DIFFERENT METHODS ARE USED, THE MAR PARITY BIT MUST BE MODIFIED ACCORDINGLY. THERE ARE THREE DISTINCT METHODS OF MODIFYING THE MAR PARITY BIT APART FROM LOADING IT DIRECTLY.

1. COMPLEMENT ITS PREVIOUS STATE. FOR THE CASE WHERE THE CA CONTROL BIT IS USED, THE OLD CONTENTS OF THE MAR ARE SAVED, AND BIT 0 OF THE MAR IS JAMMED FROM 0 TO 1, THE MAR PARITY BIT MUST BE COMPLEMENTED. IN COMPOSITE DIAGRAM 18 (A1) THE VARIOUS CONTROL FUNCTIONS THAT CAN BE PERFORMED WHEN THE CA CONTROL BIT IS ACTIVE ARE USED TO TOGGLE THE MAR PARITY BIT.
2. COMPLEMENT PNA BIT. ON A NORMAL ADDRESSING SEQUENCE, THE MIR(NA) REGISTER IS GATED DIRECTLY INTO THE MAR HENCE. THE PNA BIT IS ALSO GATED DIRECTLY TO THE MAR PARITY BIT. WHEN A CONDITIONAL BRANCH IS PERFORMED, BIT 0 OF THE MAR IS JAMMED FROM A 0 TO A 1 IF THE BRANCH IS SUCCESSFUL. THEREFORE, THE PNA BIT MUST BE COMPLEMENTED BEFORE PUTTING THE BIT IN THE MAR PARITY BIT IF A CONDITIONAL BRANCH IS THERE.
3. IN A NUMBER OF CASES, A NEW ADDRESS IS LOADED INTO THE MAR, BUT THE STATE OF THE PNA BIT THAT IS FLOWING INTO THE MAR PARITY BIT IS KNOWN. FOR EXAMPLE, WHEN AN OP CODE IS LOADED INTO THE MAR, THE PNA BIT=1 SINCE THE MIR(NA)=0'S. IN FACT, IF THE LNØP FUNCTION IS NOT ACTIVE, THE ALL-ZERO'S ADDRESS IS GATED TO THE MAR AND HENCE THE PNA=1 IS REQUIRED IN THE ~~MAR~~ PARITY BIT. WHEN THE OP CODE IS LOADED, THE MAR PARITY BIT IS DETERMINED BY THE IB PH BIT AND THE BA CHECK BIT. THIS PH COVERS THE OP CODE FIELD AND THE BA BIT IN THE IB REGISTER. THEREFORE, THE PARITY OVER THE OP CODE FIELD MUST BE MODIFIED ACCORDINGLY.

THE RAR PARITY BIT IS LOADED DIRECTLY INTO THE MAR PARITY BIT BUT THE CONTROL PATH INPUT ASSUMES THE PNA BIT=1 FOR THIS FUNCTION (NA IS ALL "ONES"). THE ERAR PARITY BIT IS ALSO LOADED DIRECTLY INTO THE MAR PARITY BIT AND IT REQUIRES THAT THE PNA BIT=1.

THE INVOKING OF THE MICROCODE COMPLEMENT CORRECTION STARTING ADDESS REQUIRES THAT THE MAR PARITY BIT BE ZEROED SINCE THIS FUNCTION STARTS AT ADDRESS (0777).

THE INTERRUPT STARTING ADDRESS DOES NOT CHANGE THE PARITY OF THE ALL-ZERO'S WORD. HENCE, THE PNA BIT FROM THE ALL-ZERO'S WORD WILL BE GATED INTO THE MAR PARITY BIT AS USUAL AND PROVIDE CORRECT PARITY FOR THE INTERRUPT ADDRESS Ø(0120).

THE MRF ADDRESS DOES NOT REQUIRE PARITY TO BE LOADED SINCE THE INITIALIZATION FUNCTION TENDS TO CREATE A MAR PARITY ERROR. IT ALSO CREATES SOME OTHER ERRORS BECAUSE THE 3A CC CLOCK IS STOPPED AND RESTARTED. THE DISTURBANCE OF THE CLOCKS THEREFORE, TENDS TO CAUSE ERRORS BUT THEIR OCCURANCE IS NOT DETERMINISTIC.

THE STOP FUNCTION INHIBITS THE BLOCKING THE MAR PARITY CHECK AND HENCE IT DOES NOT ATTEMPT TO LOAD THE MAR PARITY BIT.

AS SHOWN IN COMPOSITE DIAGRAM 18, A MAINTENANCE STATE CAN INHIBIT THE STROBING OF THE MAR CHECK CIRCUIT. A MISCELLANEOUS DECODER CROSSPOINT CAN THEN SAMPLE, AT THE APPROPRIATE INTERVAL, VARIOUS TEST CONDITIONS IN THE MAR PARITY CHECK CIRCUITRY. THE MAR PARITY BIT CAN BE ACCESSED VIA THE MCS REGISTER. THAT IS, THE MAR PARITY BIT IS PLACED ONTO THE MCS REGISTER OUTPUT TO THE GB WITH A DUPLICATED ACCESS TO THE MAR PARITY BIT.

PART OF FS 1
COMPOSITE DIAGRAM 19

3A CENTRAL CONTROL
②
DWG SIZE 6S
ISSUE 5A
BELL LABORATORIES
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B1GU

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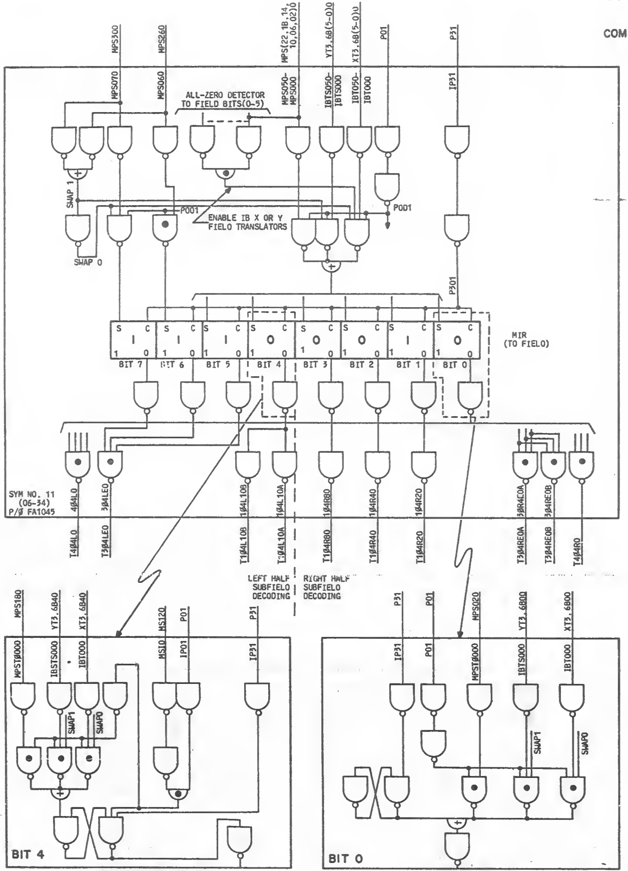
PART OF FS 1

MICROCONTROL

COMPOSITE DIAGRAM 20

"TO FIELD" DECODER



REPRESENTATIVE OF LEFT HALF SUBFIELD DECODING

REPRESENTATIVE OF RIGHT HALF SUBFIELD DECODING

CIRCUIT OPERATION

THE TO-FIELD DECODER BUFFERS A 4-OUT-OF-8 CODE RECEIVED AT ITS INPUT AND DECODES THIS CODE INTO A 1-OUT-OF-70 STATE CONDITION ON ITS OUTPUTS. THE TO-FIELD DECODER DESIGN RESULTS IN PARTITIONING THE TO-FIELD BUFFER REGISTER INTO TWO HALVES, A LEFT HALF AND A RIGHT HALF. THE PARTITION IS A RESULT OF THE FACT THAT THE FINAL STAGE OF DECODING IS NOT PERFORMED WITHIN THE TO-FIELD DECODER CIRCUIT PACK. IT IS INSTEAD PERFORMED ON THE CIRCUIT PACK ON WHICH THE CONTROL FUNCTION IS USED. THEREFORE, BY PARTITIONING THE DECODER IN TWO HALVES, ONLY 32, 16 FROM EACH HALF, DISTINCT CONTROL SIGNALS ARE REQUIRED TO OUTPUT FROM THE TO-FIELD DECODER INSTEAD OF THE POSSIBLE 70 IF THE FINAL STAGE OF DECODING WAS PERFORMED. THE DECODING ON A PARTITIONED HALF CONSISTS OF DETERMINING THE COMBINATION OF BIT POSITIONS IN WHICH A ONE IS LOCATED. FOR EXAMPLE, IF THERE ARE 3 ONES IN THE 4-BIT LEFT SUBFIELD, THERE WOULD BE A POSSIBLE 4 GATES IN THE LEFT HALF THAT WOULD BE ACTIVE (I.E., 0111,1011,1101, AND 1110). FOR EACH OF THESE FOUR STATES, THERE WOULD BE CORRESPONDING 4 GATES IN THE RIGHT HALF THAT COULD BE ACTIVE (I.E.,1000,0100,0010, AND 0001) FOR A TOTAL OF 16 UNIQUE COMBINATIONS. THE FOLLOWING IS A LIST OF THE COMBINATIONS OF ONES IN EACH 4-BIT SUBFIELD AND THE CORRESPONDING ONES IN ITS ASSOCIATED SUBFIELD:

COMBINATIONS	LEFT SIDE	RIGHT SIDE
1	4-OUT-OF-4	0-OUT-OF-4
16	3-OUT-OF-4	1-OUT-OF-4
36	2-OUT-OF-4	2-OUT-OF-4
16	1-OUT-OF-4	3-OUT-OF-4
1	0-OUT-OF-4	4-OUT-OF-4
70 TOTAL		

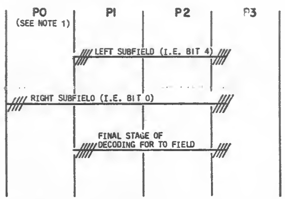
FOR EXAMPLE, IF THE 3-OUT-OF-4 GATE (1110) WAS ACTIVE IN THE LEFT SUBFIELD, THEN THE 2-OUT-OF-4 GATES (1100, 1010, 0110) WOULD ALSO BE ACTIVE. HOWEVER, ONLY A UNIQUE 1-OUT-OF-4 GATE IN THE RIGHT SUBFIELD WOULD BE ACTIVE IN ORDER TO PERFORM THE CORRECT FINAL STAGE OF DECODING.

THE TIMING ON THE TO-FIELD DECODER OUTPUT IS SUCH THAT THE LEFT SUBFIELD IS ACTIVATED DURING CLOCK PHASES P1, AND P2. THE RIGHT SUBFIELD IS ACTIVE DURING CLOCK PHASES P0, P1, AND P2. THEREFORE, THE FINAL STAGE OF DECODING IS ONLY ACTIVE DURING CLOCK PHASES P1 AND P2. THIS TIMING IS REQUIRED TO SATISFY THE TIMING REQUIREMENT OF A BASIC REGISTER TO REGISTER GATING OPERATION AS DESCRIBED ON SHEET B3GB.

THE LOW 6 BITS THAT INPUT FROM THE MICROPROGRAM STORE TO FIELD HAVE A ALL-ZERO'S DETECTOR ATTACHED. THIS DETECTOR, WHEN ACTIVE, IS USED TO GATE THE OUTPUT OF THE IB X-FIELD 3-OUT-OF-6 TRANSLATOR INTO BITS 0-5 OF THE TO FIELD. IF A 1-OUT-OF-2 CODE IS GATED INTO BITS 6 AND 7 (I.E., BIT 6=1 AND BIT 7=0) OF THE TO FIELD, A 4-OUT-OF-8 CODE WILL SELECT A GENERAL REGISTER AS A DESTINATION REGISTER FOR A GATING OPERATION. IF BITS 6 AND 7 ARE BOTH ONES, THE IB Y-FIELD 3-OUT-OF-6 TRANSLATOR OUTPUT IS "SWAPPED" FOR THE IB X-FIELD TRANSLATOR. ALSO, IF BITS 6 AND 7 ARE SET, IT RESULTS IN CLEARING BIT 6 OF THE TO FIELD SO THAT THE 4-OUT-OF-8 CODE GENERATED WILL SELECT ONE OF 16 SPECIAL REGISTERS. NOTE THAT THESE 16 SPECIAL REGISTERS DO NOT DIRECTLY CORRESPOND TO THE 16 SPECIAL REGISTERS DESIGNATED ON THE 3A CC CONTROL PANEL.

COMPOSITE DIAGRAM 21

TO-FIELD TIMING


P0
(SEE NOTE 1)
P1
P2
P3
LEFT SUBFIELD (I.E. BIT 4)
RIGHT SUBFIELD (I.E. BIT 0)
FINAL STAGE OF DECODING FOR TO FIELD

NOTES:

1. ALL INPUTS TO THE TO-FIELD DECODER (MICROSTORE OUTPUT, MCH OUTPUT, SIR OUTPUT) MICROINTERRUPT AND IB 3-OUT-OF-6 CODE TRANSLATORS MUST BE STABLE BEFORE P0 STARTS.

PART OF FS 1
COMPOSITE DIAGRAM 20,21

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES
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BIGV

PART OF FS 1

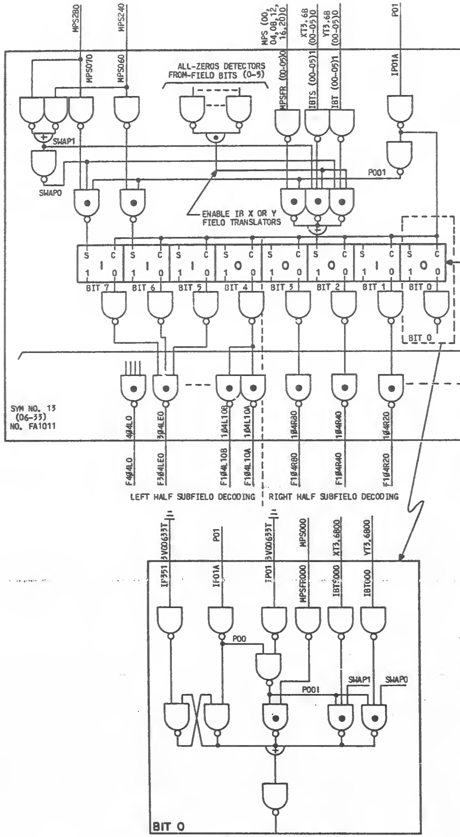
MICROCONTROL

COMPOSITE DIAGRAM 22

FROM-FIELD DECODER

CIRCUIT OPERATION

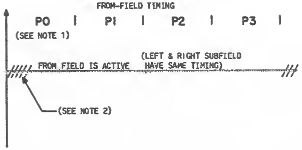
SAME AS TO-FIELD DECODER EXCEPT THAT DECODER CONTROL TIMING IS MODIFIED. SEE SHEET B1GV.



REPRESENTATIVE OF LEFT AND RIGHT SUBFIELD DECODING

COMPOSITE DIAGRAM 23

FROM-FIELD TIMING



NOTES

1. ALL INPUTS TO THE FROM DECODER (MICROSTORE OUTPUT, MCH OUTPUT, SIR OUTPUT) MICROINTERPRET AND THE IB 3-OUT-OF-6 CODE TRANSLATORS MUST BE STABLE BEFORE P0 STARTS.
2. SINCE THE FROM DECODER IS ACTIVE FOR THE FULL DURATION OF THE MICROCYCLE, IT IS POSSIBLE TO GET FROM FIELDS OVERLAPPING AT THE START AND END OF THEIR RESPECTIVE MICROCYCLES.

PART OF FS 1
COMPOSITE DIAGRAM 22, 23

3A CENTRAL CONTROL
②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES | SD-1C900-01 | B1GW

E-7421 (12-73)

CIRCUIT OPERATION

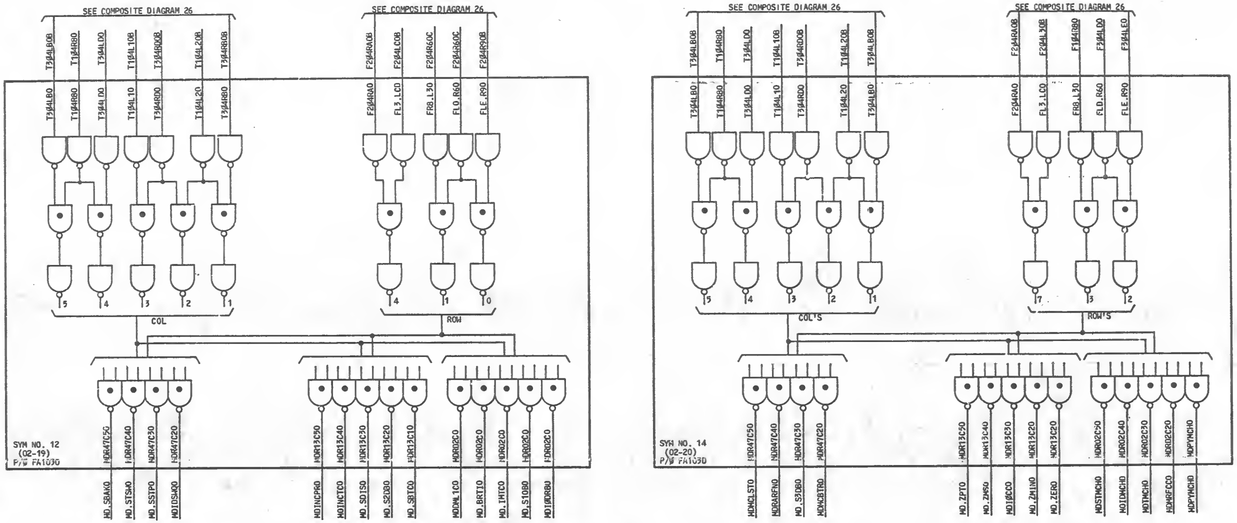
SEE COMPOSITE DIAGRAM 26 FOR A BRIEF DESCRIPTION OF THE MISCELLANEOUS DECODER FUNCTION.

PART OF FS I

MICROCONTROL

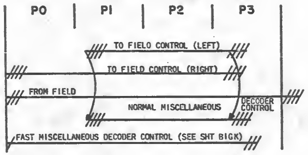
COMPOSITE DIAGRAM 24

MISCELLANEOUS DECODER CONTROL
(ASSOCIATED WITH BIT SLICED HIGH LOGIC PACKS)



COMPOSITE DIAGRAM 25

MISCELLANEOUS DECODER TIMING



PART OF FS 1
COMPOSITE DIAGRAM 24, 25

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	BIGX

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PART OF FS 1

MICROCONTROL

COMPOSITE DIAGRAM 26

ASSIGNMENT OF MISCELLANEOUS DECODER CONTROL
(ASSOCIATED WITH BIT SLICED HIGH LOGIC PACKS)

TABLE A

FUNCTION		FUNCTION OUTPUT			TO FIELD				FROM FIELD			
MNEMONIC	DESCRIPTION	NETNAME	(PIN NO)			(PIN NO.)		(PIN NO.)		(PIN NO.)		(PIN NO.)
SBA	SET THE BA CHECK LIST	MD.SBAKO	203	FA1030, SYM NO. 12 (02-19)	T304LB0B	(310)	T104R80	(110)	F204LC0B	(109)	F204RA0B	(309)
STPASW	INITIATE A STOP AND SWITCH TO OTHER CC	MD.STSWO	003		T304LD0	(100)	T104R80	(110)	F204LC0B	(109)	F204RA0B	(309)
SSTP	SET THE STOP BIT	MD.SSTPO	302		T104L10B	(011)	T304RD0B	(009)	F204LC0B	(109)	F204RA0B	(309)
IDSWQ	IDLE THE SWITCH SEQUENCER IN THE MCH	MDIDSWQO	202		T104L20B	(209)	T304RD0B	(009)	F204LC0B	(109)	F204RA0B	(309)
INCPR	INCREMENT THE PRESCALER (PART OF TC)	MD.INCPRO	305		T304LB0B	(310)	T104R90	(110)	F204L30B	(206)	F204R90B	(10)
INCTC	INCREMENT THE TIMING COUNTER	MD.INCTCO	105		T304LD0	(100)	T104R80	(110)	F204L30B	(206)	F204R90B	(010)
SDIS	SET THE OISABLE FLIP-FLOP	MD.SDISO	205		T104L10B	(011)	T304RD0B	(009)	F204L30B	(206)	F204R90B	(010)
SZDB	GATE SWITCH REGISTER 2 TO THE DB	MD.S2DBO	005		T104L20B	(209)	T304RD0B	(009)	F204L30B	(206)	F204R90B	(010)
SBTC	SET BLOCK TIMER CHECK BIT	MD.SBTCO	304		T104L20B	(209)	T304LB0B	(310)	F204L30B	(206)	F204R90B	(010)
DML1=> CR	GATE OUTPUT OF DML1 TO CR	MDDML1CO	104		T304LB0B	(310)	T104R80	(110)	F204L30B	(206)	F204R60C	(006)
BR=> TI	GATE BR (15-0) TO TI (15-0)	MD.BRTIO	204		T304LD0B	(100)	T104R30	(110)	F204L30B	(206)	F204R60C	(006)
SIDB	GATE SWITCH REGISTER 1 TO THE DB	MD.S10BO	303		T104L20B	(209)	T304RD0B	(009)	F204L30B	(206)	F204R60C	(006)
I0D=> R11	GATE THE I0D TO R11	MDI0DRBO	103		T104L20B	(209)	T304LB0B	(310)	F204L30B	(206)	F204R60C	(006)
IMTC	IOLE THE MCH	MD.IMTCO	004		T104L10B	(011)	T304RD0B	(009)	F204L30B	(206)	F204R60C	(006)
MCLSTR	LOAD THE START CODE BIT INTO MCH	MDMCLSTO	203	FA1030, SYM NO. 14 (02-20)	T304LB0B	(310)	T104R90	(110)	F204L30B	(109)	F204RA0B	(309)
RAR=> FN	GATE RAR TO FN	MDRARFNO	003		T304LD0B	(100)	T104R80	(110)	F204L30B	(109)	F204RA0B	(309)
S3DB	GATE SWITCH REGISTER 3 TO DB	MD.S3DBO	302		T104L10B	(011)	T304RD0B	(009)	F204L30B	(109)	F204RA0B	(309)
MCHB = > MCHTR	GATE MCHB TO MCHTR	MDMCBTRO	202		T104L20B	(209)	T304RD0B	(009)	F204L30B	(109)	F204RA0B	(309)
ZPT	CLEAR THE PROGRAM TIMER	MD.ZPTO	305		T304LB0B	(310)	T104R80	(110)	F304LE0	(010)	F104R80	(206)
ZMS	CLEAR THE MAINTENANCE STATE REGISTER	MD.ZMSO	105		T304LD0B	(100)	T104R80	(110)	F304LE0	(010)	F104R80	(206)
I0CC	INTERRUPT THE OTHER 3A CC	MDI0CCO	205		T104L10B	(011)	T304RD0B	(009)	F304LE0	(010)	F104R80	(206)
ZMINT	CLEAR THE MICROINTERPRET BIT	MD.ZMINO	005		T104L20B	(209)	T304RD0B	(009)	F304LE0	(010)	F104R80	(206)
ZER	CLEAR THE ERROR REGISTER	MD.ZERO	304		T104L20B	(209)	T304LB0B	(310)	F304LE0	(010)	F104R80	(206)
IDLMCH	IDLE THE MCH	MDIDMCHO	204		T304LD0	(100)	T104R80	(110)	F304LD0	(006)	F104R80	(206)
TMCH	TEST THE MCH	MDTMCHO	004		T104L1DB	(011)	T304RD0B	(009)	F304LD0	(006)	F104R80	(206)
HMRF	HARDWARE INITIALIZE THE 3A CC	MDMRFCCO	303		T104L20B	(209)	T304RD0B	(009)	F304LD0	(006)	F104R80	(206)
PYMCH	GATE BITS FROM BR TO MCHTR	MDPYMCHO	103		T104L20B	(209)	T304LB0B	(310)	F304LD0	(006)	F104R80	(206)

PART OF FS 1
COMPOSITE DIAGRAM 26

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	BIGY

PART OF FS 1

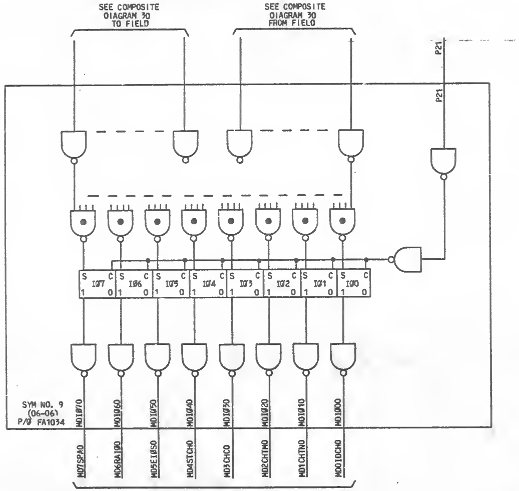
MICROCONTROL

CIRCUIT OPERATION

SEE COMPOSITE DIAGRAM 30 FOR A BRIEF DESCRIPTION OF MISCELLANEOUS DECODER FUNCTION. NOTE THAT THE I/0 MISCELLANEOUS DECODER CONTROL SIGNALS ARE PULSE STRETCHED TO PROVIDE IMPROVED TIMING MARGINS IN THE I/O.

COMPOSITE DIAGRAM 27

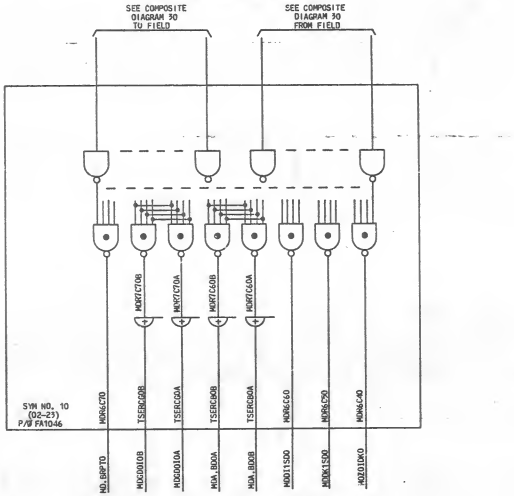
I/0 MISCELLANEOUS DECODER CONTROL



THESE 8 MISCELLANEOUS DECODER CROSSPOINTS ARE USED TO CONTROL THE 3ACC I/0 SERIAL CHANNELS AS WELL AS OTHER I/0 INTERFACES TO THE 3ACC (i.e. THE 2B I/0 UNIT, THE AUXILIARY PROCESSORS PARALLEL I/0, ETC.)

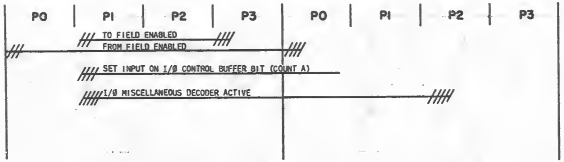
COMPOSITE DIAGRAM 28

MISCELLANEOUS DECODER CONTROL



COMPOSITE DIAGRAM 29

TIMING FOR I/0 MISCELLANEOUS DECODER CONTROL


P0
P1
P2
P3
P0
P1
P2
P3
TO FIELD ENABLED
FROM FIELD ENABLED
SET INPUT ON I/0 CONTROL BUFFER BIT (COUNT A)
I/0 MISCELLANEOUS DECODER ACTIVE

PART OF FS 1
COMPOSITE DIAGRAM 27, 28, 29

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	BIHA

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PART OF FS I

MICROCONTROL

COMPOSITE DIAGRAM 30

ASSIGNMENT OF MISCELLANEOUS DECODER CONTROL
(ASSOCIATED WITH I/O FUNCTIONS AND MISC.)

FUNCTION		FUNCTION OUTPUT			"TO FIELD"				"FROM FIELD"			
MNEMONIC	DESCRIPTION	NETNAME	(PIN NO.)			(PIN NO.)		(PIN NO.)		(PIN NO.)		(PIN NO.)
MD0 IDCH	IDLE I/O SERIAL CHANNEL	MD0IDCH0	(110)	FA1034 SYM NO. 9 (06-06)	T304LE0	(219)	T104R80	(019)	F204L30B	(316)	F204R60C	(217)
MD1 CHTN	LOAD R9 TO IOS (NORMAL)	M01CHTN0	(204)		T304LE0	(219)	T104R80	(019)	F204L30B	(316)	F204R90B	(108)
MD2 CHTM	LOAD R9 TO IOS (MAINTENANCE)	M02CHTM0	(318)		T304LE0	(219)	T104R80	(019)	F204L30B	(316)	F204RA0B	(210)
MD3 CHC	LOAD R9 TO IOS	MD3CHCD	(118)		T304LE0	(219)	T104R80	(019)	F204L30B	(316)	F204RC0C	(017)
M04 STCH	START I/O	MD4STCH0	(317)		T304L70	(201)	T104R80	(019)	F204L30B	(316)	F204R60C	(217)
MD5 EIO5	ENABLE IOS TO IOD	MD5EIOS0	(117)		T304L70	(201)	T104R80	(019)	F204L30B	(316)	F204R60C	(217)
MD6 RAIO	ENABLE R10 TO IOD	MD6RAIO0	(218)		T304L70	(201)	T104R80	(019)	F204L30B	(316)	F204RA0B	(210)
MD7 SPA	SPARE I/O CONTROL	MD7SPA0	(018)		T304L70	(201)	T104R80	(019)	F204L30B	(316)	F204RC0C	(017)
MD.BRPTO	GATE THE BR (15-8) TO TI (15-8) [UPT]	MD.BRPTO	(303)	FA1046 SYM NO.10(02-23)	T304LE0	(101)	T104R80	(301)	F204LC0B	(110)	F204R90E	(310)
MDOI1SD0	GATE OI1 TO SDR	MDOI1SD0	(003)		T304L70	(305)	T104R80	(301)	F204LC0B	(110)	F204R90B	(310)
MDDK1SD0	DKI TO SDR	MDDK1SD0	(102)		T304LB0	(001)	T104R80	(301)	F204LC0B	(110)	F204R90B	(310)
MOZDIDK0	CLEAR DI1 AND DK1	MDZ01DK0	(202)		T304LD0	(201)	T104R80	(301)	F204LC0B	(110)	F204R90B	(310)

PART OF FS 1
COMPOSITE DIAGRAM 30

3A CENTRAL CONTROL ②

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B1HB

PRINTED IN U.S.A.

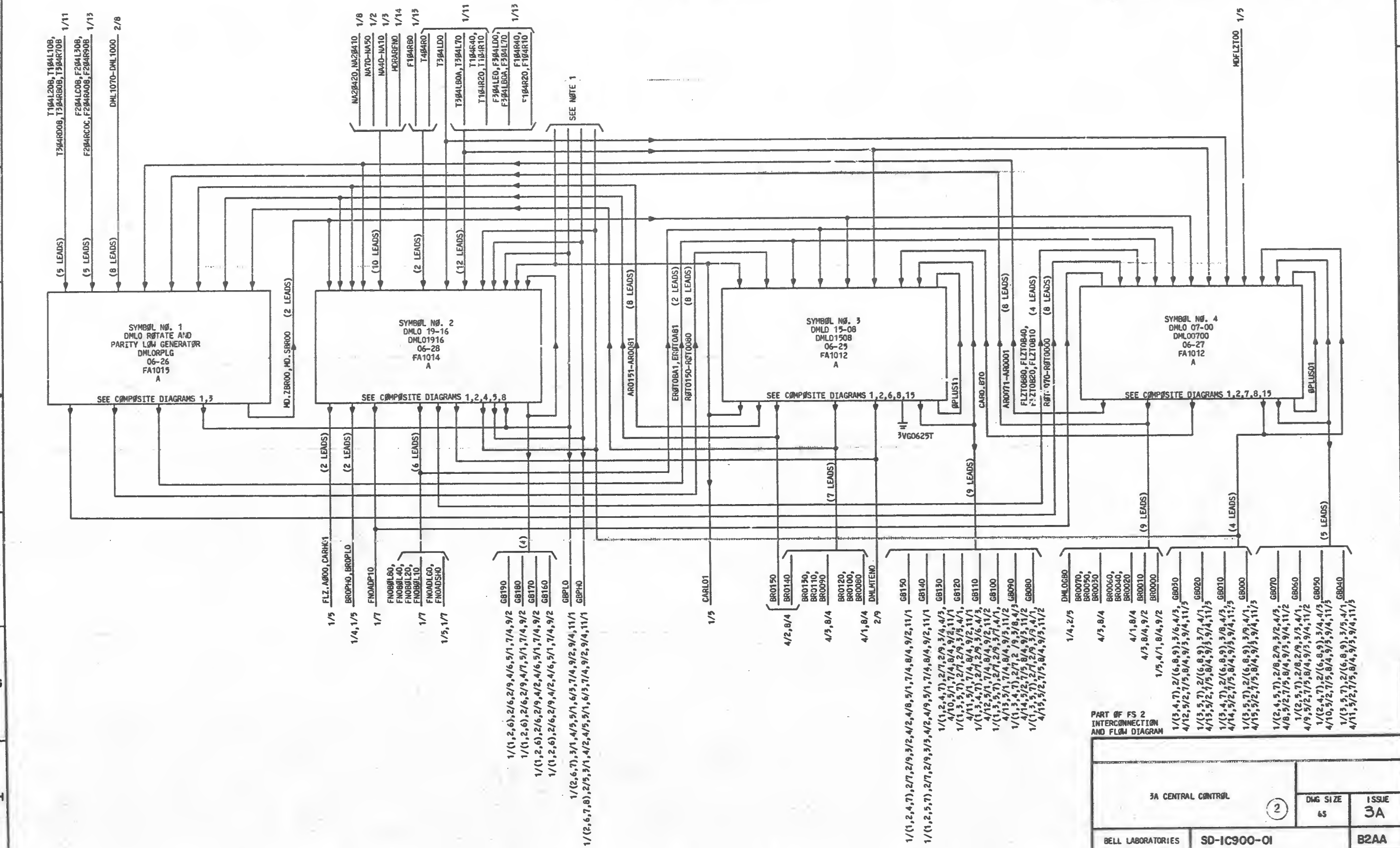
E-7431 (12-73)

PART OF FS 2

DATA MANIPULATIØN LØGIC (DML)
INTERCØNNECTIØN AND FLØW DIAGRAM

NØTES:

1. LEADS SHØWN CØULD FUNCTIØN AS EITHER ØUTPUTS ØR INPUTS (ØI). ALL ØFF-PAGE REFERENCING WILL BE SHØWN ØN ØUTPUT LEAD.
2. FØR "FRØM" FIELD AND "TØ" FIELD DECØDING ASSIGNMENTS SEE NØTE 312.


SYMBØL NØ. 1
DMLØ RØTATE AND PARITY LØW GENERATØR
DMLØRPLG
06-26
FA1015
A
SEE CØMPØSITE DIAGRAMS 1,5
SYMBØL NØ. 2
DMLØ 19-16
DML01916
06-28
FA1014
A
SEE CØMPØSITE DIAGRAMS 1,2,4,5,8
SYMBØL NØ. 3
DMLØ 15-08
DML01508
06-25
FA1012
A
SEE CØMPØSITE DIAGRAMS 1,2,6,8,15
SYMBØL NØ. 4
DMLØ 07-00
DML00700
06-27
FA1012
A
SEE CØMPØSITE DIAGRAMS 1,2,7,8,15
T1Ø4L20B,T1Ø4L10B, T3Ø4RD0B,T3Ø4RB0B,T3Ø4R70B 1/11
F2Ø4LC0B,F2Ø4L50B, F2Ø4RC0C,F2Ø4RA0B,F2Ø4R90B 1/13
DML1070-DML1000 2/8
NA2Ø420,NA2Ø410 1/8
NA70-NA50 1/2
NA40-NA10 1/3
MDRARFN0 1/14
F1Ø4RB0 1/13
T4Ø4R0
T3Ø4LD0 1/11
T3Ø4LB0A,T3Ø4L70
T1Ø4R40, T1Ø4R20,T1Ø4R10
F3Ø4LE0,F3Ø4LD0, F3Ø4LB0A,F3Ø4L70 1/13
F1Ø4R40, F1Ø4R20,F1Ø4R10
SEE NØTE 1
MDFLZT00 1/5
(5 LEADS)
(5 LEADS)
(8 LEADS)
(2 LEADS)
(10 LEADS)
(2 LEADS)
(12 LEADS)
MD.ZBR00,MD.SBR00
AR0151-AR0081
(8 LEADS)
ERØT0BA1,ERØT0A81
(2 LEADS)
RØT0150-RØT0080
(8 LEADS)
BPLUS11
CARD.B70
(9 LEADS)
AR0071-AR0001
(8 LEADS)
FLZT0880,FLZT0840, FLZT0820,FLZT0810
(4 LEADS)
RØT0070-RØT0000
(8 LEADS)
BPLUS01
3VG0625T
(2 LEADS)
(2 LEADS)
(6 LEADS)
(4)
(7 LEADS)
(9 LEADS)
(4 LEADS)
(5 LEADS)
FLZ.A000,CARH51 1/5
BRØPH0,BRØPL0 1/4,1/5
FNØADP10 1/7
FNØBØL80, FNØBØL40, FNØBØL20, FNØBØL10 1/7
FNØADLG0, FNØADSH0 1/5,1/7
GB190 1/(1,2,6),2/6,2/9,4/6,5/1,7/4,9/2
GB180 1/(1,2,6),2/6,2/9,4/7,5/1,7/4,9/2
GB170 1/(1,2,6),2/6,2/9,4/2,4/6,5/1,7/4,9/2
GB160 1/(1,2,6),2/6,2/9,4/2,4/6,5/1,7/4,9/2
GBPL0 1/(2,6,7),3/1,4/5,5/1,6/3,7/4,9/2,9/4,11/1
GBPH0 1/(2,6,7,8),2/5,3/1,4/2,4/5,5/1,6/3,7/4,9/2,9/4,11/1
CARL01 1/5
BR0150, BR0140 4/2,8/4
BR0130, BR0110, BR0090 4/3,8/4
BR0120, BR0100, BR0080 4/1,8/4
DMLMTEN0 2/9
GB150
GB140
GB130
GB120
GB110
GB100
GB090
GB080
DMLØGB0 1/4,2/5
BR0070, BR0050, BR0030 4/3,8/4
BR0060, BR0040, BR0020 4/1,8/4
BR0010, BR0000 4/3,8/4,9/2 1/5,4/1,8/4,9/2
GB030 1/(3,4,7),2/(6,8,9),3/6,4/3, 4/12,5/2,7/5,8/4,9/3,9/4,11/5
GB020 1/(3,5,7),2/(6,8,9),3/7,4/1, 4/13,5/2,7/5,8/4,9/3,9/4,11/5
GB010 1/(3,4,7),2/(6,8,9),3/8,4/3, 4/14,5/2,7/5,8/4,9/3,9/4,11/5
GB000 1/(3,5,7),2/(6,8,9),3/9,4/1, 4/15,5/2,7/5,8/4,9/3,9/4,11/5
GB070 1/(2,4,5,7),2/8,2/9,3/2,4/3, 4/8,5/2,7/5,8/4,9/3,9/4,11/2
GB060 1/(2,5,7),2/8,2/9,3/3,4/1, 4/9,5/2,7/5,8/4,9/3,9/4,11/2
GB050 1/(2,4,7),2/(6,8,9),3/4,4/3, 4/10,5/2,7/5,8/4,9/3,9/4,11/5
GB040 1/(3,5,7),2/(6,8,9),3/5,4/1, 4/11,5/2,7/5,8/4,9/3,9/4,11/5

PART ØF FS 2
INTERCØNNECTIØN
AND FLØW DIAGRAM

3A CENTRAL CØNTRØL ②

DWG SIZE	ISSUE
65	3A

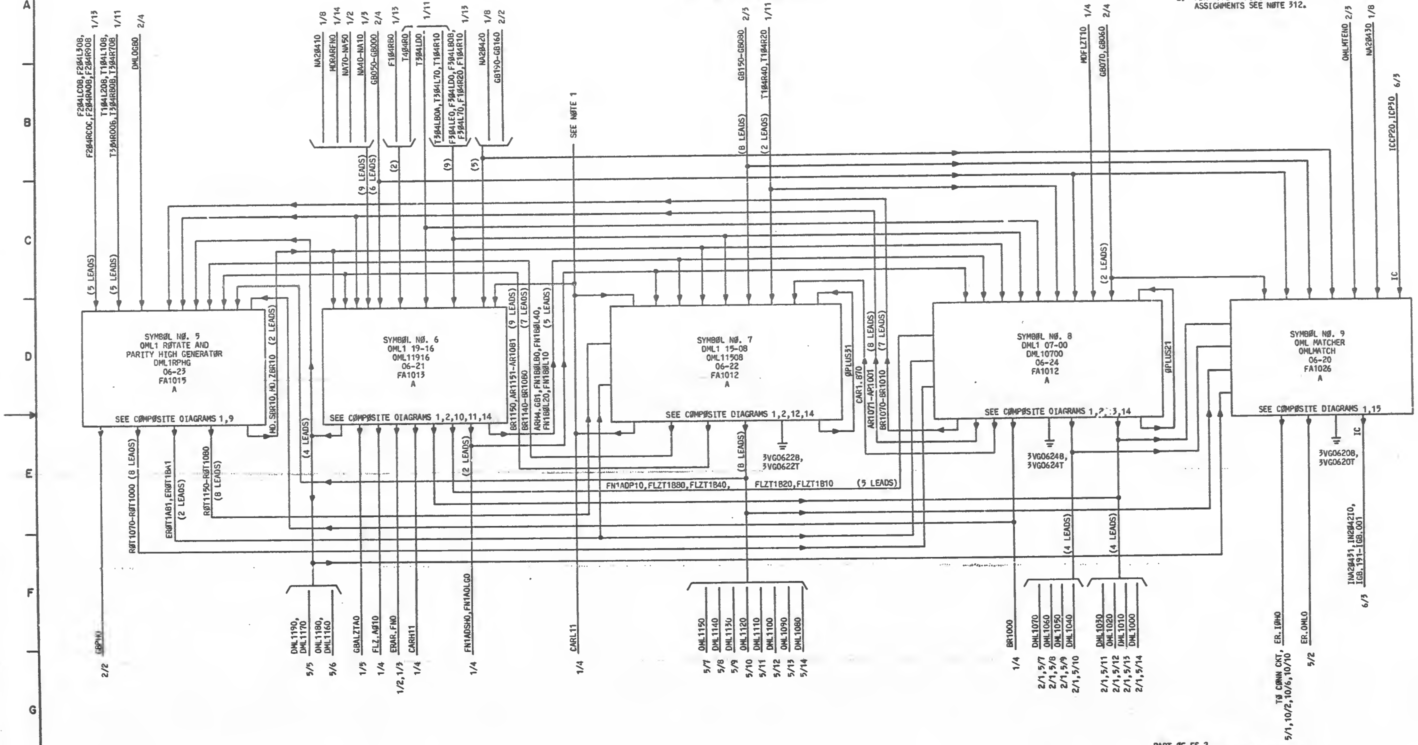
BELL LABØRATØRIES | SD-1C900-01 | B2AA

PART OF FS 2

DATA MANIPULATIØN LØGIC (DML)
INTERCØNNECTIØN AND FLØW DIAGRAM

NØTES:

1. LEADS SHØWN CØULD FUNCTIØN AS EITHER ØUTPUTS ØR INPUTS (3T). ALL ØFF-PAGE REFERENCING WILL BE SHØWN ØN ØUTPUT LEADS.
2. FØR "FRØM" FIELD AND "TØ" FIELD DECØDING ASSIGNMENTS SEE NØTE 312.



PART ØF FS 2
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL ②	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B2AB

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E - 7021 (12 - 73)

PART OF FS 2

DATA MANIPULATION LOGIC (DML)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ARH4.GB1	ENABLE HIGH 4 BITS (16-19) OF AR TO THE GATING BUS
AR0001-AR0151	BITS 0-15 OF THE AR REGISTER (COPY 0)
AR1001-AR1151	BITS 0-15 OF THE AR REGISTER (COPY 1)
BROPH0	PARITY HIGH OF THE BR REGISTER (COPY 0)
BROPL0	PARITY LOW OF THE BR REGISTER (COPY 0)
BR0000-BR0150	BITS 0-15 OF THE BR REGISTER (COPY 0)
BR1000-BR1150	BITS 0-15 OF THE BR REGISTER (COPY 1)
CARH01	CARRY HIGH FROM DML (COPY 0)
CARH11	CARRY HIGH FROM DML (COPY 1)
CARL01	CARRY LOW FROM DML (COPY 0)
CARL11	CARRY LOW FROM DML (COPY 1)
CAR0.B70	CARRY FROM BIT 7 DML (COPY 0)
CAR1.B70	CARRY FROM BIT 7 DML (COPY 1)
DMLMTEN0	DML MATCH ENABLE
DML0GB0	DML TO THE GB (COPY 0)
DML1GB0	DML TO THE GB (COPY 1)
DML1000-DML1190	BITS 0-19 OF DML (COPY 1)
ER.DML0	DML MATCH ERROR
ER.IOH0	I/O CHANNEL ERROR (I/O DML MATCH ERROR, I/O SUBCHANNEL OR I/O CONTROL STATES ERROR)
ERAR.FN0	ENABLE RAR TO THE FUNCTION REGISTER
EROT0AB1	ENABLE ROTATE OF REGISTER A TO REGISTER B (COPY 0)
EROT0BA1	ENABLE ROTATE OF REGISTER B TO REGISTER A (COPY 0)
EROT1AB1	ENABLE ROTATE A REGISTER TO BE REGISTER (COPY 1)
EROT1BA1	ENABLE ROTATE A REGISTER TO B REGISTER (COPY 1)
FLZ.A000	ALL ONES FOUND IN A FIND LOW ZERO'S TEST (COPY 0)
FLZ.A010	ALL ONES FOUND IN A FIND LOW ZERO'S TEST (COPY 1)
FLZT0B(1,2,4,8)0	FIND LOW ZERO TEST, BITS 1, 2, 4 AND 8 (COPY 0)
FLZT1B(1,2,4,8)0	FIND LOW ZERO TEST, BITS 1, 2, 4 AND 8 (COPY 1)
FN0ADLG0	ADD LONG BIT OF THE FUNCTION REGISTER (COPY 0)
FN0ADP10	ADD + 1 BIT OF THE FUNCTION REGISTER (COPY 0)
FN0ADSH0	ADD SHORT BIT OF FUNCTION REGISTER (COPY 0)
FN0BOL(1,2,4,8)0	BOOLEAN BITS 1, 2, 4, 8 OF THE FUNCTION REGISTER (COPY 0)
FN1ADLG0	ADD LONG BIT OF FUNCTION REGISTER (COPY 1)
FN1ADP10	ADD + 1 BIT OF FUNCTION REGISTER (COPY 1)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
FN1ADSH0	ADD SHORT BIT OF FUNCTION REGISTER (COPY 1)
FN1BOL(1,2,4,8)0	BOOLEAN BITS 1, 2, 4, 8, OF FUNCTION REGISTER (COPY 1)
GBALZTA0	GATING BUS ALL ZEROS TEST PART A (COPY 0)
GBPH0	PARITY HIGH OF THE GATING BUS
GBPL0	PARITY LOW OF THE GATING BUS
GB000-GB190	BITS 0-19 OF THE GATING BUS
ICCP20	P2 CLOCK PHASE [IC]
ICP30	CLOCK PHASE P30 [IC]
IGB.001-IGB.191	OUTPUTS OF GATING BUS BITS 0-19 [IC]
INA20431	2 OUT OF 4 AUXILIARY DECODER CONTROL BIT 3 [IC]
IN204210	2 OUT OF 4 AUXILIARY DECODER CONTROL BIT 2 [IC]
MD.SBR00	MISC. DECODER, SET BR REGISTER TO 1'S (COPY 0)
MD.SBR10	MISC. DECODER, SET BR REGISTER TO 1'S (COPY 1)
MD.ZBR00	MISC. DECODER, ZERO BR REGISTER (COPY 0)
MD.ZBR10	MISC. DECODER, ZERO BR REGISTER (COPY 1)
MDFLZT00	MISC. DECODER, ENABLE FIND LOW 0 TEST (COPY 0)
MDFLZT10	MISC. DECODER, ENABLE FIND LOW 0 TEST (COPY 1)
MDRARFN0	MISC. DECODER, GATE THE RAR TO THE FUNCTION REGISTER
NA10	BIT 1 OF THE NEXT ADDRESS FIELD OF THE MIR
NA20410-NA20430	OUTPUTS OF THE 2 OUT OF 4 AUXILIARY DECODER ATTACHED TO BITS 9 TO 11 AT THE MIR NEXT ADDRESS FIELD
NA20-NA70	BITS 2-7 OF THE NEXT ADDRESS FIELD OF THE MIR
OPLUS01-OPLUS31	PULL UP RESISTOR NET
ROT0000-ROT0150	ROTATE BUS BITS 0-15 OF DML (COPY 0)
ROT1000-ROT1150	ROTATE BUS BITS 0-15 AT DML (COPY 1)

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B2AC

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PART OF FS 2

DATA MANIPULATION LOGIC(DML)

SYMBOL NO. 1

DMLO ROTATE AND
PARITY LOW GENERATOR

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DMLORPLG	06-26	FA1015	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		017			OML110	2A1
		117			OML090	2A2
		217			OML100	2A1
		317			OML080	2A3
AR0001	I	302	2/4		AR0011	4A7
AR0011	I	303	2/4		AR0111	4A5
AR0021	I	318	2/4		AR0211	4A3
AR0031	I	315	2/4		AR0311	4A1
AR0041	I	202	2/4		AR0411	4A8
AR0051	I	203	2/4		AR0511	4A6
AR0061	I	218	2/4		AR0611	4A3
AR0071	I	219	2/4		AR0711	4A1
AR0081	I	002	2/3		AR0811	4A8
AR0091	I	003	2/3		AR0911	4A6
AR0101	I	018	2/3		AR1011	4A4
AR0111	I	019	2/3		AR1111	4A2
AR0121	I	102	2/3		AR1211	4A7
AR0131	I	103	2/3		AR1311	4A5
AR0141	I	118	2/3		AR1411	4A2
AR0151	I	115	2/3		AR1511	4A0
BR0000	I	306	2/4	202	BR000	11A6
BR0010	I	206	2/4	202	BR010	11A4
BR0020	I	207	2/4	202	BR020	11A2
BR0030	I	308	2/4	202	BR030	11A1
BR0040	I	307	2/4	202	BR040	10A6
BR0050	I	209	2/4	202	BR050	10A4
BR0060	I	208	2/4	202	BR060	10A2
BR0070	I	309	2/4	202	BR070	10A1
BR0080	I	107	2/3	202	BR080	9A6
BR0090	I	009	2/3	202	BR090	9A4
BR0100	I	008	2/3	202	BR100	9A2
BR0110	I	109	2/3	202	BR110	9A1
BR0120	I	108	2/3	202	BR120	8A6
BR0130	I	006	2/3	202	BR130	8A4
BR0140	I	007	2/3	202	BR140	8A2
BR0150	I	106	2/3	202	BR150	8A1
OMLOGBO	I	316	2/4	202	OML.GBOA	2A0
DML1000	I	215	2/8	202	OML000	2A8
OML1010	I	113	2/8	202	DML010	2A8
OML1020	I	213	2/8	202	OML020	2A7
OML1030	I	013	2/8	202	OML030	2A6
OML1040	I	312	2/8	202	OML040	2A6
OML1050	I	112	2/8	202	OML050	2A5
OML1060	I	212	2/8	202	OML060	2A4
OML1070	I	011	2/8	202	OML070	2A3
EROTOAB1	0	300	2/3,2/4		ROTA.B1	3H5
EROTOBA1	0	100	2/3,2/4		ROTB.A1	3H1
F204LC0B	I	114	1/13		F204LC0	3A3
F204L30B	I	313	1/13		F204L30	3A4
F204RA0B	I	314	1/13		F204RA0	3A3
F204RC0C	I	014	1/13		F204RC0	3A4
F204R90B	I	214	1/13		F204R90	3A4
GBPL0	OT	101	2/2		PL.PH0	2H1
MD.SBR00	0	201	2/2,2/3 2/4		SET.BR0	3H3
MD.2BR00	0	001	2/2,2/3 2/4		CLR.BR0	3H4
ROT0000	0	204	2/4		TROW.000	11G8
ROT0010	0	305	2/4		TROW.010	11G6

SYMBOL NO. 1 (CONT)

OMLO ROTATE AND
PARITY LOW GENERATOR

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
OMLORPLG	06-26	FA1015	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ROT0020	0	310	2/4		TROW.020	11G4
ROT0030	0	311	2/4		TROW.030	11G2
ROT0040	0	304	2/4		TROW.040	10G8
ROT0050	0	205	2/4		TROW.050	10G6
ROT0060	0	210	2/4		TROW.060	10G4
ROT0070	0	211	2/4		TROW.070	10G2
ROT0080	0	004	2/3		TROW.080	9G8
ROT0090	0	005	2/3		TROW.090	9G6
ROT0100	0	010	2/3		TROW.100	9G4
ROT0110	0	111	2/3		TROW.110	9G2
ROT0120	0	104	2/3		TROW.120	8G8
ROT0130	0	105	2/3		TROW.130	8G6
ROT0140	0	110	2/3		TROW.140	8G4
ROT0150	0	012	2/3		TROW.150	8G2
T104L10B	I	116	1/11		T104L10	3A2
T104L20B	I	301	1/11		T104L20	3A0
T304RB0B	I	016	1/11		T304RB0	3A1
T304R00B	I	216	1/11		T304R00	3A2
T304R70B	I	015	1/11		T304R70	3A0
3T062A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V062A	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 2

OMLO 19-16

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML01916	06-28	FA1014	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
AR0001	I	202	2/4		ARBT011	8A8
AR0011	I	002	2/4		ARBT111	8A8
AR0021	I	301	2/4		ARBT211	8A7
AR0031	I	101	2/4		ARBT311	8A6
AR0041	I	207	2/4		ARBT411	8A4
AR0051	I	001	2/4		ARBT511	8A3
AR0061	I	300	2/4		ARBT611	8A3
AR0071	I	100	2/4		ARBT711	8A2
AR0081	I	008	2/3		ARBT811	9A8
AR0091	I	307	2/3		ARBT911	9A8
AR0101	I	107	2/3		ARBT1011	9A7
AR0111	I	207	2/3		ARBT1111	9A7
AR0121	I	007	2/3		ARBT1211	9A4
AR0131	I	306	2/3		ARBT1311	9A4
AR0141	I	106	2/3		ARBT1411	9A3
AR0151	I	206	2/3		ARBT1511	9A3
BRPH0	0	208	1/4,1/5	202	BRPH0	4H1
BRPL0	0	108	1/4,1/5	202	BRPL0	4H1

SYMBOL NO. 2 (CONT)

OMLO 19-16

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML01916	06-28	FA1014	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
BR0150	I	214	2/3	202	BR150	4A6
CARH01	0	011	1/5		CCAR191	5H0
CARL01	I	215	2/3		CCAR1511	5A8
OMLMTEN0	OT	211	2/3		OMLR.GB0	6H3
FLZ.A000	0	210	1/5		TALLOT0	9H1
FLZT0B10	0	109	2/4		FLZTB10	8H3
FLZT0B20	0	209	2/4		FLZTB20	8H3
FLZT0B40	0	009	2/4		FLZTB40	8H4
FLZT0B80	0	308	2/4		FLZTB80	9G9
FN0ADLG0	0	104	1/5,1/7 2/3,2/4		ADDLG0A	7H5
FN0ADP10	0	005	1/7,2/4		ADDP10	7H7
FN0ADSH0	0	304	1/5,1/7 2/3,2/4		ADDSH0	7H5
FN0BOL10	0	305	1/7,2/3 2/4		BOOLFN10	7H4
FN0BOL20	0	006	1/7,2/3 2/4		BOOLFN20	7H3
FN0BOL40	0	105	1/7,2/3 2/4		BOOLFN40	7H2
FN0BOL80	0	205	1/7,2/3 2/4		BOOLFN80	7H2
F104R10	I	113	1/13		F104R10	6A3
F104R20	I	014	1/13		F104R20	6A1
F104R40	I	013	1/13		F104R40	6A5
F104R80	I	312	1/13		F104R80	3A2
F304LB0A	I	311	1/13		F304LB0	6A2
F304LD0	I	112	1/13		F304L00B	6A3
	I	114	1/13		F304L00A	6A2
F304LE0	I	213	1/13		F304LE0	6A1
F304L70	I	314	1/13		F304L70	6A2
GBPH0	OI	309	1/2,1/6 1/7,2/5 3/1,4/2 4/5,5/1 7/4,9/2 9/4,11/1 1/8,3/1 4/5,6/3		TDMLGPH0	6H4
GBPL0	OI	010	1/2,1/6 1/7,2/1 3/1,4/5 5/1,7/4 9/2,9/4 11/1 3/1,4/5 6/3		TDMLGPL0	6H5
GB000	OI	015	2/4		AR16LGB0	3H4
GB010	OI	216	2/4		AR17LGB0	3H3
GB020	OI	018	2/4		AR18LGB0	3H3
GB030	OI	218	2/4		AR19LGB0	3H3
GB160	OT	317	1/1,1/2 1/6,4/2 4/7,5/1 7/4,9/2		OMLGB160	6H8
	I		2/6,2/9			
	I	118	2/2		GB.1610	4A8
GB170	OT	017	1/1,1/2 1/6,4/2 4/6,5/1 7/4,9/2		DMLGB170	6H8
	I		2/6,2/9			
	I	318	2/2		GB.1710	4A8
GB180	OT	217	1/1,1/2 1/6,4/7 5/1,7/4 9/2		OMLGB180	6H6
	I		2/6,2/9			

SYMBOL NO. 2 (CONT)

OMLO 19-16

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML01916	06-28	FA1014	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
GB180	I	019	2/2		GB.1810	4A7
GB190	OT	117	1/1,1/2 1/6,4/6 5/1,7/4 9/2		DMLGB190	6H6
	I		2/6,2/9			
	I	219	2/2		GB.1910	4A3
MD.SBR00	I	110	2/1		SETBR10	4A6
MD.2BR00	I	310	2/1		CLRBR10	4A5
MORARFN0	I	103	1/14		RAR.FN10	7A1
NA10	I	303	1/3		NA.10	7A7
NA20410	I	212	1/8		NA20410	7A0
NA20420	I	012	1/8		NA20420	7A0
NA20	I	004	1/3	202	NA.20	7A5
NA30	I	204	1/3	202	NA.30	7A5
NA40	I	003	1/3	202	NA.40	7A4
NA50	I	203	1/2	202	NA.50	7A3
NA60	I	102	1/2	202	NA.60	7A2
NA70	I	302	1/2	202	NA.70	7A2
T104R10	I	016	1/11		T104R10	2A1
T104R20	I	315	1/11		T104R20	2A1
T104R40	I	115	1/11		T104R40	2A0
T304LB0A	I	313	1/11		T304LB0	2A0
T304L00	I	316	1/11		T304L00	2A3
T304L70	I	116	1/11		T304L70	4A2
T404R0	I	111	1/11		TSTBR150	4A6
3T058F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V058F	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 2
SYMBOL(S) 1 2

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B2CA

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12/01/77

PART OF FS 2

OATA MANIPULATION LOGIC(OML)

SYMBOL NO. 3

OMLO 15-08

OESIG	EOPT LOC	COOE	ELEM IOENT	OPT
OML01508	06-25	FA1012	A	

LEAD OESIG	FUNC	TERM.	OESTINATION	NOTE	TERM. MOO	LOC
			FS INFO		CP INFO	
		007			CCAR70	8H1
		016			FLZB20	6A7
		017			FLZB80	6A4
		018			FLZBINI0	[illegible]
		315			FLZB00	6A9
		316			FLZB40	6A6
AR0081	0	105	2/1,2/2		ARB01	5H9
AR0091	0	011	2/1,2/2		ARB11	5H8
AR0101	0	305	2/1,2/2		ARB21	5H6
AR0111	0	211	2/1,2/2		ARB31	5H5
AR0121	0	202	2/1,2/2		ARB41	5H4
AR0131	0	210	2/1,2/2		ARB51	5H3
AR0141	0	302	2/1,2/2		ARB61	5H2
AR0151	0	308	2/1,2/2		ARB71	5H1
BR0080	0	113	2/1,4/1 8/4	202	BRB00	6H8
BR0090	0	107	2/1,4/3 8/4	202	BRB10	6H8
BR0100	0	313	2/1,4/1 8/4	202	BRB20	6H6
BR0110	0	304	2/1,4/3 8/4	202	BRB30	6H5
BR0120	0	009	2/1,4/1 8/4	202	BRB40	6H4
BR0130	0	101	2/1,4/3 8/4	202	BRB50	6H3
BR0140	0	209	2/1,4/2 8/4	202	BRB60	6H2
BR0150	0	004	2/1,2/2 4/2,8/4	202	BRB70	6H2
CARL01	0I	207	1/5,2/2		CCAR71	8H1
CAR0.B70	I	114	2/4		ADOPI10	7A0
OMLMTEN0	OT	310	2/2		OML.GB0	3H2
	I		2/9			
EROT0AB1	I	216	2/1		ROTA.B1	2A7
EROT0BA1	I	309	2/1		ROTB.A1	2A2
FN0ADLG0	I	217	2/2		ADOLGI0	7A1
FN0ADSH0	I	117	2/2		ADOSHI0	7A2
FN0BOL10	I	314	2/2		BOLI100	7A3
FN0BOL20	I	015	2/2		BOLI200	7A4
FN0BOL40	I	215	2/2		BOLI400	7A5
FN0BOL80	I	115	2/2		BOLI800	7A6
F104R10	I	111	1/13		F104R10	3A1
F104R20	I	214	1/13		F104R20	3A1
F104R40	I	012	1/13		F104R40	3A0
F304LB0A	I	112	1/13		F304LB0B	3A2
	I	311	1/13		F304LB0A	3A0
F304LD0	I	312	1/13		F304L00	3A2
F304LE0	I	014	1/13		F304LE0	3A1
F304L70	I	212	1/13		F304L70	3A2
GB080	OT	110	1/1,1/3 1/5,1/7 3/9,4/1 4/15,5/2 7/5,8/4 9/3,11/2		OML.GB00	3H8
	I		2/7,2/9 3/9,4/15			
	I	006	2/3		GB0010	4A8
GB090	OT	108	1/1,1/3 1/4,1/7 3/8,4/3 4/14,5/2 7/5,8/4 9/3,11/2		OML.GB10	3H7
	I		2/7,2/9 3/8,4/14			

SYMBOL NO. 3 (CONT)

OMLO 15-08

OESIG	EQPT LOC	COOE	ELEM IOENT	OPT
OML01508	06-25	FA1012	A	

LEAD OESIG	FUNC	TERM.	OESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
GB090	I	106	2/3		GB0110	4A7
GB100	OT	208	1/1,1/3 1/5,1/7 3/7,4/1 4/13,5/1 7/4,8/4 9/3,11/2		OML.GB20	3H7
	I		2/7,2/9 3/7,4/13			
	I	307	2/3		GB0210	4A6
GB110	OT	100	1/1,1/3 1/4,1/7 3/6,4/3 4/12,5/1 7/4,8/4 9/2,11/2		OML.GB30	3H6
	I		2/7,2/9 3/6,4/12			
	I	205	2/3		GB0310	4A5
GB120	OT	001	1/1,1/3 1/5,1/7 3/5,4/1 4/11,5/1 7/4,8/4 9/2,11/1		OML.GB40	3H5
	I		2/7,2/9 3/5,4/11			
	I	002	2/3		GB0410	4A4
GB130	OT	201	1/1,1/2 1/4,1/7 3/4,4/3 4/10,5/1 7/4,8/4 9/2,11/1		OML.GB50	3H4
	I		2/7,2/9 3/4,4/10			
	I	003	2/3		GB0510	4A3
GB140	OT	013	1/1,1/2 1/5,1/7 3/3,4/2 4/9,5/1 7/4,8/4 9/2,11/1		OML.GB60	3H4
	I		2/7,2/9 3/3,4/9			
	I	103	2/3		GB0610	4A2
GB150	OT	213	1/1,1/2 1/4,1/7 3/2,4/2 4/8,5/1 7/4,8/4 9/2,11/1		DML.GB70	3H3
	I		2/7,2/9 3/2,4/8			
	I	204	2/3		GB0710	4A1
MD.SBR00	I	317	2/1		BRSETI0	2A8
MD.ZBR00	I	218	2/1		BRCLRI0	2A8
OPLUS11	0	300			OPLUS1	2H0
	I	010			T304LD0	2A4
	I	102			OGRD0	2A3
ROT0080	I	206	2/1		A.BRT000	4A8
ROT0090	I	306	2/1		A.BRT010	4A7
ROT0100	I	008	2/1		A.BRT020	4A6
ROT0110	I	005	2/1		A.BRT030	4A5
ROT0120	I	301	2/1		A.BRT040	4A4
ROT0130	I	203	2/1		A.BRT050	4A3
ROT0140	I	303	2/1		A.BRT060	4A2
ROT0150	I	104	2/1		A.BRT070	4A1
T104R10	I	318	1/11		T104R10	2A1
T104R20	I	019	1/11		T104R20	2A1

SYMBOL NO. 3 (CONT)

OMLO 15-08

OESIG	EOPT LOC	COOE	ELEM IOENT	OPT
OML01508	06-25	FA1012	A	

LEAD OESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOO	LOC
			FS INFO		CP INFO	
T104R40	I	219	1/11		T104R40	2A1
T304LB0A	I	109	1/11		T304LB0	2A0
T304L70	I	118	1/11		T304L70	2A5
3T062A	GRD	0G0		203	~~GRD~~	
	GRD	2G0		203	GRD	
	GRO	200		203	GRO	
	GRO	319		203	GRD	
3VG0625T	I	116			BLK840	2A5
	GRO	319			GRD	
3V062A	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 4

DMLO 07-00

OESIG	EOPT LOC	CODE	ELEM IOENT	OPT
DML00700	06-27	FA1012	A	

LEAD OESIG	FUNC	TERM.	OESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
		207			CCAR71	8H1
AR0001	0	105	2/1,2/2		ARB01	5H9
AR0011	0	011	2/1,2/2		ARB11	5H8
AR0021	0	305	2/1,2/2		ARB21	5H6
AR0031	0	211	2/1,2/2		ARB31	5H5
AR0041	0	202	2/1,2/2		ARB41	5H4
AR0051	0	210	2/1,2/2		ARB51	5H3
AR0061	0	302	2/1,2/2		ARB61	5H2
AR0071	0	308	2/1,2/2		ARB71	5H1
BR0000	0	113	1/5,2/1 4/1,8/4 9/2	202	BRB00	6H8
BR0010	0	107	2/1,4/3 8/4,9/2	202	BRB10	6H8
BR0020	0	313	2/1,4/1 8/4	202	BRB20	6H6
BR0030	0	304	2/1,4/3 8/4	202	BRB30	6H5
BR0040	0	009	2/1,4/1 8/4	202	BRB40	6H4
BR0050	0	101	2/1,4/3 8/4	202	BRB50	6H3
BR0060	0	209	2/1,4/1 8/4	202	BRB60	6H2
BR0070	0	004	2/1,4/3 8/4	202	BRB70	6H2
CAR0.B70	0	007	2/3		CCAR70	8H1
DMLOGB0	0	310	1/4,2/1 2/5	202	DML.GB0	3H2
EROT0AB1	I	216	2/1		ROTA.B1	2A7
EROT0BA1	I	309	2/1		ROTB.A1	2A2
FL2T0B10	I	315	2/2		FLZB00	6A9
FL2T0B20	I	016	2/2		FLZB20	6A7
FL2T0B40	I	316	2/2		FLZB40	6A6
FL2T0B80	I	017	2/2		FLZB80	6A4
FN0ADLG0	I	217	2/2		ADOLGI0	7A1
FN0ADP10	I	114	2/2		ADDPI10	7A0

SYMBOL NO. 4 (CONT)

OMLO 07-00

DESIG	EOPT LOC	CODE	ELEM IOENT	OPT
DML00700	06-27	FA1012	A	

LEAD OESIG	FUNC	TERM.	OESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
FN0ADSH0	I	117	2/2		ADOSHI0	7A2
FN0BOL10	I	314	2/2		BOLI100	7A3
FN0BOL20	I	015	2/2		BOLI200	7A4
~~FN0BOL40~~	~~I~~	~~215~~	2/2		BOLI400	7A5
FN0BOL80	I	115	2/2		BOLI800	7A6
F104R10	I	111	1/13		F104R10	3A1
F104R20	I	214	1/13		F104R20	3A1
F104R40	I	012	1/13		F104R40	3A0
F304LB0A	I	112	1/13		F304LB0B	3A2
	I	311	1/13		F304LB0A	3A0
F304L00	I	312	1/13		F304L00	3A2
F304LE0	I	014	1/13		F304LE0	3A1
F304L70	I	212	1/13		F304L70	3A2
GB000	OT	110	1/3,1/5 1/7,2/2 3/9,4/1 4/15,5/2 7/5,8/4 9/3,9/4 11/3		OML.GB00	3H8
	I		2/6,2/8 2/9,3/9 4/15			
	I	006	2/4		GB0010	4A8
GB010	OT	108	1/3,1/4 1/7,2/2 3/8,4/3 4/14,5/2 7/5,8/4 9/3,9/4 11/3		OML.GB10	3H7
	I		2/6,2/8 2/9,3/8 4/14			
	I	106	2/4		GB0110	4A7
GB020	OT	208	1/3,1/5 1/7,2/2 3/7,4/1 4/13,5/2 7/5,8/4 9/3,9/4 11/3		OML.GB20	3H7
	I		2/6,2/8 2/9,3/7 4/13			
	I	307	2/4		GB0210	4A6
GB030	OT	100	1/3,1/4 1/7,2/2 3/6,4/3 4/12,5/2 7/5,8/4 9/3,9/4 11/3		DML.GB30	3H6
	I		2/6,2/8 2/9,3/6 4/12			
	I	205	2/4		GB0310	4A5
GB040	OT	001	1/3,1/5		DML.GB40	3H5

PART OF FS 2

SYMBOL(S) 3 4

3A CENTRAL CONTROL	OWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	82CB

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PART OF FS 2

DATA MANIPULATION LOGIC(DML)

SYMBOL NO. 4 (CONT)

DML0 07-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML00700	06-27	FA1012	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			1/7,3/5			
			4/1,4/11			
			5/2,7/5			
			8/4,9/3			
			9/4,11/3			
	I		2/6,2/8			
			2/9,3/5			
			4/11			
	I	002	2/4		GB0410	4A4
GB050	OT	201	1/2,1/4		DML.GB50	3H4
			1/7,3/4			
			4/3,4/10			
			5/2,7/5			
			8/4,9/3			
			9/4,11/3			
	I		2/6,2/8			
			2/9,3/4			
			4/10			
	I	003	2/4		GB0510	4A3
GB060	OT	013	1/2,1/5		DML.GB60	3H4
			1/7,3/3			
			4/1,4/9			
			5/2,7/5			
			8/4,9/3			
			9/4,11/2			
	I		1/5,2/8			
			2/9,3/3			
			4/9			
	I	103	2/4		GB0610	4A2
GB070	OT	213	1/2,1/4		DML.GB70	3H3
			1/7,3/2			
			4/3,4/8			
			5/2,7/5			
			8/4,9/3			
			9/4,11/2			
	I		1/5,2/8			
			2/9,3/2			
			4/8			
	I	204	2/4		GB0710	4A1
MD.SBR00	I	317	2/1		BRSET10	2A8
MD.2BR00	I	218	2/1		BRCLR10	2A8
MDFL2T00	I	018	1/5		FL2BIN10	2A9
OPLUS01	0	300			OPLUS1	2H0
	I	102			0GRD0	2A3
	I	116			BLK840	2A5
ROT0000	I	206	2/1		A.BRT000	4A8
ROT0010	I	306	2/1		A.BRT010	4A7
ROT0020	I	008	2/1		A.BRT020	4A6
ROT0030	I	005	2/1		A.BRT030	4A5
ROT0040	I	301	2/1		A.BRT040	4A4
ROT0050	I	203	2/1		A.BRT050	4A3
ROT0060	I	303	2/1		A.BRT060	4A2
ROT0070	I	104	2/1		A.BRT070	4A1
T104R10	I	318	1/11		T104R10	2A1
T104R20	I	019	1/11		T104R20	2A1
T104R40	I	219	1/11		T104R40	2A1
T304LB0A	I	109	1/11		T304LB0	2A0
T304LD0	I	010	1/11		T304LD0	2A4
T304L70	I	118	1/11		T304L70	2A5
3T062A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V062A	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 5

DML1 ROTATE AND
PARITY HIGH GENERATOR

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML1RPHG	06-23	FA1015	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
AR1001	I	302	2/8		AR0011	4A7
AR1011	I	303	2/8		AR0111	4A5
AR1021	I	318	2/8		AR0211	4A3
AR1031	I	315	2/8		AR0311	4A1
AR1041	I	202	2/8		AR0411	4A8
AR1051	I	203	2/8		AR0511	4A6
AR1061	I	218	2/8		AR0611	4A3
AR1071	I	219	2/8		AR0711	4A1
AR1081	I	002	2/7		AR0811	4A8
AR1091	I	003	2/7		AR0911	4A6
AR1101	I	018	2/7		AR1011	4A4
AR1111	I	019	2/7		AR1111	4A2
AR1121	I	102	2/7		AR1211	4A7
AR1131	I	103	2/7		AR1311	4A5
AR1141	I	118	2/7		AR1411	4A2
AR1151	I	115	2/7		AR1511	4A0
BR1000	I	306	2/8	202	BR000	11A6
BR1010	I	206	2/8	202	BR010	11A4
BR1020	I	207	2/8	202	BR020	11A2
BR1030	I	308	2/8	202	BR030	11A1
BR1040	I	307	2/8	202	BR040	10A6
BR1050	I	209	2/8	202	BR050	10A4
BR1060	I	208	2/8	202	BR060	10A2
BR1070	I	309	2/8	202	BR070	10A1
BR1080	I	107	2/7	202	BR080	9A6
BR1090	I	009	2/7	202	BR090	9A4
BR1100	I	008	2/7	202	BR100	9A2
BR1110	I	109	2/7	202	BR110	9A1
BR1120	I	108	2/7	202	BR120	8A6
BR1130	I	006	2/7	202	BR130	8A4
BR1140	I	007	2/7	202	BR140	8A2
BR1150	I	106	2/7	202	BR150	8A1
DML0GB0	I	316	2/4	202	DML.GB0A	2A0
DML1080	I	215	2/7	202	DML000	2A8
DML1090	I	113	2/7	202	DML010	2A8
DML1100	I	213	2/7	202	DML020	2A7
DML1110	I	013	2/7	202	DML030	2A6
DML1120	I	312	2/7	202	DML040	2A6
DML1130	I	112	2/7	202	DML050	2A5
DML1140	I	212	2/7	202	DML060	2A4
DML1150	I	011	2/7	202	DML070	2A3
DML1160	I	317	2/6	202	DML080	2A3
DML1170	I	117	2/6	202	DML090	2A2
DML1180	I	217	2/6	202	DML100	2A1
DML1190	I	017	2/6	202	DML110	2A1
EROT1AB1	0	300	2/7,2/8		ROTA.B1	3H5
EROT1BA1	0	100	2/7,2/8		ROTB.A1	3H1
F204LC0B	I	114	1/13		F204LC0	3A3
F204L30B	I	313	1/13		F204L30	3A4
F204RA0B	I	314	1/13		F204RA0	3A3
F204RC0C	I	014	1/13		F204RC0	3A4
F204R90B	I	214	1/13		F204R90	3A4
GBPH0	OT	101	2/2		PL.PH0	2H1
MD.SBR10	0	201	2/6,2/7		SET.BR0	3H3
			2/8			
MD.2BR10	0	001	2/6,2/7		CLR.BR0	3H4
			2/8			
ROT1000	0	204	2/8		TROW.000	11G8
ROT1010	0	305	2/8		TROW.010	11G6

SYMBOL NO. 5 (CONT)

DML1 ROTATE AND
PARITY HIGH GENERATOR

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML1RPHG	06-23	FA1015	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ROT1020	0	310	2/8		TROW.020	11G4
ROT1030	0	311	2/8		TROW.030	11G2
ROT1040	0	304	2/8		TROW.040	10G8
ROT1050	0	205	2/8		TROW.050	10G6
ROT1060	0	210	2/8		TROW.060	10G4
ROT1070	0	211	2/8		TROW.070	10G2
ROT1080	0	004	2/7		TROW.080	9G8
ROT1090	0	005	2/7		TROW.090	9G6
ROT1100	0	010	2/7		TROW.100	9G4
ROT1110	0	111	2/7		TROW.110	9G2
ROT1120	0	104	2/7		TROW.120	8G8
ROT1130	0	105	2/7		TROW.130	8G6
ROT1140	0	110	2/7		TROW.140	8G4
ROT1150	0	012	2/7		TROW.150	8G2
T104L10B	I	116	1/11		T104L10	3A2
T104L20B	I	301	1/11		T104L20	3A0
T304RB0B	I	016	1/11		T304RB0	3A1
T304R00B	I	216	1/11		T304R00	3A2
T304R70B	I	015	1/11		T304R70	3A0
3T062A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V062A	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 6

DML1 19-16

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML11916	06-21	FA1013	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ARH4.GB1	0	010	2/7,2/8		ARH4GB1	3G8
AR1001	I	202	2/8		ARBT011	8A6
AR1011	I	002	2/8		ARBT111	8A6
AR1021	I	301	2/8		ARBT211	8A5
AR1031	I	101	2/8		ARBT311	8A5
AR1041	I	201	2/8		ARBT411	8A1
AR1051	I	001	2/8		ARBT511	8A1
AR1061	I	300	2/8		ARBT611	8A1
AR1071	I	100	2/8		ARBT711	8A0
AR1081	I	008	2/7		ARBT811	9A7
AR1091	I	307	2/7		ARBT911	9A6
AR1101	I	107	2/7		ARBT1011	9A6
AR1111	I	207	2/7		ARBT1111	9A6
AR1121	I	007	2/7		ARBT1211	9A1
AR1131	I	306	2/7		ARBT1311	9A1
AR1141	I	106	2/7		ARBT1411	9A1
AR1151	I	206	2/7		ARBT1511	9A0
BR1150	I	111	2/7	202	BR150	4A1

SYMBOL NO. 6 (CONT)

DML1 19-16

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML11916	06-21	FA1013	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
CARH11	0	011	1/4		CCAR191	5H0
CARL11	I	215	2/7	202	CCAR1511	5A8
DML1000	OT	015	2/8	202	AR16LGB0	3H6
DML1010	OT	216	2/8	202	AR17LGB0	3H6
DML1020	OT	018	2/8	202	AR18LGB0	3H3
DML1030	OT	218	2/8	202	AR19LGB0	3H3
DML1160	0	317	2/5,2/9	202	DMLGB160	6H7
			5/6			
DML1170	0	017	2/5,2/9	202	DMLGB170	6H5
			5/5			
DML1180	0	217	2/5,2/9	202	DMLGB180	6H3
			5/6			
DML1190	0	117	2/5,2/9	202	DMLGB190	6H1
			5/5			
ERAR.FN0	0	309	1/2,1/3		RARFN0B0	7H1
FL2.AD10	0	210	1/4		TALLOT0	9H1
FL2T1B10	0	109	2/8		FL2TB10	8H2
FL2T1B20	0	209	2/8		FL2TB20	8H3
FL2T1B40	0	009	2/8		FL2TB40	8H4
FL2T1B80	0	308	2/8		FL2TB80	9H5
FN1ADLG0	0	104	1/4,2/7		ADDLGCA	7H6
			2/8			
FN1ADP10	0	005	2/8		ADDP10	7H8
FN1ADSH0	0	304	1/4,2/7		ADDSH0	7H7
			2/8			
FN1BOL10	0	305	2/7,2/8		BOOLFN10	7H5
FN1BOL20	0	006	2/7,2/8		BOOLFN20	7H5
FN1BOL40	0	105	2/7,2/8		BOOLFN40	7H4
FN1BOL80	0	205	2/7,2/8		BOOLFN80	7H3
F104R10	I	113	1/13		F104R10	6A1
F104R20	I	014	1/13		F104R20	6A2
F104R80	I	312	1/13		F104R80	3A8
F304LB0B	I	311	1/13		F304LB0	3A8
F304LD0	I	114	1/13		F304LD0A	6A1
F304LE0	I	213	1/13		F304LE0	6A1
F304L70	I	314	1/13		F304L70	6A1
GBAL2TA0	0	211	1/5		BALL2T0	2G8
GB000	I	013	2/4		GB.0010	2A8
GB010	I	214	2/4		GB.0110	2A7
GB020	I	115	2/4		GB.0210	2A6
GB030	I	315	2/4		GB.0310	2A5
GB040	I	112	2/4		GB.0410	2A4
GB050	I	108	2/4		GB.0510	2A4
GB160	I	118	2/2		GB.1610	2A3
GB170	I	318	2/2		GB.1710	2A2
GB180	I	019	2/2		GB.1810	2A1
GB190	I	219	2/2		GB.1910	2A0
MD.SBR10	I	110	2/5		SETBR10	4A2
MD.2BR10	I	310	2/5		CLRBR10	4A2
MDRARFN0	I	103	1/14		RAR.FN10	7A1
NA10	I	303	1/3		NA.10	7A8

PART OF FS 2
SYMBOL(S) 4 5 6

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	DWG SIZE C2	ISSUE 7D
			B2CC

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PART OF FS 2

DATA MANIPULATION LOGIC(DML)

SYMBOL NO. 6 (CONT)

DML1 19-16

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML11916	06-21	FA1013	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
NA20410	I	212	1/8		NA20410	7A2
NA20420	I	012	1/8		NA20420	7A2
NA20	I	004	1/3	202	NA.20	7A7
NA30	I	204	1/3	202	NA.30	7A7
NA40	I	003	1/3	202	NA.40	7A5
NA50	I	203	1/2	202	NA.50	7A5
NA60	I	102	1/2	202	NA.60	7A4
NA70	I	302	1/2	202	NA.70	7A3
T1D4R10	I	016	1/11		T1D4R10	3A1
T3D4L80A	I	313	1/11		T3D4L80	3A1
T3D4LD0	I	316	1/11		T3D4LD0	3A1
T3D4L70	I	116	1/11		T3D4L70	4A0
T4D4R0	I	208	1/11		TSTBR150	4A1
3T062B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V062A	PWR	000	14/8		+3	
	PWR	119	14/8		+3	
3V062B	PWR	000	(X)14/8	203	+3	
	PWR	119	(X)14/8	203	+3	

SYMBOL NO. 7

DML1 15-08

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML11508	06-22	FA1012	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			CCAR70	8H1
		016			FL2B20	6A7
		017			FL2B80	6A4
		018			FL2BINI0	2A9
		310			DML.GB0	3H2
		315			FL2B00	6A9
		316			FL2B40	6A6
ARH4.GB1	I	012	2/6		F1D4R40	3A0
AR1081	0	105	2/5,2/6		ARB01	5H9
AR1091	0	011	2/5,2/6		ARB11	5H8
AR1101	0	305	2/5,2/6		ARB21	5H6
AR1111	0	211	2/5,2/6		ARB31	5H5
AR1121	0	202	2/5,2/6		ARB41	5H4
AR1131	0	210	2/5,2/6		ARB51	5H3
AR1141	0	302	2/5,2/6		ARB61	5H2
AR1151	0	308	2/5,2/6		ARB71	5H1
BR1080	0	113	2/5	202	BRB00	6H8
BR1090	0	107	2/5	202	BRB10	6H8
BR1100	0	313	2/5	202	BRB20	6H6
BR1110	0	304	2/5	202	BRB30	6H5
BR1120	0	009	2/5	202	BRB40	6H4
BR1130	0	101	2/5	202	BRB50	6H3
BR1140	0	209	2/5	202	BRB60	6H2
BR1150	0	004	2/5,2/6	202	BRB70	6H2

SYMBOL NO. 7 (CONT)

DML1 15-08

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML11508	06-22	FA1012	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
CARL11	0I	207	1/4,2/6	202	CCAR71	8H1
CAR1.B70	I	114	2/8		ADDPI10	7A0
DML1080	0	110	2/5,2/9 5/14	202	DML.GB00	3H8
DML1090	0	108	2/5,2/9 5/13	202	DML.GB10	3H7
DML1100	0	208	2/5,2/9 5/12	202	DML.GB20	3H7
DML1110	0	100	2/5,2/9 5/11	202	DML.GB30	3H6
DML1120	0	001	2/5,2/9 5/10	202	DML.GB40	3H5
DML1130	0	201	2/5,2/9 5/9	202	DML.GB50	3H4
DML1140	0	013	2/5,2/9 5/8	202	DML.GB60	3H4
DML1150	0	213	2/5,2/9 5/7	202	DML.GB70	3H3
EROT1AB1	I	216	2/5		ROTA.B1	2A7
EROT1BA1	I	309	2/5		ROTB.A1	2A2
FN1ADLG0	I	217	2/6		ADDLGI0	7A1
FN1ADSH0	I	117	2/6		ADDSHI0	7A2
FN1BDL10	I	314	2/6		BDLI100	7A3
FN1BDL20	I	015	2/6		BDLI200	7A4
FN1BDL40	I	215	2/6		BDLI400	7A5
FN1BDL80	I	115	2/6		BDLI800	7A6
F1D4R10	I	111	1/13		F1D4R10	3A1
F1D4R20	I	214	1/13		F1D4R20	3A1
F3D4L80B	I	112	1/13		F3D4L80B	3A2
F3D4LD0	I	312	1/13		F3D4LD0	3A2
F3D4LE0	I	014	1/13		F3D4LE0	3A1
F3D4L70	I	212	1/13		F3D4L70	3A2
GB080	I	006	2/3		GB0010	4A8
GB090	I	106	2/3		GB0110	4A7
GB100	I	307	2/3		GB0210	4A6
GB110	I	205	2/3		GB0310	4A5
GB120	I	002	2/3		GB0410	4A4
GB130	I	003	2/3		GB0510	4A3
GB140	I	103	2/3		GB0610	4A2
GB150	I	204	2/3		GB0710	4A1
MO.SBR10	I	317	2/5		BRSETI0	2A8
MO.2BR10	I	218	2/5		BRCLRI0	2A8
OPLUS31	0	300			OPLUS1	2H0
	I	010			T3D4LD0	2A4
ROT1080	I	206	2/5		A.BRT000	4A8
ROT1090	I	306	2/5		A.BRT010	4A7
ROT1100	I	008	2/5		A.BRT020	4A6
ROT1110	I	005	2/5		A.BRT030	4A5
ROT1120	I	301	2/5		A.BRT040	4A4
ROT1130	I	203	2/5		A.BRT050	4A3
ROT1140	I	303	2/5		A.BRT060	4A2
ROT1150	I	104	2/5		A.BRT070	4A1
T1D4R10	I	318	1/11		T1D4R10	2A1
T1D4R20	I	019	1/11		T1D4R20	2A1
T1D4R40	I	219	1/11		T1D4R40	2A1
T3D4L80A	I	109	1/11		T3D4L80	2A0
T3D4L70	I	118	1/11		T3D4L70	2A5
3T062B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0622B	I	102			OGRD0	2A3

SYMBOL NO. 7 (CONT)

DML1 15-08

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML11508	06-22	FA1012	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0622B	GRD	200			GRD	
3VG0622T	I	116			BLK840	2A5
	I	311			F3D4L80A	3A0
	GRD	319			GRD	
3V062A	PWR	000	14/8		+3	
	PWR	119	14/8		+3	
3V062B	PWR	000	(X)14/8	203	+3	
	PWR	119	(X)14/8	203	+3	

SYMBOL NO. 8

DML1 07-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML10700	06-24	FA1012	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		207			CCAR71	8H1
ARH4.GB1	I	012	2/6		F1D4R40	3A0
AR1001	0	105	2/5,2/6		ARB01	5H9
AR1011	0	011	2/5,2/6		ARB11	5H8
AR1021	0	305	2/5,2/6		ARB21	5H6
AR1031	0	211	2/5,2/6		ARB31	5H5
AR1041	0	202	2/5,2/6		ARB41	5H4
AR1051	0	210	2/5,2/6		ARB51	5H3
AR1061	0	302	2/5,2/6		ARB61	5H2
AR1071	0	308	2/5,2/6		ARB71	5H1
BR1000	0	113	1/4,2/5	202	BRB00	6H8
BR1010	0	107	2/5	202	BRB10	6H8
BR1020	0	313	2/5	202	BRB20	6H6
BR1030	0	304	2/5	202	BRB30	6H5
BR1040	0	009	2/5	202	BRB40	6H4
BR1050	0	101	2/5	202	BRB50	6H3
BR1060	0	209	2/5	202	BRB60	6H2
BR1070	0	004	2/5	202	BRB70	6H2
CAR1.B70	0	007	2/7		CCAR70	8H1
DML1GB0		310			DML.GB0	3H2
DML1000	0T I	110	2/6 2/1,2/9 5/14	202	DML.GB00	3H8
DML1010	0T I	108	2/6 2/1,2/9 5/13	202	DML.GB10	3H7
DML1020	0T I	208	2/6 2/1,2/9 5/12	202	DML.GB20	3H7
DML1030	0T I	100	2/6 2/1,2/9 5/11	202	DML.GB30	3H6
DML1040	0	001	2/1,2/9 5/10	202	DML.GB40	3H5
DML1050	0	201	2/1,2/9 5/9	202	DML.GB50	3H4
DML1060	0	013	2/1,2/9 5/8	202	DML.GB60	3H4

SYMBOL NO. 8 (CONT)

DML1 07-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML10700	06-24	FA1012	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
DML1070	0	213	2/1,2/9 5/7	202	DML.GB70	3H3
EROT1AB1	I	216	2/5		ROTA.B1	2A7
EROT1BA1	I	309	2/5		ROTB.A1	2A2
FL2T1B10	I	315	2/6		FL2B00	6A9
FL2T1B20	I	016	2/6		FL2B20	6A7
FL2T1B40	I	316	2/6		FL2B40	6A6
FL2T1B80	I	017	2/6		FL2B80	6A4
FN1ADLG0	I	217	2/6		ADDLGI0	7A1
FN1ADP10	I	114	2/6		ADDPI10	7A0
FN1ADSH0	I	117	2/6		ADDSHI0	7A2
FN1BDL10	I	314	2/6		BDLI100	7A3
FN1BDL20	I	015	2/6		BDLI200	7A4
FN1BDL40	I	215	2/6		BDLI400	7A5
FN1BDL80	I	115	2/6		BDLI800	7A6
F1D4R10	I	111	1/13		F1D4R10	3A1
F1D4R20	I	214	1/13		F1D4R20	3A1
F3D4L80B	I	112	1/13		F3D4L80B	3A2
F3D4LD0	I	312	1/13		F3D4LD0	3A2
F3D4LE0	I	014	1/13		F3D4LE0	3A1
F3D4L70	I	212	1/13		F3D4L70	3A2
GB000	I	006	2/4		GB0010	4A8
GB010	I	106	2/4		GB0110	4A7
GB020	I	307	2/4		GB0210	4A6
GB030	I	205	2/4		GB0310	4A5
GB040	I	002	2/4		GB0410	4A4
GB050	I	003	2/4		GB0510	4A3
GB060	I	103	2/4		GB0610	4A2
GB070	I	204	2/4		GB0710	4A1
MD.SBR10	I	317	2/5		BRSETI0	2A8
MD.2BR10	I	218	2/5		BRCLRI0	2A8
MDFL2T10	I	018	1/4		FL2BINI0	2A9
OPLUS21	0	300			OPLUS1	2H0
	I	116			BLK840	2A5
ROT1000	I	206	2/5		A.BRT000	4A8
ROT1010	I	306	2/5		A.BRT010	4A7
ROT1020	I	008	2/5		A.BRT020	4A6
ROT1030	I	005	2/5		A.BRT030	4A5
ROT1040	I	301	2/5		A.BRT040	4A4
ROT1050	I	203	2/5		A.BRT050	4A3
ROT1060	I	303	2/5		A.BRT060	4A2
ROT1070	I	104	2/5		A.BRT070	4A1
T1D4R10	I	318	1/11		T1D4R10	2A1
T1D4R20	I	019	1/11		T1D4R20	2A1
T1D4R40	I	219	1/11		T1D4R40	2A1
T3D4L80A	I	109	1/11		T3D4L80	2A0
T3D4LD0	I	010	1/11		T3D4LD0	2A4
T3D4L70	I	118	1/11		T3D4L70	2A5
3T062A	GRD	0GD		203	GRD	

PART OF FS 2

SYMBOL(S) 6 7 8

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

BELL LABORATORIES

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PART OF FS 2

DATA MANIPULATION LOGIC(DML)

SYMBOL NO. 8 (CONT)

DML1 07-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DML10700	06-24	FA1012	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
3T062A	GRD	2GD		203	GRD	
	GRD	200		203	GRD	2G1
	GRD	319		203	GRD	
3VG0624B	I	102			DGRD0	2A3
	GRD	200			GRD	
3VG0624T	I	311			F304LB0A	3A0
	GRD	319			GRD	
3V062A	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 9

DML MATCHER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DMLMATCH	06-20	FA1026	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
DMLMTEN0	I	311	2/3		DML.GB01	3A5
DML1000	I	100	2/8	202	DML.000	4A8
DML1010	I	001	2/8	202	DML.010	4A7
DML1020	I	101	2/8	202	DML.020	4A6
DML1030	I	002	2/8	202	DML.030	4A5
DML1040	I	302	2/8	202	DML.040	4A4
DML1050	I	203	2/8	202	DML.050	4A3
DML1060	I	303	2/8	202	DML.060	4A2
DML1070	I	204	2/8	202	DML.070	4A1
DML1080	I	012	2/7	202	DML.080	3A4
DML1090	I	112	2/7	202	DML.090	3A3
DML1100	I	013	2/7	202	DML.100	3A2
DML1110	I	113	2/7	202	DML.110	3A1
DML1120	I	215	2/7	202	DML.120	2A7
DML1130	I	315	2/7	202	DML.130	2A6
DML1140	I	216	2/7	202	DML.140	2A5
DML1150	I	316	2/7	202	DML.150	2A4
DML1160	I	117	2/6	202	DML.160	2A3
DML1170	I	018	2/6	202	DML.170	2A3
DML1180	I	118	2/6	202	DML.180	2A2
DML1190	I	019	2/6	202	DML.190	2A1
ER.DML0	D	015	5/2		DMLMAT1	3G5
ER.IOH0	DT	214	10/2,10/6		IOMAT1	3G6
			10/10			
	I		5/1			
			TD CONN CKT			
GB000	I	300	2/4		GB.0010	4A7
GB010	I	201	2/4		GB.0110	4A6
GB020	I	301	2/4		GB.0210	4A5
GB03D	I	202	2/4		GB.0310	4A4
GB040	I	003	2/4		GB.0410	4A3
GB050	I	103	2/4		GB.0510	4A2
GB060	I	004	2/4		GB.0610	4A1
GB070	I	104	2/4		GB.0710	4A0
GB080	I	212	2/3		GB.0810	3A3
GB090	I	312	2/3		GB.0910	3A2

SYMBOL NO. 9 (CONT)

DML MATCHER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DMLMATCH	06-20	FA1026	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
GB100	I	213	2/3		GB.1010	3A1
GB110	I	313	2/3		GB.1110	3A0
GB120	I	115	2/3		GB.1210	2A7
GB130	I	016	2/3		GB.1310	2A6
GB140	I	116	2/3		GB.1410	2A5
GB150	I	017	2/3		GB.1510	2A4
GB160	I	317	2/2		GB.1610	2A3
GB170	I	218	2/2		GB.1710	2A2
GB180	I	318	2/2		GB.1810	2A1
GB190	I	219	2/2		GB.1910	2A0
ICCP20	I	IC	6/3		P20	3A6
ICP30	I	IC	6/3		P30D1	3A5
IGB.001	O	IC	6/3		GB.001	4G7
IGB.011	O	IC	6/3		GB.011	4G6
IGB.021	D	IC	6/3		GB.021	4G5
IGB.031	O	IC	6/3		GB.031	4G4
IGB.041	D	IC	6/3		GB.041	4G3
IGB.051	O	IC	6/3		GB.051	4G2
IGB.061	O	IC	6/3		GB.061	4G1
IGB.071	O	IC	6/3		GB.071	4G0
IGB.081	O	IC	6/3		GB.081	3G3
IGB.091	O	IC	6/3		GB.091	3G2
IGB.101	O	IC	6/3		GB.101	3G1
IGB.111	O	IC	6/3		GB.111	3G0
IGB.121	O	IC	6/3		GB.121	2G7
IGB.131	O	IC	6/3		GB.131	2G5
IGB.141	O	IC	6/3		GB.141	2G4
IGB.151	O	IC	6/3		GB.151	2G3
IGB.161	O	IC	6/3		GB.161	2G3
IGB.171	O	IC	6/3		GB.171	2G2
IGB.181	O	IC	6/3		GB.181	2G1
IGB.191	O	IC	6/3		GB.191	2G0
INA2D431	O	IC	6/3		NA2D431	3G8
IN2D4210	O	IC	6/3		NA2D4210	3G7
NA2D420	I	D11	1/8		NA2D42D	3A7
NA2D430	I	211	1/8		NA2D43D	3A8
3T062B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0620B	GRD	005			GRD005	2G2
	GRD	006			GRD006	2G1
	GRD	102			GRD102	2G2
	GRD	105			GRD105	2G1
	GRD	200			GRD	
	GRD	205			GRD205	2G1
	GRD	206			GRD206	2G1
	GRD	304			GRD304	2G2
	GRD	305			GRD305	2G1
3VG0620T	GRD	114			GRD114	2G1
	GRD	217			GRD217	2G0
	GRD	319			GRD	
3V062A	PWR	000	14/8		+3	
	PWR	119	14/8		+3	
3V062B	PWR	00D	(X)14/8	203	+3	
	PWR	119	(X)14/8	203	+3	

PART OF FS 2
SYMBOL(S) 8 9

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

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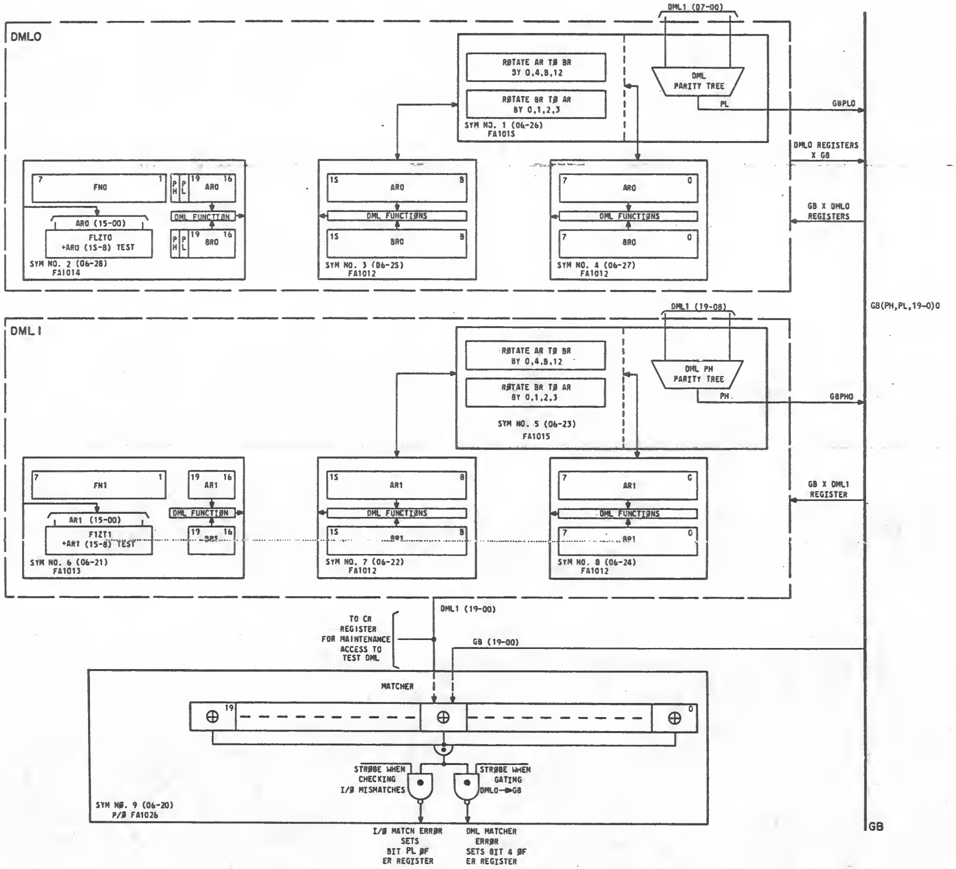
PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 1

FUNCTIONAL PARTITIONING OF DML LOGIC



CIRCUIT OPERATION

THE DATA MANIPULATION LOGIC (DML) PERFORMS THE ARITHMETIC AND LOGIC OPERATIONS IN THE 3A CC. IT CONSISTS OF A SERIES OF REGISTERS TO WHICH COMBINATIONAL LOGIC IS ATTACHED TO PERFORM ADDITION, SUBTRACTION, AND BOOLEAN OPERATIONS. IN ADDITION, THERE ARE A NUMBER OF OTHER FUNCTIONS THAT ARE PERFORMED WITHIN THE DML LOGIC. SOME ADDITIONAL FUNCTIONS ARE:

1. ROTATION.
2. A FIND LOW ZERO TEST.
3. SPECIAL GATING FUNCTIONS THAT ALLOW REGISTERS TO BE PACKED AND UNPACKED. THE PACKING RESULTS IN PUTTING BITS 0-15 OF A 20-BIT REGISTER INTO BITS 0-15 OF ONE OF THE TWO 16-BIT REGISTERS, AND PLACING BITS 16-19 OF THE SAME 20-BIT REGISTER INTO BITS 0-3 OF THE OTHER 16-BIT REGISTER. UNPACKING REFERS TO PUTTING THE SAME BIT PORTIONS OF TWO 16-BIT REGISTERS INTO A 20-BIT REGISTER, THAT IS, THE INVERSE OF THE PACK OPERATION.
4. PARITY GENERATION ON DML RESULTS. SINCE DML OPERATIONS TYPICALLY DESTROY PARITY, THIS ALLOWS DML RESULTS TO BE GATED BACK OUT ON THE GB WITHOUT GENERATING PARITY ERRORS.
5. A MATCH OF THE TWO DML'S. THIS INSURES THEIR CORRECT OPERATION.

COMPOSITE DIAGRAM NO. 1 SHOWS HOW ALL OF THIS LOGIC IS PARTITIONED WITHIN THE CIRCUIT PACKS THAT MAKE UP THE DML LOGIC. AS SHOWN, THE DML LOGIC IS DUPLICATED AND THE VERIFICATION OF THIS DUPLICATION IS PERFORMED BY A MATCHER ATTACHED TO DML 1 AND TO THE GATING BUS. EACH TIME A RESULT IS GATED OUT OF DML 0 ONTO THE GB, THE RESULT OF THAT GATING OPERATION IS CHECKED WITH THE CORRESPONDING RESULT COMING FROM DML 1. IF AN ERROR OCCURS, THE DML MATCH BIT ERROR WILL BE SET IN THE 3A CC ERROR REGISTER. NORMALLY THIS IS A "FATAL" ERROR AND WILL CAUSE THE 3A CC TO DO A "STOP AND A SWITCH".

AS SHOWN IN SYMBOL 9, AN ABILITY IS PROVIDED TO DIVERT THIS DML MATCHER TO AN "INTERRUPT" ERROR. THIS IS TYPICALLY USED WHEN CHECKING THE VALIDITY OF THE OPERATION OF THE I/O CHANNEL. IN THIS CASE, THE DML MATCH ERROR CAUSES AN INTERRUPT ERROR AND THEREFORE, THE HANDLING OF THE ERROR INDICATION IS MUCH LESS SEVERE.

ISSUE
5A

PART OF FS 2
COMPOSITE DIAGRAM 1

3A CENTRAL CONTROL

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PART OF FS 2

DATA MANIPULATIØN LØGIC (DML)

COMPOSITE DIAGRAM 2

DML GATING FUNCTIØNS(EXCEPT RØTATE)

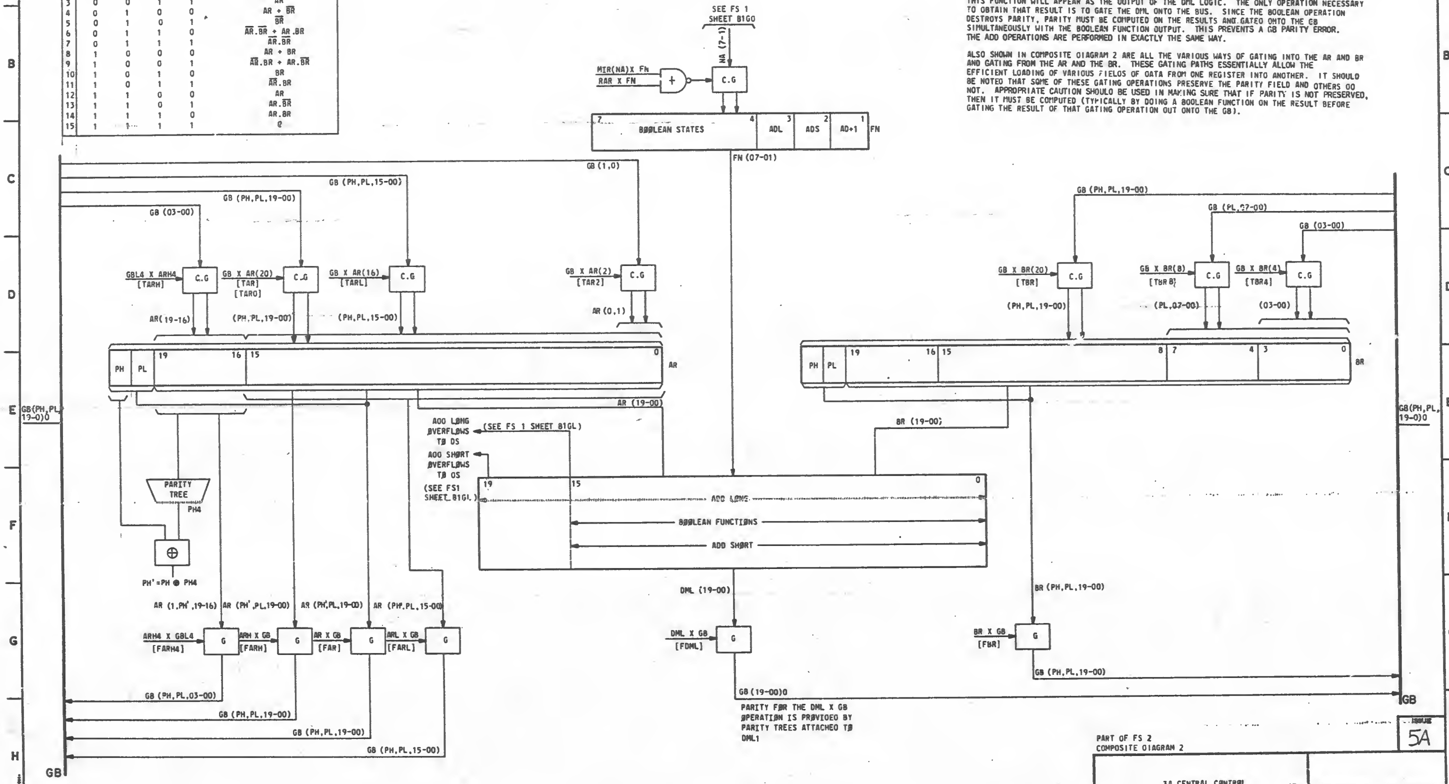
TABLE A
BØØLEAN STATES ØF THE FN REGISTERS

	FN REGISTER BIT				FUNCTIØN PERFØRMED
	7	6	5	4	[ie f(AR,BR)]
0	0	0	0	0	1
1	0	0	0	1	$\overline{AR} + \overline{BR}$
2	0	0	1	0	$\overline{AR} + BR$
3	0	0	1	1	$\overline{AR}$
4	0	1	0	0	$AR + \overline{BR}$
5	0	1	0	1	$\overline{BR}$
6	0	1	1	0	$\overline{AR}.\overline{BR} + AR.BR$
7	0	1	1	1	$\overline{AR.BR}$
8	1	0	0	0	$AR + BR$
9	1	0	0	1	$\overline{AR}.BR + AR.\overline{BR}$
10	1	0	1	0	BR
11	1	0	1	1	$\overline{AR}.BR$
12	1	1	0	0	AR
13	1	1	0	1	$AR.\overline{BR}$
14	1	1	1	0	$AR.BR$
15	1	1	1	1	0

CIRCUIT OPERATION

THERE ARE THREE MAIN REGISTERS WITHIN THE DML, THE FUNCTION REGISTER, THE AR REGISTER, AND THE BR REGISTER. A BOOLEAN OR ADD OPERATION IS PERFORMED BY LOADING THE FUNCTION REGISTER WITH THE DESIRED STATE AND, IN ADDITION, THE AR REGISTER AND THE BR REGISTER ARE LOADED WITH THE OPERANDS OF THE OPERATION TO BE PERFORMED. FOR EXAMPLE, IF A BOOLEAN OPERATION IS TO BE PERFORMED ON TWO REGISTERS, EACH REGISTER IS LOADED INTO THE AR AND BR RESPECTIVELY. THE BOOLEAN FUNCTION IS LOADED INTO THE FUNCTION REGISTER. ASSUME THE TWO REGISTERS ARE TO BE AND'ED TOGETHER AND THEREFORE, THE STATE 1110 WOULD BE LOADED INTO THE HIGH 4 BITS OF THE FUNCTION REGISTER (SEE ENTRY 14 IN TABLE A). IT SHOULD BE NOTED THAT FOR THE FOLLOWING BOOLEAN OPERATION, NONE OF THE ADD STATES CAN BE ACTIVE (BITS 1 THROUGH 3 OF THE FUNCTION REGISTER MUST EQUAL ZERO) FOR THIS OPERATION. THE BOOLEAN FUNCTION, WHEN LOADED IN THE FUNCTION REGISTER, ENABLES COMBINATIONAL LOGIC TO ATTACH THE OUTPUT OF THE AR AND THE BR TO PERFORM THE DESIGNATED BOOLEAN FUNCTION. THIS FUNCTION WILL APPEAR AS THE OUTPUT OF THE DML LOGIC. THE ONLY OPERATION NECESSARY TO OBTAIN THAT RESULT IS TO GATE THE DML ONTO THE BUS. SINCE THE BOOLEAN OPERATION DESTROYS PARITY, PARITY MUST BE COMPUTED ON THE RESULTS AND GATED ONTO THE GB SIMULTANEOUSLY WITH THE BOOLEAN FUNCTION OUTPUT. THIS PREVENTS A GB PARITY ERROR. THE ADD OPERATIONS ARE PERFORMED IN EXACTLY THE SAME WAY.

ALSO SHOWN IN COMPOSITE DIAGRAM 2 ARE ALL THE VARIOUS WAYS OF GATING INTO THE AR AND BR AND GATING FROM THE AR AND THE BR. THESE GATING PATHS ESSENTIALLY ALLOW THE EFFICIENT LOADING OF VARIOUS FIELDS OF DATA FROM ONE REGISTER INTO ANOTHER. IT SHOULD BE NOTED THAT SOME OF THESE GATING OPERATIONS PRESERVE THE PARITY FIELD AND OTHERS DO NOT. APPROPRIATE CAUTION SHOULD BE USED IN MAKING SURE THAT IF PARITY IS NOT PRESERVED, THEN IT MUST BE COMPUTED (TYPICALLY BY DOING A BOOLEAN FUNCTION ON THE RESULT BEFORE GATING THE RESULT OF THAT GATING OPERATION OUT ONTO THE GB).



PARITY FØR THE DML X GB ØPERATIØN IS PRØVIDED BY PARITY TREES ATTACHED TØ DML1

PART OF FS 2
COMPOSITE DIAGRAM 2

ISSUE 5A

3A CENTRAL CØNTRØL

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PART OF FS 2
DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 3
ROTATE LOGIC (DMLG)

TABLE B

MISCELLANEOUS DECODER ASSIGNMENTS		
FUNCTION	TO FIELD PAIR NETNAME (PIN NO.)	FROM FIELD PAIR NETNAME (PIN NO.)
ROTATE AR = > BR BY 12	T104L10 (116), T304RD0 (216)	F204L30 (313), F204RC0 (014)
8	T104L20 (301), T304RD0 (216)	F204L30 (313), F204RC0 (014)
4	T104L20 (301), T304RB0 (016)	F204L30 (313), F204RC0 (014)
0	T104L20 (301), T304R70 (015)	F204L30 (313), F204RC0 (014)
BR = > AR BY 3	T104L10 (116), T304RD0 (216)	F204LC0 (114), F204R90 (214)
2	T104L20 (301), T304RD0 (216)	F204LC0 (114), F204R90 (214)
1	T104L20 (301), T304RB0 (016)	F204LC0 (114), F204R90 (214)
0	T104L20 (301), T304R70 (015)	F204LC0 (114), F204R90 (214)
SET.BRO	T104L20 (301), T304R70 (015)	F204LC0 (114), F204RA0 (314)
CLR.BRO	T104L20 (301), T304RB0 (016)	F204LC0 (114), F204RA0 (314)

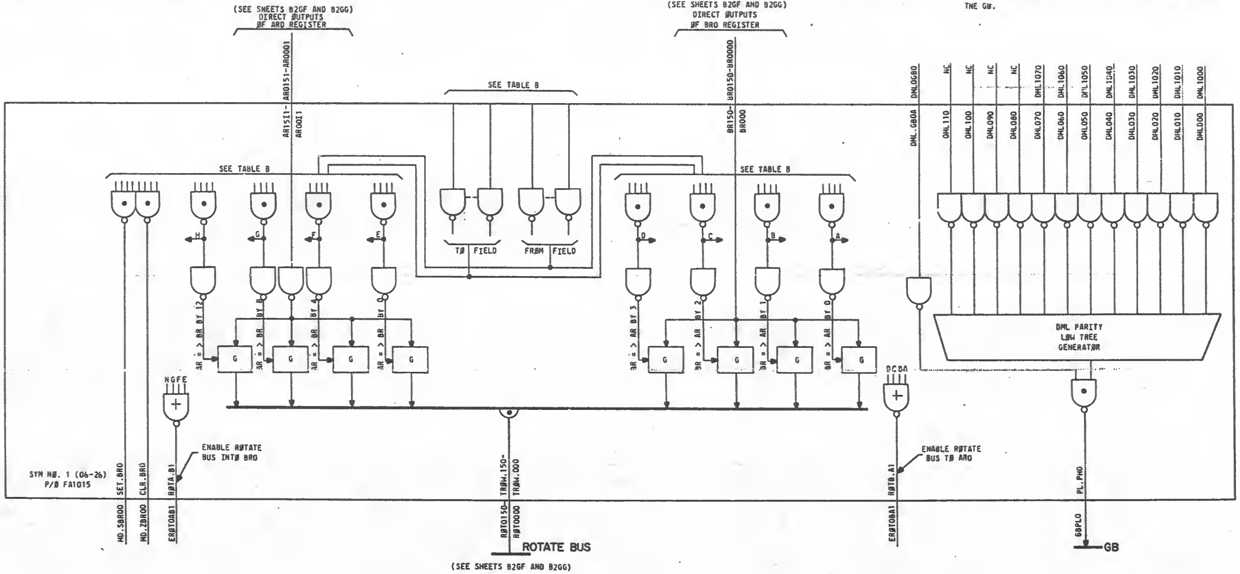
CIRCUIT OPERATION

ROTATE FUNCTIONS IN THE DML LOGIC ARE PERFORMED BY THE USE OF COMBINATIONAL LOGIC AND ARE TYPICALLY PERFORMED IN A 2-STEP SEQUENCE. THAT IS, THE ROTATION OF 0 TO 15 POSITIONS CAN BE PERFORMED BY GATING THE AR TO THE BR BY EITHER 0,4,8, OR 12 POSITIONS AND THEN GATING THE BR BACK TO THE AR BY EITHER 0,1,2, OR 3 POSITIONS. IN THIS MANNER, ANY ROTATE FUNCTION CAN BE PERFORMED IN TWO MICROCYCLES OR 300 NS.

AS SHOWN IN TABLE B, ONE OF FOUR MISCELLANEOUS DECODER CROSSPOINTS IS USED TO GATE THE AR TO THE BR BY THE APPROPRIATE NUMBER OF POSITIONS. THIS IS PERFORMED IN ONE MICROCYCLE. ON THE FOLLOWING MICROCYCLE, ONE OF FOUR MISCELLANEOUS DECODER CROSSPOINTS CAN BE USED TO GATE THE BR BACK TO THE AR. SINCE THIS OPERATION ALSO DESTROYS PARITY, IT IS NECESSARY TO RECOMPUTE PARITY ON THE RESULT OF THE ROTATE FUNCTION. ROTATE FUNCTIONS DESTROY PARITY BECAUSE PARITY IS TYPICALLY MAINTAINED OVER AN 8-BIT FIELD AND THE ROTATE IS PERFORMED OVER A 16-BIT FIELD. IN ADDITION TO THE ROTATE DATA ORIGINATING FROM THIS SYMBOL NO. 1, THE MISCELLANEOUS DECODER CROSSPOINTS THAT ENABLE THE ROTATE FUNCTIONS ARE "OR" ED TOGETHER AND SENT TO THE AR OR THE BR. THIS ALLOWS THE ROTATED DATA TO BE GATED INTO THE RESPECTIVE REGISTER.

CIRCUIT OPERATION (CONT)

THE DML PARITY TREE TO COMPUTE PARITY OVER THE LOW 8 BITS OF THE DML LOGIC IS LOCATED ON THE CIRCUIT PACK. NOTE THAT IT IS THE OUTPUT OF THE DML 1 THAT INPUTS INTO THIS PARITY TREE. NORMALLY, THE OUTPUT OF DML 1 FLOWS INTO THIS PARITY TREE ON A DC BASIS. THEREFORE, AS SOON AS A GATING SIGNAL IS RECEIVED TO GATE THE DML TO THE BUS, THE PARITY TREE IS STABLE TO ALLOW THE GATING OF THE COMPUTED PARITY BIT, IN THIS CASE PL. OUT ONTO THE GB.



PART OF FS 2
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL	SD-1C900-01-B2GC
BELL TELEPHONE LABORATORIES INCORPORATED	6S

ISSUE 5A

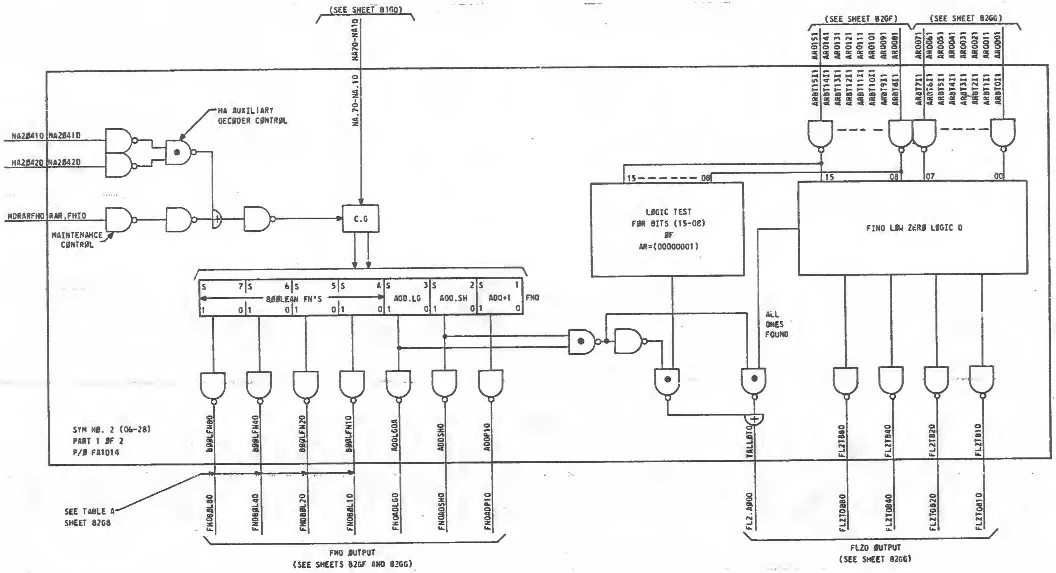
PART OF FS 2

DATA MANIPULATIØN LØGIC (DML)

COMPOSITE DIAGRAM 4

DMLO

FUNCTIØN REGISTER AND FLZT LØGIC


(SEE SHEET B1GO)
NA70-NA10
NA.70-NA.10
HA AUXILIARY DECØDER CØNTRØL
NA2Ø410 NA2Ø410
HA2Ø420 NA2Ø420
MDRARFHO RAR.FHIO
MAINTENANCE CØNTRØL
C.G
S 7 S 6 S 5 S A S 3 S 2 S 1
BØØLEAN FN'S
ADD.LG
ADD.SH
ADD+1
FNO
1 0 1 0 1 0 1 0 1 0 1 0 1 0
(SEE SHEET B2GF)
(SEE SHEET B2GG)
AR0151 AR0141 AR0131 AR0121 AR0111 AR0101 AR0091 AR0081
AR0071 AR0061 AR0051 AR0041 AR0031 AR0021 AR0011 AR0001
ARBT15I1 ARBT14I1 ARBT13I1 ARBT12I1 ARBT11I1 ARBT10I1 ARBT9I1 ARBT8I1
ARBT7I1 ARBT6I1 ARBT5I1 ARBT4I1 ARBT3I1 ARBT2I1 ARBT1I1 ARBT0I1
15 08
15 08 07 00
LØGIC TEST FØR BITS (15-08) ØF AR=(00000001)
FIND LØW ZERØ LØGIC 0
ALL ONES FOUND
SYM NØ. 2 (06-28)
PART 1 ØF 2
P/Ø FA1014
BØØLFN80 BØØLFN40 BØØLFN20 BØØLFN10 ADDLGOA ADDSHO ADDP10
TALLØTO
FLZTB80 FLZTB40 FLZTB20 FLZTB10
SEE TABLE A SHEET B2GB
FNOBØL80 FNDBØL40 FNDBØL20 FNOBØL10 FNOADLGO FNOAOSHO FNOADP10
FL2.AØ00
FLZTOB80 FLZTOB40 FLZTOB20 FLZTOB10
FNO ØUTPUT (SEE SHEETS B2GF AND B2GG)
FLZO ØUTPUT (SEE SHEET B2GG)

CIRCUIT OPERATION

WHEN THE FUNCTION REGISTER IS LOADED, ITS OUTPUT STATES DEFINE THE FUNCTIONAL OPERATION TO BE PERFORMED BY THE DML. THE DEFINITION OF THE BOOLEAN FUNCTION STATES ARE DEFINED ON SHEET B2GB. THE OPERATION OF THE THREE OTHER BITS OF THE FUNCTION REGISTER ARE AS FOLLOWS:

> ADD LONG ENABLES THE ADD LOGIC IN DML 0 TO PERFORM A 20-BIT ADD. THE OVERFLOW FROM BIT 19 OF THE ADD OPERATION IS GATED INTO THE MCS REGISTER WHEN THE RESULT OF THE ADD OPERATION IS GATED ONTO THE GB.
>
> ADD SHORT PERFORMS IN EXACTLY THE SAME WAY AS ADD LONG EXCEPT THAT IT PERFORMS A 16-BIT ADD AND THE ØVERFLOW BIT 15 IS GATED TO THE OS.
>
> ADD+1 IS USED IN CONJUNCTION WITH AN ADD LONG OR AN ADD SHORT AND SIMPLY ADD+1 TO THE RESULT OF THE SUM OF EITHER OF THESE TWO ADD OPERATIONS.

AN ADDITIONAL FUNCTIONAL STATE HAS BEEN GENERATED WITH THE USE OF THE ADD LONG AND THE ADD SHORT TOGETHER, AS SHOWN IN SYMBOL 2. THIS FUNCTIONAL STATE ENABLES A SPECIAL TEST OF THE HIGH 8 BITS OF THE AR REGISTER. THIS TEST WILL BE EXPLAINED IN A FOLLOWING PARAGRAPH.

THE FUNCTION REGISTER IS LOADED FROM THE NEXT ADDRESS FIELD OF THE NIR. THE CONTROL TO LOAD THE FUNCTION REGISTER IS ALSO DEFINED BY THE NEXT ADDRESS FIELD . THE UPPER 4 BITS OF THE NEXT ADDRESS FIELD DEFINE A 2-OUT-OF-A CODE. ONE OF THOSE CODES IS USED TO LOAD THE LOW 8 BITS OF THE OF THE NEXT ADDRESS FIELD INTO THE FUNCTION REGISTER. THIS DECODER IS CALLED THE NEXT ADDRESS AUXILIARY DECODER CONTROL. THE FINAL STAGE DECODING IS CONTAINED ON THIS SYMBOL NO. 2 AS SHOWN.

THERE IS ALSO A MAINTENANCE PATH TO LOAD THE FUNCTION REGISTER. THE SOURCE OF THE DATA FOR THE FUNCTION REGISTER COMES FROM THE RETURN ADDRESS REGISTER AND OR'S ONTO THE SAME INPUT PATH AS FROM THE NEXT ADDRESS FIELD. A SEPERATE CONTROL IS PROVIDED TO LOAD THIS PATH. IT IS A MISCELLANEOUS DECODER CONTROL, AS SHOWN.

ALSO CONTAINED ON SYMBOL NO. 2 IS THE FIND LOW ZERO LOGIC. THIS LOGIC CONVERTS THE POSITION OF THE LOW ORDER ZERO FOUND IN THE AR REGISTER (COPY 0) AND CONVERTS IT INTO A BINARY NUMBER REPRESENTING THE POSITION OF THIS LOW ORDER ZERO. IN ADDITION, IF THERE ARE NO ZEROS FOUND, A SIGNAL IS ACTIVATED THAT INDICATES THE AR IS ALL ONES. THE RESULT OF THIS SIGNAL IS GATED INTO THE OS BIT OF THE MSC REGISTER WHEN THE FIND LOW ZERO TEST IS ENABLED BY A MISCELLANEOUS DECODER CROSSPOINT. A MISCELLANEOUS DECODER CROSSPOINT IS USED TO ACTIVATE THE FIND LOW ZERO TEST AND AS SUCH, GATES THE BINARY OUTPUT TO THE LOW A BITS OF THE BRO REGISTER (SEE COMPOSITE DIAGRAM 7).

AN ADDITIONAL TEST PERFORMED ON THE AR IS USED TO DETECT THE CONSTANT "ONE" IN BITS 8 THROUGH 15 OF THE AR. IF THIS CONSTANT IS FOUND, A SIGNAL IS ACTIVATED. THIS SIGNAL IS GATED TO THE OS BIT IF A FIND LOW ZERO TEST IS PERFORMED AND THE ADD LONG AND ADD SHORT STATES ARE ACTIVATED IN THE FUNCTION REGISTER. THE PRECEEDING RESULTS IN CIRCUITRY BEING USED IS COMMON BETWEEN THE FIND LOW ZERO TEST, THE ADD LOGIC, AND THE SPECIAL TEST PERFORMED ON BITS 8 THROUGH 15 OF THE AR.

PART OF FS 2
COMPOSITE DIAGRAM A

ISSUE 5A

3A CENTRAL CØNTRØL

SD-1C900-01-B2GD

BELL TELEPHONE LABORATORIES
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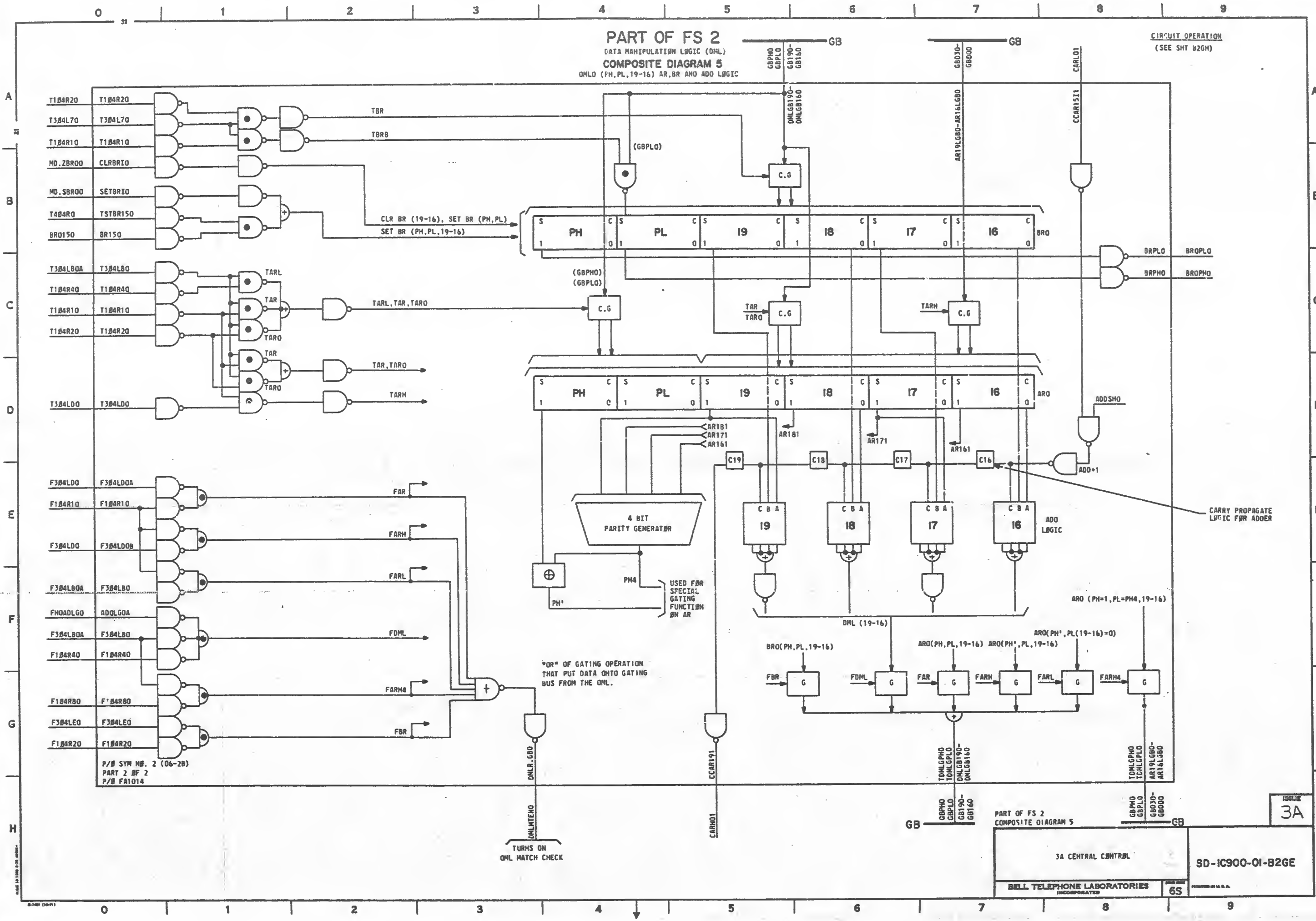
PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 5

DMLO (PH,PL,19-16) AR,BR AND ADD LOGIC

CIRCUIT OPERATION
(SEE SHT B2GH)



PART OF FS 2
COMPOSITE DIAGRAM 5

3A CENTRAL CONTROL

SD-1C900-01-B2GE

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

ISSUE
3A

PART OF FS 2

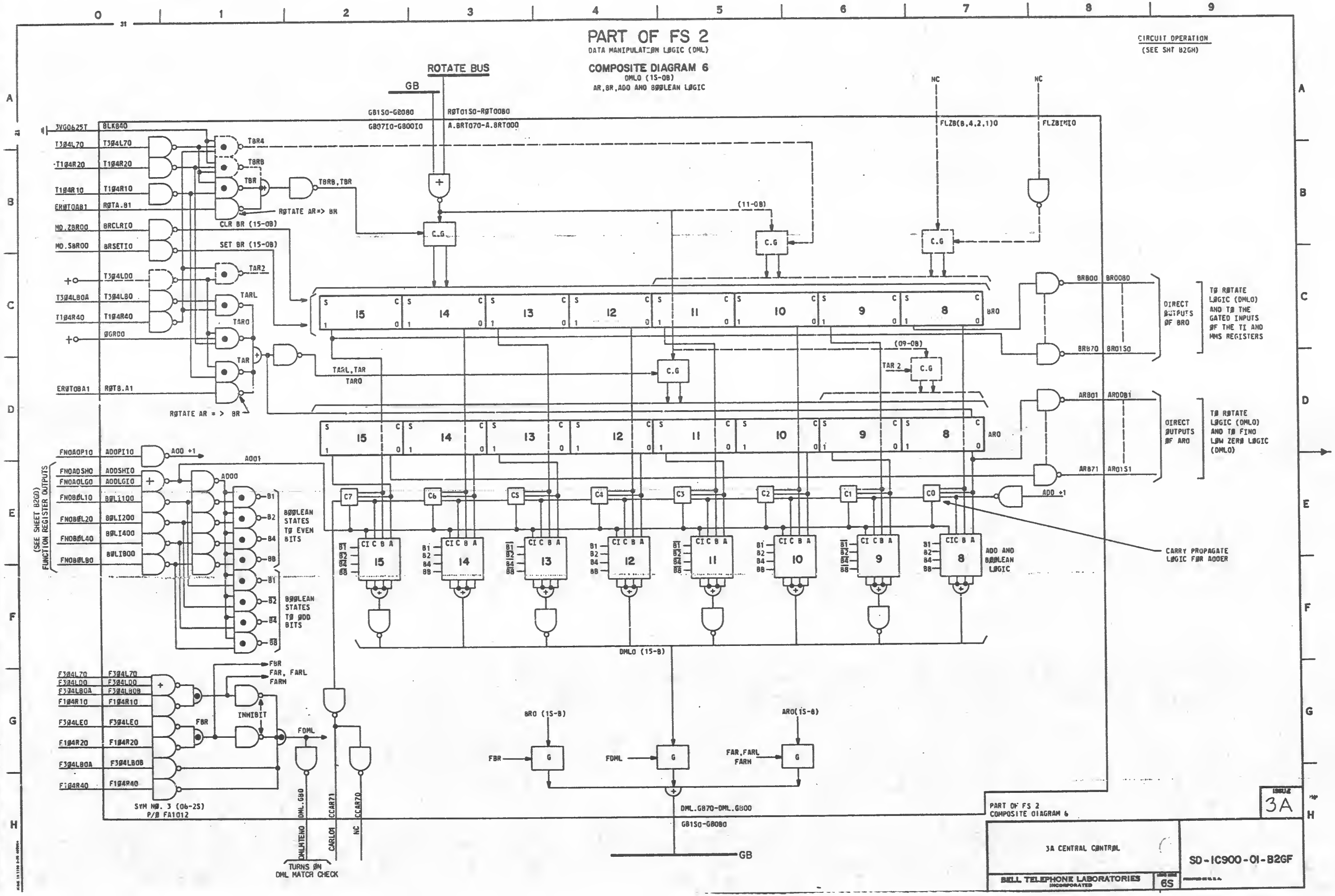
DATA MANIPULATIØN LØGIC (DML)

COMPOSITE DIAGRAM 6

DMLO (15-08)

AR,BR,ADD AND BØØLEAN LØGIC

CIRCUIT OPERATION
(SEE SHT B2GH)



PART OF FS 2
COMPOSITE DIAGRAM 6

ISSUE
3A

3A CENTRAL CONTRØL

SD-1C900-01-B2GF

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

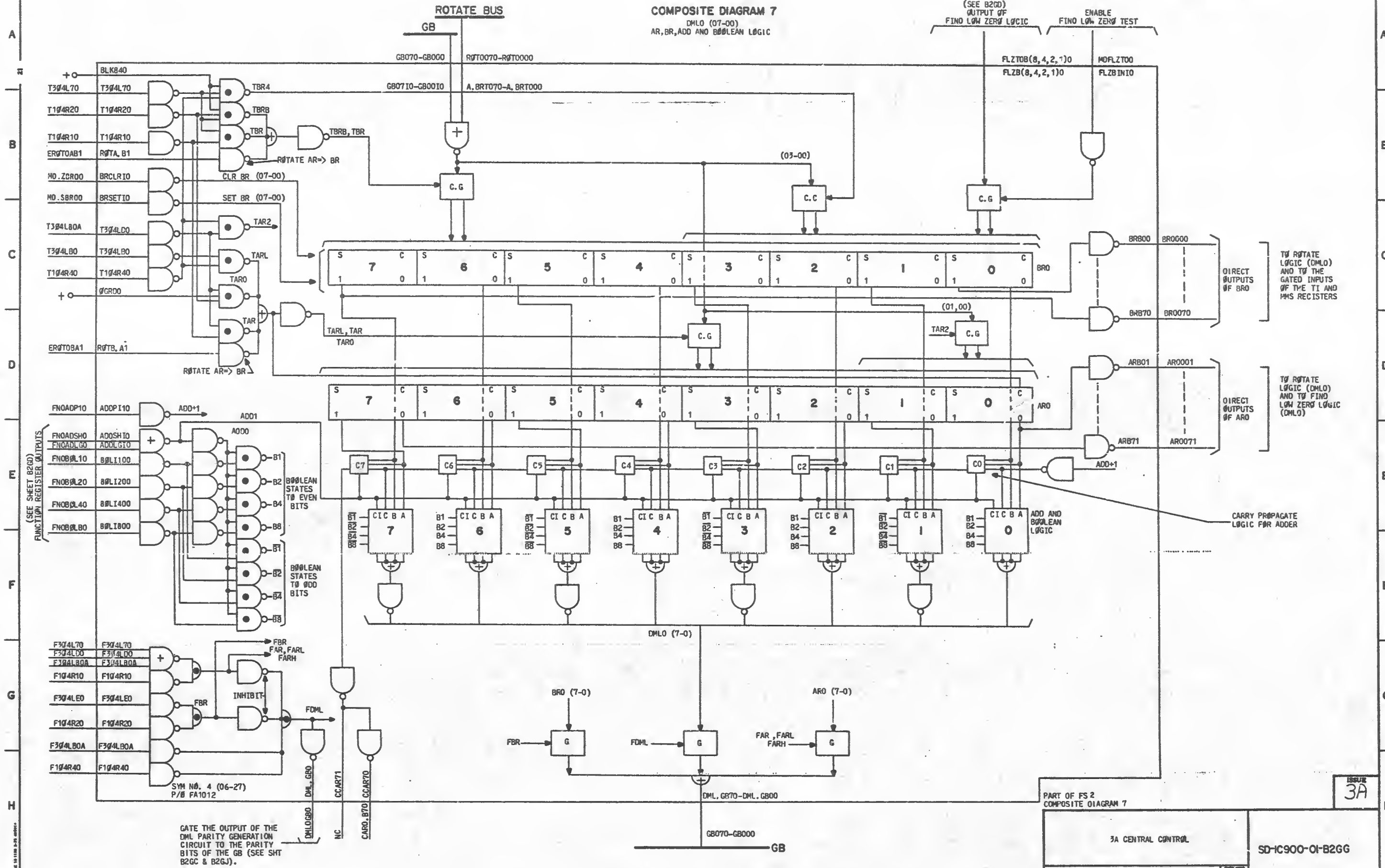
PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 7

DMLO (07-00)
AR,BR,ADD AND BOOLEAN LOGIC

CIRCUIT OPERATION
(SEE SHT B2GH)



GATE THE OUTPUT OF THE DML PARITY GENERATION CIRCUIT TO THE PARITY BITS OF THE GB (SEE SHT B2GC & B2GJ).

PART OF FS 2
COMPOSITE DIAGRAM 7

ISSUE
3A

3A CENTRAL CONTROL

SD-1C900-01-B2GG

BELL TELEPHONE LABORATORIES
INCORPORATED

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PART OF FS 2

DATA MANIPULATION LOGIC

COMPOSITE DIAGRAM 8

TABLE C (DLMO)

ABBREVIATION	FUNCTION	STM NO. 3 (06-25), FA1D12 SYM NO. 4 (06-27), FA1012 TO FIELD NETNAME (PIN NO.)	SYM NO. 2 (06-28), FA1014 TO FIELD NETNAME (PIN NO.)
TBR	GB=> BR (22)	T304L70 (118), T104R10 (318)	T304L70 (116), T104R10 (016)
TAR	GB=> AR (22)	T304LB0A (109), T104R10 (318)	T304B0A (313), T104R10 (016)
TARH	GB (0-3)=AR (16-19) NO PARITY BITS CHANGED IN AR		T304L00 (316), T104R10 (016)
TBR8	GB (0-7,PL)=> BR (D-7,PL) ALL OTHER BITS OF BR ARE UNCHANGED	T304L70 (118), T104R20 (019)	T304L70 (116), T104R20 (315)
TBR4	GB (0-3)=> BR (0-3) ALL OTHER BITS OF BR ARE UNCHANGED	T304L70 (118), T104R40 (219)	T304L70 (116), T104R40 (115)
TARO	GB=> ARD (22)	T304LB0A (109), T104R20 (019)	T304LB0A (313), T104R20 (315)
TARL	GB (0-15,PL,PH) AR (0-15,PL,PH) AR (16-19) ARE UNCHANGED	T304LB0A (109), T104R40 (219)	T304LBDA (313), T104R40 (115)
TAR2	GB (0-1)=> AR (0-1) ALL OTHER BITS OF AR ARE UNCHANGED	T304LD0 (010)*, T104R40 (219)	T304LD0 (316), T104R40 (115)

* SYM NO. 4 ONLT

TABLE D (DMLD)

ABBREVIATION	FUNCTION	SYM NO. 3 (06-25), FA1012 SYM NO. 4 (06-27), FA1012 FROM FIELD NETNAME (PIN NO.)	STM NO. 2 (06-28) FA1014 FROM FIELD NETNAME (PIN NO.)
FAR	AR=> GB (22)	F304L70 (212), F104R10 (111)	F304L70 (314), F104R10 (113)
FARL	AR (0-15,PL,PH') => GB (0-15,PL,PH)	F304LB0A (112), (311), F104R10 (111)	F304LB0A (311), F104R10 (113)
FARH	AR (0-19,PL,PH') => GB (0-19,PL,PH)	F304LD0 (312), F104R10 (111)	F304L00 (112) (114), F104R10 (113)
FBR	BR=> GB (22)	F304LE0 (014), F104R20 (214)	F304LE0 (213), F104R20 (014)
FDML	DML=> GB (22)	F304LB0A (112), (311), F104R40 (012)	F304LB0 (311), F104R40 (013)
FARH4	AR (16-19, PH4,1) => GB (0-3,PL,PH)		F304LB0 (311), F104R80 (312)

NOTE:

1. AR(PH') = AR(PH) + AR(PH4)

CIRCUIT OPERATION FOR COMPOSITE OIAGRAMS 5-8

THE FOLLOWING CIRCUIT OPERATION OESCRIPTION COVERS COMPOSITE OIAGRAMS 5,6, AND 7. SINCE EACH OF THESE COMPOSITE OIAGRAMS CONTAINS PORTIONS OF THE ARO, BRO REGISTER AND THEIR ASSOCIATED A00 ANO BOOLEAN LOGIC, ONLT COMPOSITE OIAGRAM 7 WILL BE OESCRIBEO IN DETAIL. THE OPERATION OF THE OTHER BITS OF THE AR ANO BR CAN BE ASSUMED TO BE IOENTICAL UNLESS DESCRIBEO OTHERWISE.

THE ARO AND BRO REGISTERS CAN BE LOADED OIRECTLT OFF OF THE GB IN ANALOGOUS MANNERS AS ALL OTHER REGISTERS IN THE 3A CC. IN ADOITION, THERE ARE A NUMBER OF SPECIAL GATING PATHS THAT ALLOW OPERATIONS TO BE EFFICIENTLY PERFORMED WHEN GATING IN OR OUT OF THESE REGISTERS. TABLE C INDICATES THE ABBREVIATION, THE FUNCTIONAL DESCRIPTION, AND THE BACKPLANE SIGNALS THAT ENABLE THAT FUNCTION TO BE PERFORMEO FOR EACH OF THE VARIDUS METHODS OF LOADING "TO" THE AR OR BR FROM THE GB. SIMILARLT, TABLE D, GIVES THE ABBREVIATION, FUNCTION OESCRIPTION, AND THE BACKPLANE SIGNALS THAT ENABLE THAT FUNCTION TO BE PERFORMED FOR EACH DF THE METHOOS OF LOADING "FROM" THE AR AND THE BR ONTO THE GATING BUS. THE GATING OPERATIONS IN GENERAL ARE FAIRLY STRAIGHTFORWARD ANO ARE EASILT UNDERSTOOD BY LOOKING AT THE GATING PATHS INVOLVED. THE MAJOR COMPLEXITY IN UNDERSTANDING THESE OPERATIONS IS IN DETERMINING WHEN THE PARITT IS PRESERVED OR WHEN THE PARITY IS DESTROYED. IF THE LATTER OCCURS, PARITY MUST BE RECREATED WHEN GATING OATA BACK OUT ONTO THE BUS FROM RESULTING DML OPERATIONS. NOTE THAT IT IS ASSUMEO THAT ALL DATA ARRIVES AT THE DML WITH GOOD PARITT. IF A DML OPERATION DESTROYS PARITT, IT IS NORMALLT ASSUMEO THAT BEFDRE THE DATA IS GATED BACK OUT ONTO THE GATING BUS PARITT MUST BE REGENERATEO WITHIN THE OML SO AS NOT TO CAUSE A PARITT ERRDR WITHIN THE 3A CC. IF PARITT GENERATION IS REQUIRED, A BOOLEAN LOGIC OPERATION IS USUALLY USED.

FOR EXAMPLE, IF THE ARO REGISTER CONTAINS BAD PARITY, THE BOOLEAN STATE THAT SELECTS THE AR FUNCTION OUTPUT (SEE ENTRY 12 IN TABLE A OF SHEET B2GB) IS LOADEO INTO THE FUNCTION REGISTER. THEN A DML GATING OPERATION PUTS THE ARO WITH GODD PARITT ONTO THE GB. NOTE THAT BOOLEAN FUNCTIONS ARE PERFORMEO DN 16 BITS OF DATA ONLY (0-15), IF PARITY GENERATION IS REQUIRED OVER A 20-BIT OATA FIELD, THE ADD LONG FUNCTION MUST BE USED WITH THE DATA FOR WHICH PARITY IS TO BE COMPUTED IN EITHER ARO OR BRD AND THE CONSTANT "ZERO" IN THE OTHER REGISTER, ARO OR BRO TTPICALLY.THE GATING OPERATIONS IN THE OML HAVE BEEN DESIGNEO SO THAT PARITT CAN BE PRESERVED. THEREFORE, TIME TO REGENERATE PARITY IS NOT REQUIRED. SINCE THESE ARE SOME GATING OPERATIONS THAT DO DESTRCY PARITY, APPROPRIATE CARE MUST BE TAKEN WHEN WHEN USING DML GATING FUNCTIONS.

FOR EXAMPLE, IF THE BRO REGISTER IS LOADEO WITH THE TBR FUNCTION, THEN ALL 22 BITS ARE LOADEO INTO THE BR REGISTER. THAT IS, BITS 0 THROUGH 19, THE DATA BITS, AND THE 2 PARITY BITS, PL AHO PH ARE LOADEO. THEREFORE, THE BR COULD BE GATED OIRECTLY BACK OUT ONTO THE GB WITH THE FBR FUNCTION WITHOUT CAUSING GB PARITY ERROR. ON THE OTHER HAND, IF THE T3R8 GATING FUNCTION IS USED TO LOAD THE LOW 8 BITS OF THE GB TOGETHER WITH PL BIT INTO THE RESPECTIVE BITS OF THE BR, CAUTION WOULD HAVE TO BE USED BEFORE GATING THE BR BACK OUT ONTO THE GB. THAT IS, SINCE ALL OTHER BITS OF THE BR ARE UNCHANGED, IT IS NECESSARY TO INSURE THAT THE UPPER BITS OF THE BRO CONTAINEO GOOD PARITY, BITS 8 TROUGH 19, AND ITS RESPECTIVE PARITY BIT PH.

AN EXAMPLE OF HOW THESE DML GATING OPERATIONS ARE USEO TO EFFICIENTLT PERFORM CERTAIN OPERATIONS IS SHOWN WITH THE USE OF TWO OF THE GATING COMMANOS THAT GATE FROM THE ARO REGISTER. LET US FIRST ASSUME THE ARO HAS BEEN LOAOEO WITH A 20-BIT CONSTANT. TYPICALLY, A 20-BIT CONSTANT

CIRCUIT OPERATION (CONT)

REPRESENTS THE AODRESS OF A MAINSTORE LOCATION ANO THEREFORE IT IS OFTEN REQUIREO THAT THIS 20-BIT CONSTANT BE PUT INTO TWO 16-BIT REGISTERS SO THAT IT CAN BE SAVEO AWAY IN MEMORY. THE FARL FUNCTION GATES FROM THE AR REGISTER, BITS 0 THROUGH 15 ANO THE PL BIT ANO THE PH ONTO THE GB INTO BITS 0 THROUGH 15, AND PL ANO PH BITS, RESPECTIVELT. AS SHOWN IN COMPOSITE DIAGRAM 5, THE PH PRIME BIT REPRESENTS THE EXCLUSIVE OR OF THE ARO PH BITS AND THE OUTPUT DF THE PARITY TREE (PH 4) ATTACHEO TO THE HIGH 4 BITS OF THE ARO. THEREFORE, THE PARITY THAT IS GATED ONTO THE PH BIT OF THE GB REPRESENTS THE PARITY THAT WAS CONTAINED IN THE AR REGISTER. IT IS MODIFIED BY WHETHER THE HIGH 4 BITS OF THE AR, BITS 16 THROUGH 19, HAD EVEN OR ODD PARITY. THUS, FARL COMMAND CAN BE USED TO GATE THE LOW 16 BITS OF THE AR INTO A 16-BIT REGISTER WITH GOOD PARITY IN A SINGLE MICROCYCLE. THEN ON A SUBSEQUENT MICROCYCLE, THE FARH4 COMMAND CAN BE USEO TO GATE THE HIGH 4 BITS OF THE ARO REGISTER ONTO THE LOW 4 BITS OF THE GB WITH THE PARITY BEING OBTAINEO AS FOLLOWS. SINCE ZERDS ARE GATED INTO ALL BUT THE LOW 4 BITS OF THE GB, A DNE IS JAMMED INTO THE PH BIT OF THE GB. THE PL BIT OF THE GB IS OETERMINED BY USING THE OIRECT OUTPUT OF THE PARITY TREE (PH 4) ATTACHED TO THE HIGH 4 BITS OF ARD. THIS TWO STEP GATING OPERATION IS REFERED TO AS PACKING A REGISTER. THE REVERSE OPERATION IS ALSO PERFORMED IN A VERY SIMILAR WAY ANO IS REFERREO TO AS UNPACKING.

TO PERFORM ADO OPERATIONS, THE AR ANO THE BR ARE LOADED BY ANT OF THE GATING COMMANDS THAT LOAD THE AR AND BR. IT SHOULD BE NOTED THAT TO PERFORM AN ADO, IT IS NOT NECESSARY TO LOAD THE ARO AND THE BRO WITH GODD PARITT. THE FUNCTION REGISTER IS LDAOEO WITH THE APPROPRIATE ADO STATE. ASSUME IT IS AN ADO LONG. THE OUTPUT OF THE FUNCTION REGISTER COMES INTO SYMBOLS NO. 3 AND 4 AND ALLOWS THE BOOLEAN AND ADD LOGIC TO BE CONFIGURED FOR THE ADD STATE AS SHOWN ON THESE SYMBOLS. AS SOON AS THE ARO, BRO, AND FUNCTION REGISTER ARE LOADEO, THE ADO OPERATIONS BEGINS. THE ADDER USED RIPPLE CARRY LOGIC THAT PROPAGATES FROM DNE BIT POSITION TO ANOTHER. BECAUSE THE ADDER LOGIC USES THIS SIMPLE CARRT PROPAGATION LOGIC, IT IS RELATEVELT SLOW. TO OECREASE ITS CARRY PRDPAGATION OELAY, EVERT OTHER ADOER CELL HAS THE COMPLEMENT INPUTS FROM THE RESPECTIVE BIT OF THE ARO OR BRO. IT IS NOT NECESSARY TO GO INTO THE OETAILS OF THIS OPERATION SINCE THIS ASPECT OF THE ADDER LOGIC IS TRANSPARENT AT THE TERMINALS OF THE CIRCUIT PACKS. HOWEVER, IT DOES MAKE THE CARRY PROPAGATE LOGIC SOMEWHAT FASTER. ONE MICROCYCLE OF DELAY IS REQUIRED BETWEEN THE MICROCYCLE IN WHICH A DML REGISTER IS LOADEO, THE ARO,BRO OR THE FUNCTION REGISTER, ANO THE MICROCYCLE ON WHICH THE RESULTS OF THE ADD OPERATION CAN BE GATED ONTO THE GB. THIS TIME IS REQUIRED TO ALLOW THE ADDER LOGIC TO PERFORM ITS FUNCTION AND FOR THE PARITY GENERATOR TO COMPUTE PARITY ON THE OUTPUT OF THE ADDER. THE RESULT OF THE ADD OPERATION TOGETHER WITH THE COMPUTED PARITY BITS IS OBTAINED BY GATING THE DML TO THE GB WITH THE FDML FUNCTION SHOWN IN TABLE B.

THE BOOLEAN OPERATION ON THE ARO ANO BRO REGISTERS OPERATES IN A SIMILAR MANNER TO THE ADO LOGIC IN THAT IT REQUIRES THE FUNCTION REGISTER TO BE LOADEO APPROPRIATELY. IT ALSO USES THE GENERAL PURPOSE TRANSLATOR LOGIC ATTACHED TO THE RESPECTIVE BITS OF THE ARO AND THE BRO. SINCE THE BOOLEAN COMBINATIONAL LOGIC OOES NOT HAVE TO PROPAGATE A SIGNAL BETWEEN THE VARIOUS BITS, IT IS SOMEWHAT FASTER IN ITS OPERATION THAN THE ADO LOGIC. THEREFORE, IT IS NOT NECESSARY TO WAIT ONE MICROCYCLE BETWEEN LOADING EITHER THE ARO OR BRO AND THE FUNCTION REGISTER AND THEN LOADING THE RESULT OF THE OML TO THE BUS. NOTE ALSO THAT THE BOOLEAN OPERATION COMPUTES THE PARITY ON THE RESULT OF ITS OPERATION. THE BOOLEAN

CIRCUIT OPERATION (CONT)

OPERATION, UNLIKE THE ADD, CAN ONLY PERFORM ON 16 BITS OF OATA.

THE ADO SHORT FUNCTION PERFORMS IN THE SAME MANNER AS THE ADO LONG OPERATION WITH THE ONLY OIFFERENCE BEING THAT THE ADO TAKES PLACE OVER 16 BITS DF OATA DNLY. AS SEEN IN COMPOSITE DIAGRAM 5, THE AOD SHORT BLOCKS THE CARRY PROPAGATION LOGIC FROM CARRYING INTO THE 16TH BIT OF THE ADO LOGIC. IN ADOITION, WHEN THE RESULTS OF THE ADO OPERATION ARE GATED ONTO THE BUS WITH THE FDML FUNCTION, THE ADO SHORT INHIBITS THE HIGH 4 BITS OF THE OML OUTPUT FROM BEING GATEO OUT ONTO THE BUS. THE ADO SHORT ALLOWS THE CARRY OUTPUT OF BIT 15 TO BE GATED INTO THE DS WHEN THE FDML FUNCTION IS ACTIVATEO. THUS, THE OS BIT IS SET WHEN A CARRY OCCURS OUT OF BIT 15 OF THE ADO SHORT OPERATION, DR IN DTHER WORDS, IF AN OVERFLOW OCCURS ON THE ADD.

THE ADD LONG FUNCTION ENABLES THE CARRY OUTPUT OF BIT 19 OF THE ADD LOGIC TO BE GATED INTO THE DS BIT OF THE MCS REGISTER. THUS, WHEN THE FDML FUNCTION IS ENABLEO ANO THE RESULT OF THE ADD OPERATIDN IS GATED ON THE BUS, THE OS BIT IS SET IF AN OVERFLOW CONDITION OCCURS OUT OF BIT 19 OF ADD LOGIC.

AS SHOWN IN COMPOSITE DIAGRAM 3, THE ROTATE LDGIC IS LDCATED DH A CIRCUIT PACK SEPARATELY FROM THE ONE THAT CONTAINS THE ARO AND THE BRO ITSELF. THEREFORE, THE OUTPUT OF THE ARO AND BRO HEEO TO BE BRDUGHT TO THE BACKPLAHE TO INPUT TO THE ROTATE LOGIC, AS SHOWN IN COMPOSITE DIAGRAMS 6 ANO 7. WHEN THE GATING SIGNAL THAT ENABLES THE ROTATE FUNCTION TO BE PERFORMEO, OCCURS, IT PUTS THE RESULT OF THE ROTATEO REGISTER, EITHER THE ARO OR THE BRO, ONTO A ROTATE BUS, WHICH IS THEN ENABLEO INTO THE ARO OR THE BRO, RESPECTIVELY. NOTE THAT THE ROTATE BUS, INPUTS INTO THE SAME LOGICAL GATE AS THE GB ITSELF. THEREFORE, IT IS NECESSART ONLY TO ENABLE THE COMMON NODE THAT GATES INTO EITHER THE AR OR BR TO ALLOW THE RESULT OF THE ROTATE OPERATION INTO THE RESPECTIVE REGISTER. NOTE ALSO THAT THE ROTATE BUS DOES NOT MAINTAIN GOOD PARITY, BUT SINCE IT IS ONLT THE GB BUS THAT IS REQUIRED TO HAVE GOOD PARITY, THIS CAUSES NO PROBLEM.

THE FINO LOW ZERO LOGIC THAT IS PERFORMED DH COMPOSITE DIAGRAN 4 IS EHABLED INTD THE BR REGISTER WITH THE CONTROL SHOWN IN COMPDSITE DIAGRAM 7. THIS RESULTS IN GATING A 4-BIT BINARY NUMBER INTO THE LOW 4 BITS OF THE BR CORRESPONDING TO THE POSITION OF THE LOW ORDER ZERO IN THE AR REGISTER.

THE CORRECT OPERATION OF THE DML LOGIC IS VERIFIED BY GATING THE SAME INFORMATION INTO BOTH OML 0 AND DML 1. WHILE DATA IS WITHIN THE DML, PARITY IS NOT NECESSARILY PRESERVED, BUT SINCE OUPLICATION IS PROVIDEO, THE PARITY CHECK IS NOT NECESSARY. WHEN THE RESULT OF A DML FUNCTION IS TO BE GATEO OUT BACK ONTO A GATING BUS, THE TWO DMLS MUST BE MATCHEO WITH EACH OTHER TO CHECK THE CORRECT OPERATION. THE MATCHER BETWEEN THE OMLS IS ENABLEO BY THE LOGIC SHOWN IN COMPOSITE DIAGRAMS 5 (G3) AND 6 (H1). IN ADOITION, THE PARITY THAT IS RECOMPUTED ON THE OUTPUT OF THE DML FUNCTIONS IS ENABLED ONTO THE GATING BUS WITH THE LOGIC SHOWN IN COMPOSITE OIAGRAM 7 (H2). NOTE THAT WHEN THE OUTPUT OF FUNCTIONS (ADO OR BOOLEAN) SET UP BY THE CONTROL FRON THE FUNCTION REGISTER ARE GATEO TO THE GB, THE FDML CONTROL IS USED. ALL OTHER OPERATIONS THAT GATE TO THE GB FROM THE OML USE REGISTER GATING OPERATIONS SUCH AS FARL, FARH, ETC. THESE GATING SIGNALS ALSO ACTIVATE THE DML MATCHER BUT THEY DO NOT GATE THE PARITY FORM THE DML PARITT GENERATOR. INSTEAD, PARITT IS ASSUMED TO COME FROM THE SOURCE REGISTER SELECTED FOR THAT GATING FUNCTION.

ISSUE 5A

PART OF FS 2
COMPOSITE OIAGRAN 8

3A CENTRAL CONTROL

SD-1C900-01-B2GH

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PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 9

ROTATE LOGIC (DML1)

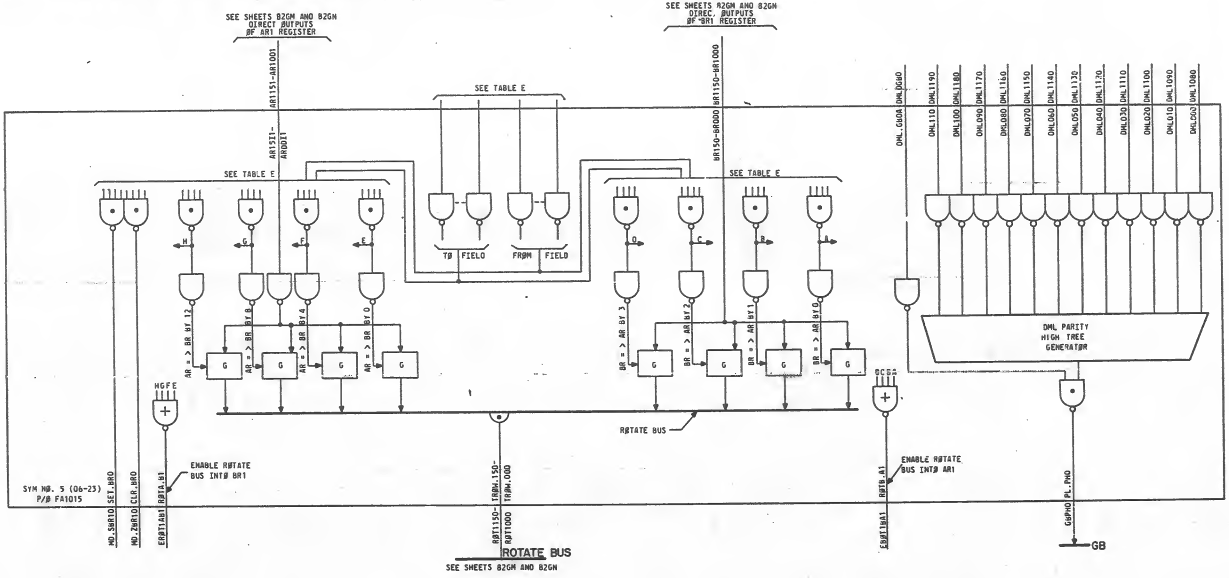
CIRCUIT OPERATION

THE ROTATE LOGIC FOR DML 1 WORKS EXACTLY THE SAME AS THE ROTATE LOGIC FOR DML 0. (SEE SHEET B2GC). COMPOSITE DIAGRAM 9 ALSO HAS THE DML PARITY TREE. IN THIS CASE, IT IS THE PARITY TREE THAT GENERATES PARITY HIGH (PH) FOR THE SW. IT ALSO OPERATES IN THE SAME MANNER AS THE PARITY LOW PARITY TREE DESCRIBED ON SHEET B2GC.

TABLE E

MISCELLANEOUS DECODER ASSIGNMENTS

FUNCTION		TO FIELD PAIR NETNAME (PIN NO.)	FROM FIELD PAIR NETNAME (PIN NO.)
ROTATE	AR = > BR BY 17	T104L10 (116), T304R00 (216)	F204L30 (313), F204RC0 (014)
	8	T104L20 (301), T304R00 (216)	F204L30 (313), F204RC0 (014)
	4	T104L20 (301), T304RB0 (016)	F204L30 (313), F204RC0 (014)
	0	T104L20 (301), T304R70 (015)	F204L30 (313), F204RC0 (014)
	BR = > AR BY 3	T104L10 (116), T304R00 (216)	F204LC0 (114), F204R90 (214)
	2	T104L20 (301), T304R00 (216)	F204LC0 (114), F204R90 (214)
	1	T104L20 (301), T304RB0 (016)	F204LC0 (114), F204R90 (214)
	0	T104L20 (301), T304R70 (015)	F204LC0 (114), F204R90 (214)
SET.BRO		T104L20 (301), T304R70 (015)	F204LC0 (114), F204RA0 (314)
CLR.BRO		T104L20 (301), T304RB0 (016)	F204LC0 (114), F204RA0 (314)



PART OF FS 2
COMPOSITE DIAGRAM 9

ISSUE 5A

3A CENTRAL CONTROL

SD-1C900-01-B2GJ

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PART OF FS 2

DATA MANIPULATIØN LØGIC (DML)

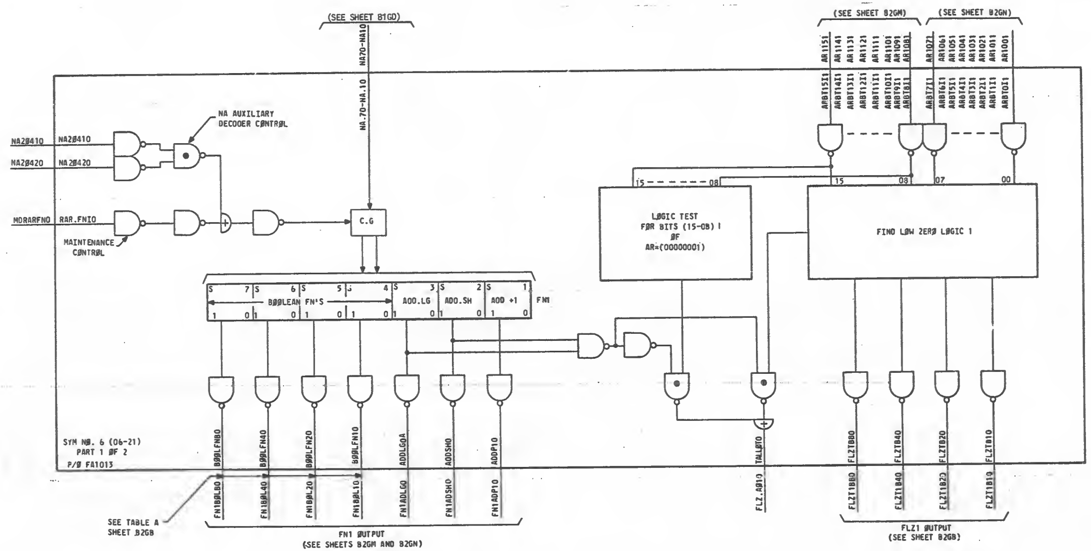
COMPOSITE DIAGRAM 10

DML1

FUNCTIØN REGISTER AND FLZT LØGIC

CIRCUIT OPERATION

THE FUNCTION REGISTER AND THE FIND LOW ZERO LOGIC FOR DML 1 WORKS THE SAME AS THE LOGIC AT THE FUNCTION REGISTER AND FIND LOW ZERO LOGIC FOR DML 0. SEE SHEET B2GO FOR CIRCUIT OPERATION.



PART OF FS 2
COMPOSITE DIAGRAM 10

ISSUE	5A
3A CENTRAL CØNTRØL	SD-1C900-01-B2GK
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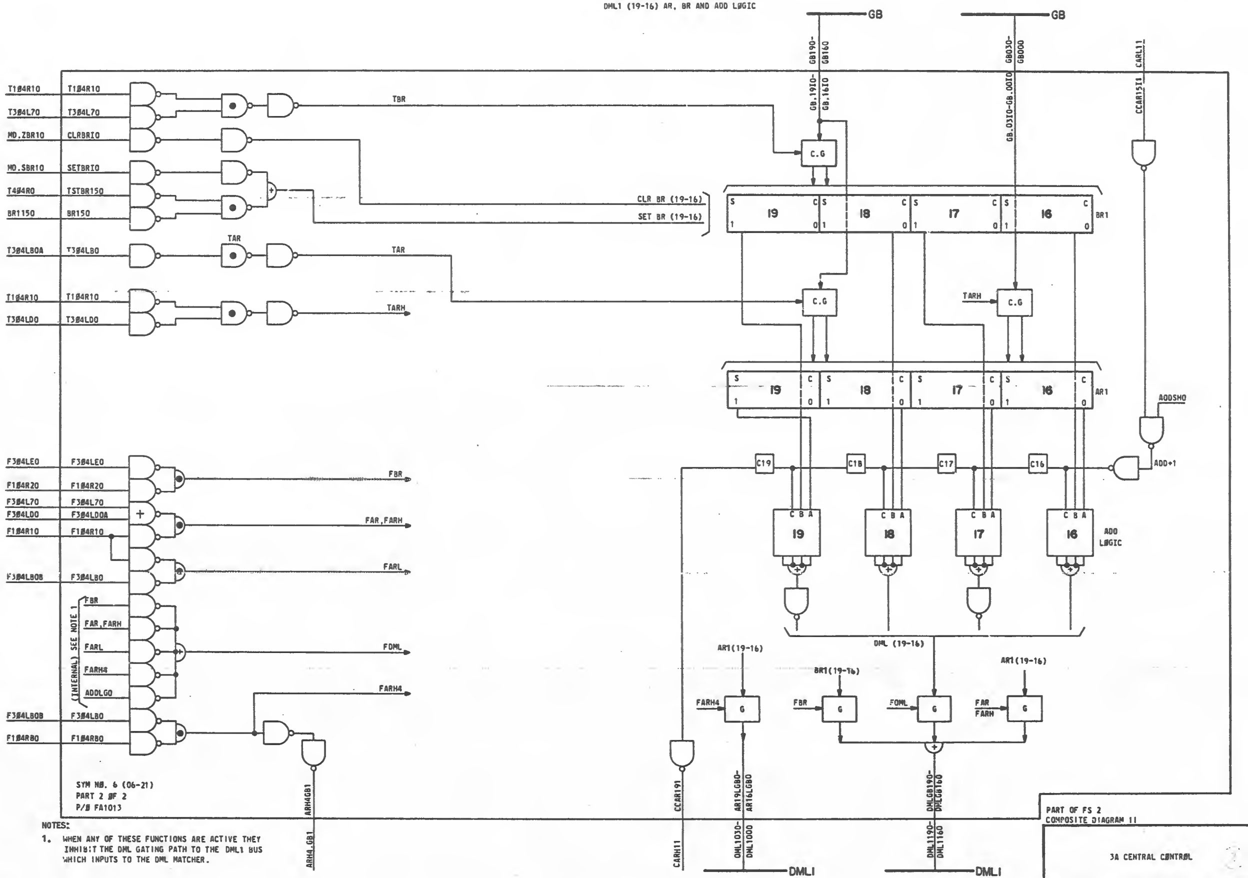
PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 11

DML1 (19-16) AR, BR AND ADD LOGIC

CIRCUIT OPERATION
(SEE SHT B2GP)



SYM NO. 6 (06-21)
PART 2 OF 2
P/O FA1013

NOTES:

1. WHEN ANY OF THESE FUNCTIONS ARE ACTIVE THEY INHIBIT THE DML GATING PATH TO THE DML1 BUS WHICH INPUTS TO THE DML MATCHER.

PART OF FS 2
COMPOSITE DIAGRAM 11

ISSUE
3A

3A CENTRAL CONTROL

SD-1C900-01-B2GL

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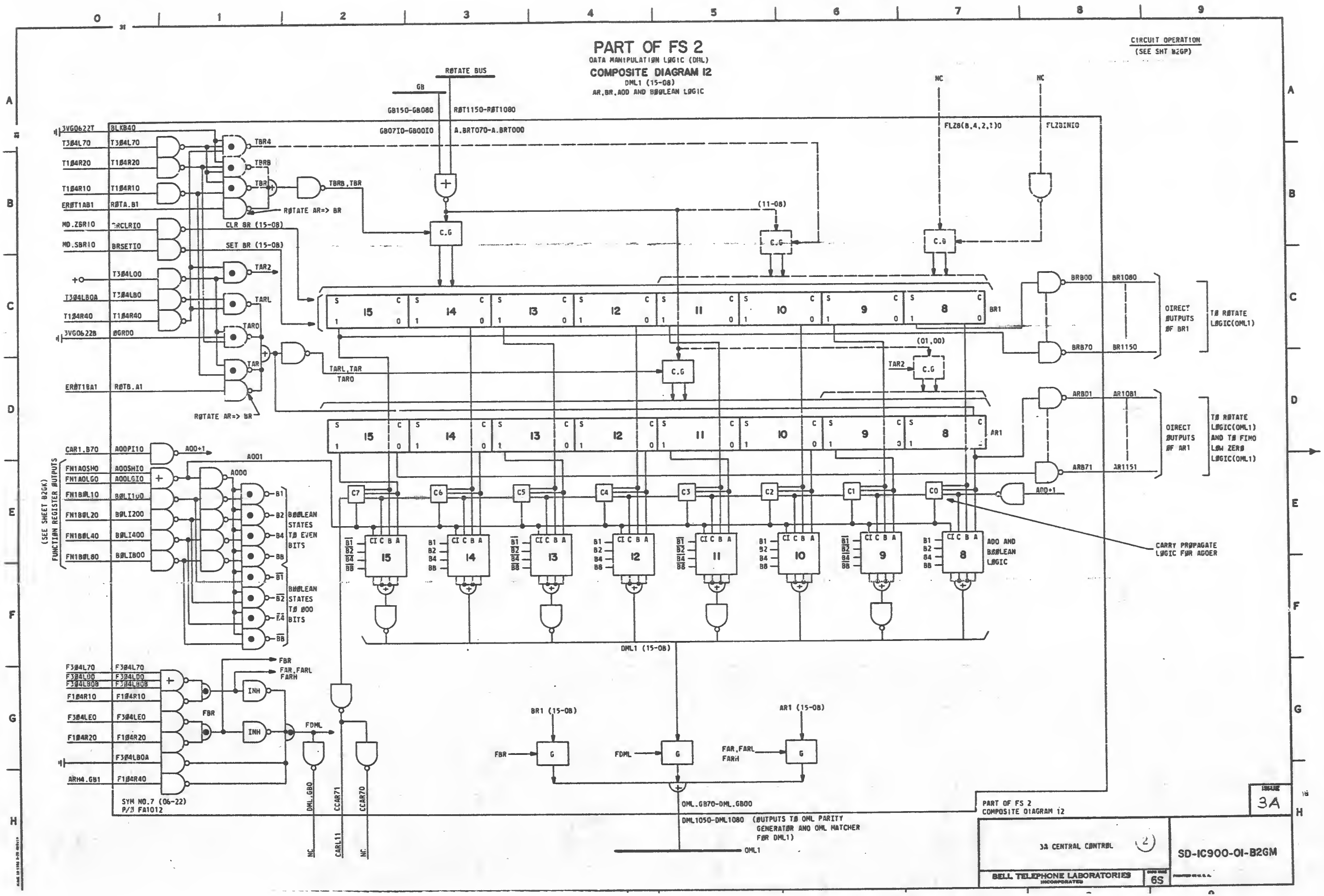
6S

PART OF FS 2
DATA MANIPULATIØN LØGIC (DML)
COMPOSITE DIAGRAM 12
DML1 (15-08)
AR,BR,ADD AND BØØLEAN LØGIC

CIRCUIT OPERATION
(SEE SHT B2GP)



PART OF FS 2
COMPOSITE DIAGRAM 12

ISSUE
3A

3A CENTRAL CØNTRØL
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PART OF FS 2

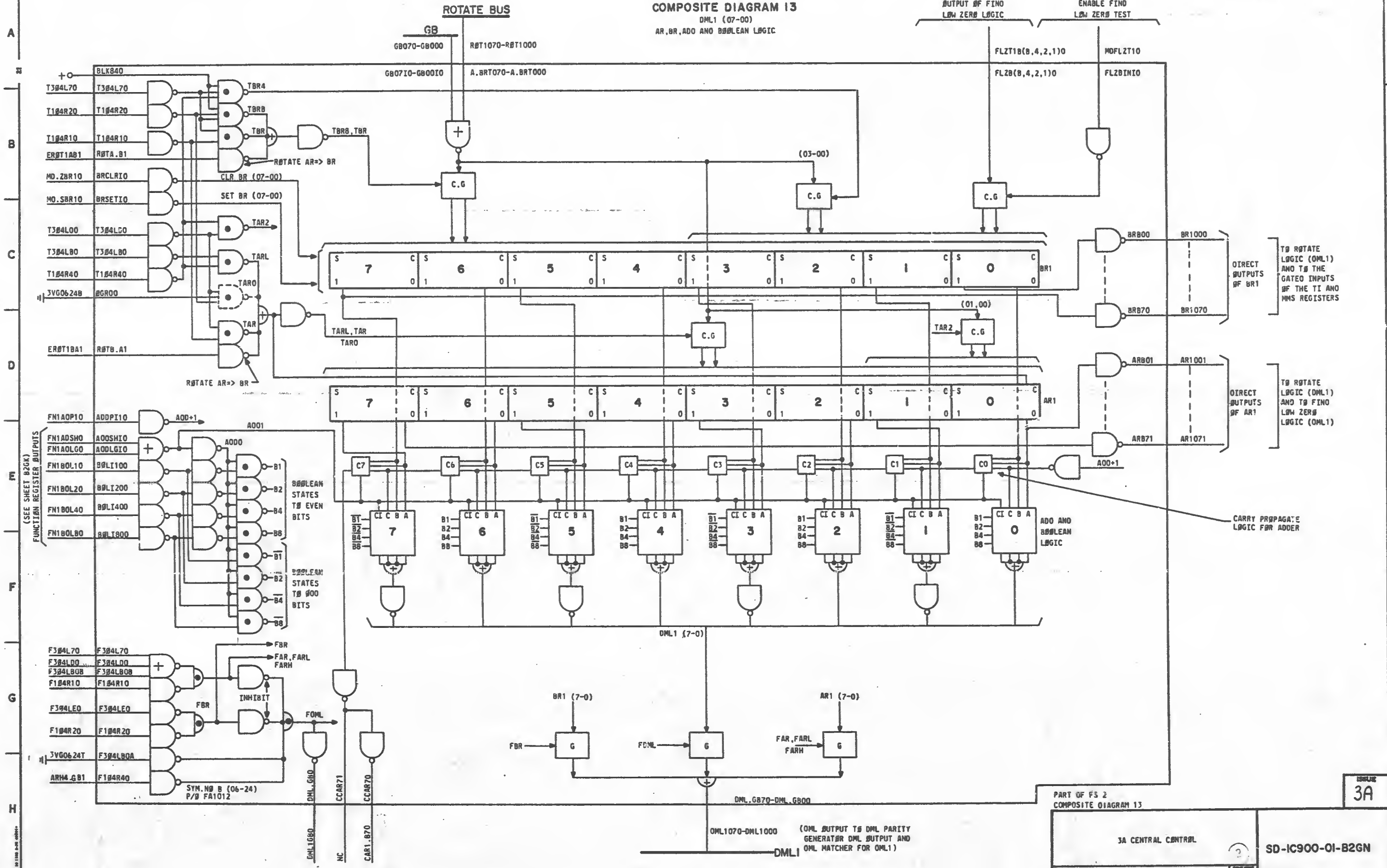
DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 13

DML1 (07-00)

AR,BR,ADD AND BOOLEAN LOGIC

CIRCUIT OPERATION
(SEE SHT B2GP)



PART OF FS 2
COMPOSITE DIAGRAM 13

3A CENTRAL CONTROL

SD-1C900-01-B2GN

ISSUE 3A

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6S

PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 14

TABLE F (OLM1)

ABBREVIATION	FUNCTION	SYM NO. 7 (06-25), FA1012 SYM NO. 8 (06-27), FA1012 TO FIELO NETNAME (PIN NO.)	SYM NO. 6 (06-28), FA1013 TO FIELO NETNAME (PIN NO.)
TBR	GB=> BR (22)	T304L70 (118), T104R10 (318)	T304L70 (116), T104R10 (016)
TAR	GB=> AR (22)	T304LB0A (109), T104R10 (318)	T304B0A (313), T104R10 (016)
TARH	GB (0-3) = AR (16-19) NO PARITY BITS CHANGEO IN AR		T304LD0 (316), T104R10 (016)
TBR8	GB (0-7,PL)=> BR (0-7,PL) ALL OTHER BITS OF AR ARE UNCHANGEO	T304L70 (118), T104R20 (019)	
TBR4	GB (0-3)=> BR (0-3) ALL OTHER BITS OF BR ARE UNCHANGEO	T304L70 (118), T104R40 (219)	
TARL	GB (0-15,PL,PH) AR (0-15,PL,PH) AR (16-19) ARE UNCHANGEO	T304LB0A (109), T104R40 (219)	
TAR2	GB (0-1)=> AR (0-1) ALL OTHER BITS OF AR ARE UNCHANGEO	T304L00 (010)*, T104R40 (219)	

* SYM NO. 8 ONLY

TABLE G (DML1)

ABBREVIATION	FUNCTION	SYM NO. 7 (06-25) FA1012 SYM NO. 8 (06-27) FA1012 FROM FIELO NETNAME (PIN NO.)	SYM NO. 6 (06-28) FA1013 FROM FIELO NETNAME (PIN NO.)
FAR	AR=> GB (22)	F304L70 (212), F104R10 (111)	F304L70 (314), F104R10 (113)
FARL	AR (0-15,PL,PH') => GB (0-15,PL,PH)	F304LB0A (311), F104R10 (111)	F304LB0B (311), F104R10 (113)
FARH	AR (0-19,PL,PH') => GB (0-19,PL,PH)	F304LD0 (312), F104R10 (111)	F304L00 (114), F104R10 (113)
FBR	BR=> GB (22)	F304LE0 (014), F104R20 (214)	F304LE0 (213), F104R20 (014)
FARH4	AR (16-19,PH4,1) => GB (0-3,PL,PH)		F304LB0 (311), F104RB0 (312)

NOTE: 1 AR(PH') = AR(PH) + AR(PH4)

CIRCUIT OPERATION

THE OPERATION OF THE GATING PATHS FOR DML 1 ARE EXACTLY AS FOR DML 0. AND, FOR THE ADD AND THE BOOLEAN LOGIC. THE ONLY EXCEPTION IS THAT FOR DML 1. THE PARITY BITS DO NOT HAVE TO BE MAINTAINED AND THEREFORE, THE LOGIC IS OMITTED. NOTE THAT THIS IS BECAUSE THE PARITY IS KEPT IN DML 0 FOR THOSE OPERATIONS THAT PRESERVE PARITY. IF PARITY MUST BE COMPUTED, PARITY IS ACTUALLY OBTAINED BY A PARITY TREE ATTACHED TO THE OUTPUT OF DML 1, AS SHOWN ON SHEET B2GA. THE ONE OTHER OPERATION THAT DML 1 DOES NOT PERFORM, THAT IS PERFORMED IN DML 0, IS THE GATING INTO THE ARO REGISTER. THAT IS, IT IS POSSIBLE TO LOAD INTO THE ARO REGISTER OF DML 0 WITHOUT LOADING INTO DML 1. THIS ALLOWS DISSIMILAR CONTENTS TO BE GATED INTO THE TWO DML'S SO THAT MAINTENANCE CAN BE PERFORMED ON THE DML LOGIC TO CHECK THE CORRECT OPERATION OF THE MATCHERS.

PART OF FS 2
COMPOSITE DIAGRAM 14

ISSUE 5A

3A CENTRAL CONTROL

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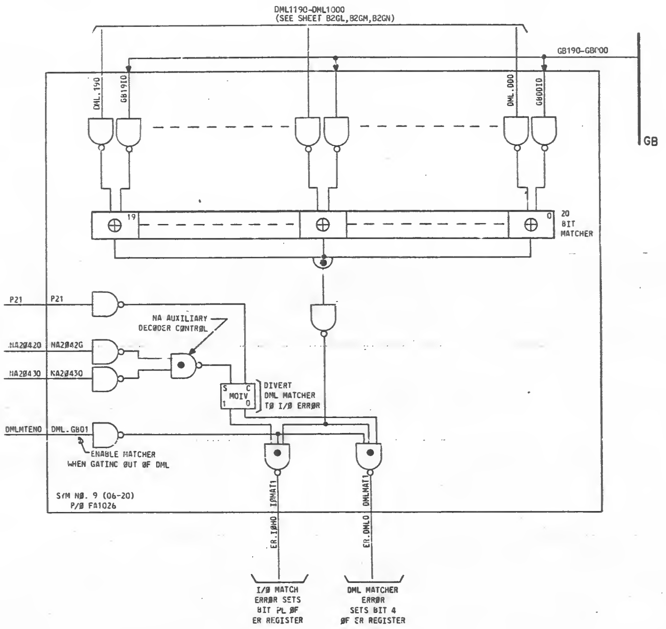
PART OF FS 2

DATA MANIPULATION LOGIC (DML)

COMPOSITE DIAGRAM 15

DML MATCHER



CIRCUIT OPERATION

THE DML MATCHES THE OUTPUT OF THE DML 0 WITH THE OUTPUT OF THE DML 1. THE MATCH IS PERFORMED BY GATING DML 0 ONTO THE GB AND THEN MATCHING THE CONTENTS OF THE GB WITH THE DML 1. SINCE THE GB IS USED FOR MANY OTHER OPERATIONS OTHER THAN DML GATING FUNCTIONS, THE MATCHER MUST BE STROBED ONLY WHEN GATING DML 0 TO THE GB.

THE DML MATCHER ERROR RESULTS IN SETTING BIT 4 OF THE ERROR REGISTER. THIS ERROR IS IN A CLASS OF ERRORS REFERRED TO AS FATAL ERRORS. THEY WILL TYPICALLY CAUSE THE 3A CC TO STOP AND SWITCH TO THE OTHER 3A CC. TO PROVIDE THE ABILITY TO USE THE DML MATCHES FOR MATCH FUNCTIONS THAT CAUSE A LESS SEVERE RECOVERY STRATEGY FOR AN ERROR DETECTED, AN ADDITIONAL CONTROL FEATURE IS INCLUDED. THIS CONTROL IS ACTIVATED BY THE NEXT ADDRESS FIELD AUXILIARY DECODER AND RESULTS IN SETTING THE MATCH DIVERT FLIP-FLOP IN COMPOSITE DIAGRAM 15. THIS FLIP-FLOP CAUSES THE DML ERROR TO BE DIVERTED TO A SO CALLED I/O MATCH ERROR (BIT PL OF THE ERROR REGISTER) WHICH IS AN ERROR INTERRUPT. IT IS USUALLY USED TO CHECK THE VALIDITY OF I/O CHANNEL OPERATIONS.

PART OF FS 2
COMPOSITE DIAGRAM 15

ISSUE 5A

3A CENTRAL CONTROL

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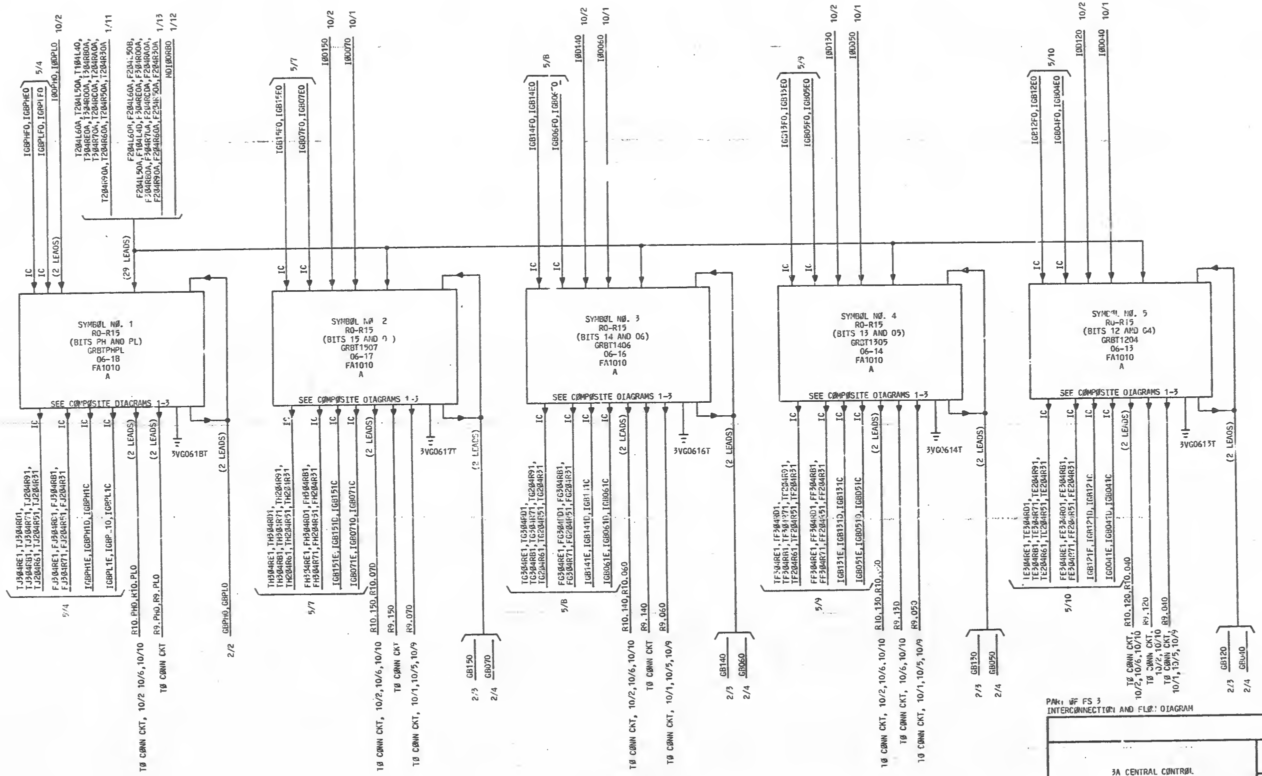
PART OF FS 3

GENERAL REGISTERS (Ru-R15)
INTERCØNNECTIØN AND FLØW OIAGRAM

NØTES:
1. FØR "FPØM" ANC "TØ" FIELO OECØDING ASSIGNMENTS SFE NØTE 312.


IGBPHFO, IGBPHEO
IGBPLFO, IGBPLFO
5/4
IØOPHO, IØDPLO
10/2
T2Ø4L60A, T2Ø4L50A, T1Ø4L40, T3Ø4REOA, T3Ø4R00A, T3Ø4RBOA, T3Ø4R70A, T2Ø4RCOA, T2Ø4RAOA, T2Ø4R90A, T2Ø4R60A, T2Ø4R50A, T2Ø4R30A
1/11
F2Ø4L60R, F2Ø4L60A, F2Ø4L50B, F2Ø4L50A, F1Ø4L4D, F3Ø4REOA, F3Ø4R00A, F3Ø4RBOA, F3Ø4R7UA, F2Ø4RCDA, F2Ø4RAOA, F2Ø4R90A, F2Ø4R60A, F2Ø4R50A, F2Ø4R30A
1/13
NDIØ0RBO
1/12
IC
IC
(2 LEADS)
(29 LEADS)
SYMBØL NØ. 1
RO-R15
(BITS PH AND PL)
GRBTPHPL
06-18
FA1010
A
SEE CØMPØSITE DIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
(2 LEADS)
3VG061BT
(2 LEADS)
TJ3Ø4RE1, TJ3Ø4RD1, TJ3Ø4RB1, TJ3Ø4R71, TJ2Ø4R91, TJ2Ø4R61, TJ2Ø4R51, TJ2Ø4R31
FJ3Ø4RE1, FJ3Ø4RD1, FJ3Ø4RB1, FJ3Ø4R71, FJ2Ø4R51, FJ2Ø4R31
IGBPH1E, IGBPH1D, IGBPH1C
IGBPL1E, IGBPL1D, IGBPL1C
5/4
R10.PHO, R10.PLO
TØ CØNN CKT, 10/2 10/6, 10/10
R9.PHO, R9.PLO
TØ CØNN CKT
GBPHO, GBPLO
2/2
IGB15FO, IGB15EO
IGB07FO, IGB07EO
5/7
IØ0150
10/2
IØ0070
10/1
IC
IC
SYMBØL NØ 2
RO-R15
(BITS 15 AND 07)
GRBT1507
06-17
FA1010
A
SEE CØMPØSITE OIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
3VG0617T
(2 LEADS)
TH3Ø4RE1, TH3Ø4RD1, TH3Ø4RB1, TH3Ø4R71, TH2Ø4R91, TH2Ø4R61, TH2Ø4R51, TH2Ø4R31
FH3Ø4RE1, FH3Ø4RD1, FH3Ø4RB1, FH3Ø4R71, FH2Ø4R51, FH2Ø4R31
IGB151E, IGB151D, IGB151C
IGB071E, IGB071D, IGB071C
5/7
R10.150, R10.070
R9.150
R9.070
TØ CØNN CKT, 10/2, 10/6, 10/10
TØ CØNN CKT
TØ CØNN CKT, 10/1, 10/5, 10/9
GB150
GB070
2/3
2/4
IGB14FO, IGB14EO
IGB06FO, IGB06EO
5/8
IØ0140
10/2
IØ0060
10/1
IC
IC
SYMBØL NØ. 3
RO-R15
(BITS 14 AND 06)
GRBT1406
06-16
FA1010
A
SEE CØMPØSITE OIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
3VG0616T
(2 LEADS)
TG3Ø4RE1, TG3Ø4RD1, TG3Ø4RB1, TG3Ø4R71, TG2Ø4R91, TG2Ø4R61, TG2Ø4R51, TG2Ø4R31
FG3Ø4RE1, FG3Ø4RD1, FG3Ø4RB1, FG3Ø4R71, FG2Ø4R51, FG2Ø4R31
IGB141E, IGB141D, IGB141C
IGB061E, IGB061D, IGB061C
5/8
R10.140, R10.060
R9.140
R9.060
TØ CØNN CKT, 10/2, 10/6, 10/10
TØ CØNN CKT
TØ CØNN CKT, 10/1, 10/5, 10/9
GB140
GB060
2/3
2/4
IGB13FO, IGB13EO
IGB05FO, IGB05EO
5/9
IØ0130
10/2
IØ0050
10/1
IC
IC
SYMBØL NØ. 4
RO-R15
(BITS 13 AND 05)
GRBT1305
06-14
FA1010
A
SEE CØMPØSITE OIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
3VG0614T
(2 LEADS)
TF3Ø4RE1, TF3Ø4RD1, TF3Ø4RB1, TF3Ø4R71, TF2Ø4R91, TF2Ø4R61, TF2Ø4R51, TF2Ø4R31
FF3Ø4RE1, FF3Ø4RD1, FF3Ø4RB1, FF3Ø4R71, FF2Ø4R51, FF2Ø4R31
IGB131E, IGB131D, IGB131C
IGB051E, IGB051D, IGB051C
5/9
R10.130, R10.050
R9.130
R9.050
TØ CØNN CKT, 10/2, 10/6, 10/10
TØ CØNN CKT, 10/6, 10/10
TØ CØNN CKT, 10/1, 10/5, 10/9
GB130
GB050
2/3
2/4
IGB12FO, IGB12EO
IGB04FO, IGB04EO
5/10
IØ0120
10/2
IØ0040
10/1
IC
IC
SYMBØL NØ. 5
RO-R15
(BITS 12 AND 04)
GRBT1204
06-13
FA1010
A
SEE CØMPØSITE OIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
3VG0613T
(2 LEADS)
TE3Ø4RE1, TE3Ø4RD1, TE3Ø4RB1, TE3Ø4R71, TE2Ø4R91, TE2Ø4R61, TE2Ø4R51, TE2Ø4R31
FE3Ø4RE1, FE3Ø4RD1, FE3Ø4RB1, FE3Ø4R71, FE2Ø4R51, FE2Ø4R31
IGB121F, IGB121D, IGB121C
IGB041E, IGB041D, IGB041C
5/10
R10.120, R10.040
R9.120
R9.040
TØ CØNN CKT, 10/2, 10/6, 10/10
TØ CØNN CKT, 10/2, 10/10
TØ CØNN CKT, 10/1, 10/5, 10/9
GB120
GB040
2/3
2/4

PART OF FS 3
INTERCØNNECTIØN AND FLØW OIAGRAM

3A CENTRAL CØNTRØL

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES

SD-1C900-01

B3AA

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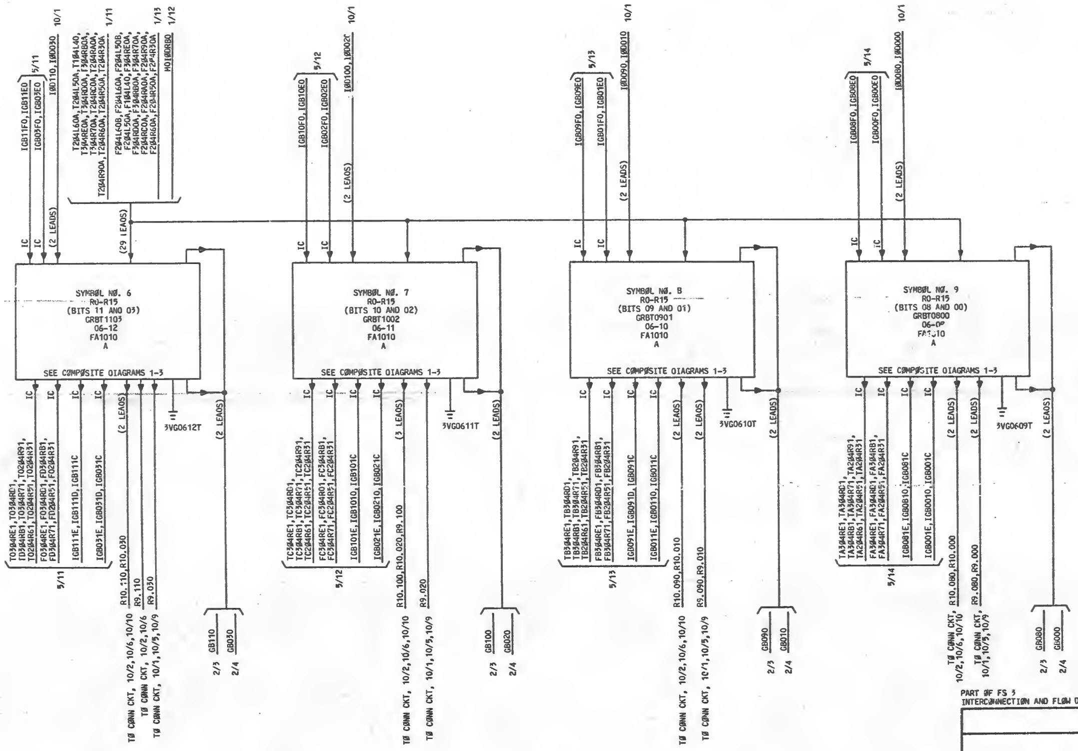
PART OF FS 3

GENERAL REGISTERS (R0-R15)
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.


IGB11F0, IGB11E0
IGB03F0, IGB03E0
5/11
I0D110, I0D030
10/1
(2 LEADS)
IC
IC
T204L60A, T204L50A, T104L40,
T304RE0A, T304RD0A, T304RB0A,
T304R70A, T204RC0A, T204RA0A,
T204R90A, T204R60A, T204R50A, T204R30A
1/11
F204L60B, F204L60A, F204L50B,
F204L50A, F104L40, F304RE0A,
F304RD0A, F304RB0A, F304R70A,
F204RC0A, F204RA0A, F204R90A,
F204R60A, F204R50A, F204R30A
1/13
HOI0DRB0
1/12
(29 LEADS)
SYMBOL NO. 6
R0-R15
(BITS 11 AND 03)
GRBT1103
06-12
FA1010
A
SEE COMPOSITE DIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
3VG0612T
(2 LEADS)
T0304RE1, T0304RD1,
TD304RB1, T0304R71, T0204R91,
T0204R61, T0204R51, T0204R31
F0304RE1, F0304RD1, FD304RB1,
FD304R71, FD204R51, F0204R31
IGB111E, IGB111D, IGB111C
IGB031E, IGB031D, IGB031C
5/11
R10.110, R10.030
R9.110
R9.030
TO CONN CKT, 10/2, 10/6, 10/10
TO CONN CKT, 10/2, 10/6
TO CONN CKT, 10/1, 10/5, 10/9
GB110
GB030
2/3
2/4
IGB10F0, IGB10E0
IGB02F0, IGB02E0
5/12
I0D100, I0D020
10/1
(2 LEADS)
IC
IC
SYMBOL NO. 7
R0-R15
(BITS 10 AND 02)
GRBT1002
06-11
FA1010
A
SEE COMPOSITE DIAGRAMS 1-3
IC
IC
IC
IC
(3 LEADS)
3VG0611T
(2 LEADS)
TC304RE1, TC304RB1,
TC304RB1, TC304R71, TC204R91,
TC204R61, TC204R51, TC204R31
FC304RE1, FC304R01, FC304RB1,
FC304R71, FC204R51, FC204R31
IGB101E, IGB1010, IGB101C
IGB021E, IGB0210, IGB021C
5/12
R10.100, R10.020, R9.100
R9.020
TO CONN CKT, 10/2, 10/6, 10/10
TO CONN CKT, 10/1, 10/5, 10/9
GB100
GB020
2/3
2/4
IGB09F0, IGB09E0
IGB01F0, IGB01E0
5/13
I0D090, I0D010
10/1
(2 LEADS)
IC
IC
SYMBOL NO. 8
R0-R15
(BITS 09 AND 01)
GRBT0901
06-10
FA1010
A
SEE COMPOSITE DIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
(2 LEADS)
3VG0610T
(2 LEADS)
TB304RE1, TB304RD1,
TB304RB1, TB304R71, TB204R91,
TB204R61, TB204R51, TB204R31
FB304RE1, FB304RD1, FB304RB1,
FB304R71, FB204R51, FB204R31
IGB091E, IGB091D, IGB091C
IGB011E, IGB0110, IGB011C
5/13
R10.090, R10.010
R9.090, R9.010
TO CONN CKT, 10/2, 10/6, 10/10
TO CONN CKT, 10/1, 10/5, 10/9
GB090
GB010
2/3
2/4
IGB08F0, IGB08E0
IGB00F0, IGB00E0
5/14
I0D080, I0D000
10/1
(2 LEADS)
IC
IC
SYMBOL NO. 9
R0-R15
(BITS 08 AND 00)
GRBT0800
06-0P
FA1010
A
SEE COMPOSITE DIAGRAMS 1-3
IC
IC
IC
IC
(2 LEADS)
(2 LEADS)
3VG0609T
(2 LEADS)
TA304RE1, TA304RC1,
TA304RB1, TA304R71, TA204R91,
TA204R61, TA204R51, TA204R31
FA304RE1, FA304RE1, FA304RB1,
FA304R71, FA204R51, FA204R31
IGB081E, IGB0B10, IGB081C
IGB001E, IGB0010, IGB001C
5/14
R10.080, R10.000
R9.080, R9.000
TO CONN CKT, 10/2, 10/6, 10/10
TO CONN CKT, 10/1, 10/5, 10/9
GB080
GB000
2/3
2/4

PART OF FS 3
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B3AB

PART OF FS 3

GENERAL REGISTERS (R0-R15)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
GBPH0	PARITY HIGH OF THE GATING BUS
GBPL0	PARITY LOW OF THE GATING BUS
GB000-GB150	BITS 0-15 OF THE GATING BUS
IGBPH(E,F)0	INPUTS TO PARITY HIGH OF THE GATING BUS [IC]
IGBPH1C-IGBPH1E	OUTPUTS OF PARITY HIGH OF THE GATING BUS [IC]
IGBPLE0	OUTPUTS OF GATING BUS BIT PL [IC]
IGBPLF0	OUTPUTS OF GATING BUS BIT PL [IC]
IGBPL1C-IGBPL1E	OUTPUTS FROM PARITY LOW OF THE GATING BUS [IC]
IGB00E0-IGB15E0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGF00F0-IGB15F0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB001C-IGB151C	OUTPUTS OF GATING BUS 00-15 [IC]
IGB001D-IBG151D	OUTPUTS OF GATING BUS 00-15 [IC]
IBG001E-IBG151E	OUTPUTS OF GATING BUS 00-15 [IC]
IODPH0	PARITY HIGH OF THE IOD REGISTER
IODPL0	PARITY LOW OF THE IOD REGISTERS
IOD000-IOD150	BITS 0-15 OF THE IOD REGISTER
MDIODRB0	MISC. DECODER, GATE THE IOD TO R11
R10.PH0	PARITY HIGH OF GENERAL REGISTER 10
R10.PL0	PARITY LOW OF GENERAL REGISTER 10
R10.000-R10.150	BITS 0-15 OF GENERAL REGISTER 10
R9.PH0	PARITY HIGH OUTPUT OF GENERAL REGISTER 9
R9.PL0	PARITY LOW OUTPUT OF GENERAL REGISTER 9
R9.000-R9.150	BITS 0-15 OF GENERAL REGISTER 9

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B3AC

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11/17/75

PART OF FS 3

GENERAL REGISTERS(R0-R15)

SYMBOL NO. 1

R0-R15
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBTPHPL	06-18	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FJ204R31	O	IC	5/4		F204R31	2G7
FJ204R51	O	IC	5/4		F204R51	2G8
FJ304RB1	O	IC	5/4		F304RB1	3G3
FJ304RD1	O	IC	5/4		F304RD1	3G3
FJ304RE1	O	IC	5/4		F304RE1	2G7
FJ304R71	O	IC	5/4		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2
GBPH0	OT	113	2/2		TGB.B0	8H6
	I	208	2/2		GB.BI0	2A4
GBPL0	OT	214	2/2		TGB.A0	8H5
	I	008	2/2		GB.AI0	2A5
IGBPHE0	I	IC	5/4		TA9	8A5
IGBPHF0	I	IC	5/4		TB9	8A6
IGBPH1C	O	IC	5/4		GB.B01C	2H3
IGBPH10	O	IC	5/4		GB.B010	2H3
IGBPH1E	O	IC	5/4		GB.B01A	2H4
IGBPLE0	I	IC	5/4		TA8	8A5
IGBPLF0	I	IC	5/4		TB8	8A6
IGBPL1C	O	IC	5/4		GB.AD1C	2H5
IGBPL10	O	IC	5/4		GB.AD10	2H5
IGBPL1E	O	IC	5/4		GB.AD1A	2H4
IODPH0	I	108	10/2	202	IOD.BI0	2A4
IODPL0	I	307	10/2	202	IOD.AI0	2A5
MDIODRB0	I	218	1/12		IOD.R110	6A6
R10.PH0	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R10.PL0	O	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R9.PH0	O	015	TO CONN CKT	202	R9.BN10A	8H4
R9.PLC	O	014	TO CONN CKT	202	R9.AN10A	8H4
TJ204R31	O	IC	5/4		T204R31	2H0
TJ204R51	O	IC	5/4		T204R51	2H0
TJ204R61	O	IC	5/4		T204R61	2H1
TJ204R91	O	IC	5/4		T204R91	2H1
TJ304RB1	O	IC	5/4		T304RB1	3G1
TJ304RD1	O	IC	5/4		T304RD1	3G2
TJ304RE1	O	IC	5/4		T304RE1	2H0
TJ304R71	O	IC	5/4		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1

SYMBOL NO. 1 (CONT)

R0-R15
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBTPHPL	06-18	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T062B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0618T	GRD	012			GRD012	2H3
	GRD	017			GRD017	2H2
	GRD	114			GRD114	2H2
	GRD	212			GRD212	2H3
	GRD	217			GRD217	2H2
	GRD	314			GRD314	2H2
	GRD	319	TO CONN CKT		GRD	
3V062A	PWR	000	14/8		+3	
	PWR	119	14/8		+3	
3V062B	PWR	000	(X)14/8	203	+3	
	PWR	119	(X)14/8	203	+3	

SYMBOL NO. 2

R0-R15
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1507	06-17	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FH204R31	O	IC	5/7		F204R31	2G7
FH204R51	O	IC	5/7		F204R51	2G8
FH304RB1	O	IC	5/7		F304RB1	3G3
FH304RD1	O	IC	5/7		F304RD1	3G3
FH304RE1	O	IC	5/7		F304RE1	2G7
FH304R71	O	IC	5/7		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2
GB070	OT	214	2/4		TGB.A0	8H5
	I	008	2/4		GB.AI0	2A5
GB150	OT	113	2/3		TGB.B0	8H6

SYMBOL NO. 2 (CONT)

R0-R15
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1507	06-17	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
GB150	I	208	2/3		GB.BI0	2A4
IGB07E0	I	IC	5/7		TA8	8A5
IGB07F0	I	IC	5/7		TB8	8A6
IGB071C	O	IC	5/7		GB.AD1C	2H5
IGB0710	O	IC	5/7		GB.AD10	2H5
IGB071E	O	IC	5/7		GB.AD1A	2H4
IGB15E0	I	IC	5/7		TA9	8A5
IGB15F0	I	IC	5/7		TB9	8A6
IGB151C	O	IC	5/7		GB.BD1C	2H3
IGB1510	O	IC	5/7		GB.BD10	2H3
IGB151E	O	IC	5/7		GB.BD1A	2H4
IOD070	I	307	10/1	202	IOD.AI0	2A5
IOD150	I	108	10/2	202	IOD.BI0	2A4
MDIODRB0	I	218	1/12		IOD.R110	6A6
R10.070	O	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.150	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.070	O	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.150	O	015	TO CONN CKT	202	R9.BN10A	8H4
TH204R31	O	IC	5/7		T204R31	2H0
TH204R51	O	IC	5/7		T204R51	2H0
TH204R61	O	IC	5/7		T204R61	2H1
TH204R91	O	IC	5/7		T204R91	2H1
TH304RB1	O	IC	5/7		T304RB1	3G1
TH304RD1	O	IC	5/7		T304RD1	3G2
TH304RE1	O	IC	5/7		T304RE1	2H0
TH304R71	O	IC	5/7		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T058A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0617T	GRD	012	3/2		GRD012	2H3
	GRD	017	3/2		GRD017	2H2
	GRD	114	3/2		GRD114	2H2
	GRD	212	3/2		GRD212	2H3
	GRD	217	5/7		GRD217	2H2
	GRD	314	3/2		GRD314	2H2
	GRD	319	3/2		GRD	
3V058A	PWR	000	(X)14/4	203	+3	
	PWR	119	(X)14/4	203	+3	
3V058B	PWR	000	14/4		+3	
	PWR	119	14/4		+3	

PART OF FS 3
SYMBOL(S) 1 2

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B3CA

PRINTED IN U. S. A.

12/01/77

PART OF FS 3

GENERAL REGISTERS(R0-R15)

SYMBOL NO. 3

R0-R15
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1406	06-16	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FG204R31	O	IC	5/8		F204R31	2G7
FG204R51	O	IC	5/8		F204R51	2G8
FG304RB1	O	IC	5/8		F304RB1	3G3
FG304RD1	O	IC	5/8		F304RD1	3G3
FG304RE1	O	IC	5/8		F304RE1	2G7
FG304R71	O	IC	5/8		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2
GB060	OT	214	2/4		TGB.A0	8H5
	I	008	2/4		GB.AI0	2A5
GB140	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
IGB06E0	I	IC	5/8		TA8	8A5
IGB06F0	I	IC	5/8		TB8	8A6
IGB061C	O	IC	5/8		GB.AD1C	2H5
IGB0610	O	IC	5/8		GB.AD10	2H5
IGB061E	O	IC	5/8		GB.AD1A	2H4
IGB14E0	I	IC	5/8		TA9	8A5
IGB14F0	I	IC	5/8		TB9	8A6
IGB141C	O	IC	5/8		GB.BD1C	2H3
IGB1410	O	IC	5/8		GB.BD10	2H3
IGB141E	O	IC	5/8		GB.BD1A	2H4
IOD060	I	307	10/1	202	IOD.AI0	2A5
IOD140	I	108	10/2	202	IOD.BI0	2A4
MDIOORB0	I	218	1/12		IOD.R110	6A6
R10.060	O	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.140	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.060	O	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.140	O	015	TO CONN CKT	202	R9.BN10A	8H4
TG204R31	O	IC	5/8		T204R31	2H0
TG204R51	O	IC	5/8		T204R51	2H0
TG204R61	O	IC	5/8		T204R61	2H1
TG204R91	O	IC	5/8		T204R91	2H1
TG304RB1	O	IC	5/8		T304RB1	3G1
TG304RD1	O	IC	5/8		T304RD1	3G2
TG304RE1	O	IC	5/8		T304RE1	2H0
TG304R71	O	IC	5/8		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2

SYMBOL NO. 3 (CONT)

R0-R15
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1406	06-16	FA1010	A	

FS INFG					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T058A	GRD	0G0		203	GRD	
	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0616T	GRD	012			GRD012	2H3
	GRD	017			GRD017	2H2
	GRD	114			GRD114	2H2
	GRD	212			GRD212	2H3
	GRD	217			GRD217	2H2
	GRD	314			GRD314	2H2
	GRD	319			GRD	
3V058A	PWR	000	(X)14/4	203	+3	
	PWR	119	(X)14/4	203	+3	
3V058B	PWR	000	14/4		+3	
	PWR	119	14/4		+3	

SYMBOL NO. 4

R0-R15
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1305	06-14	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FF204R31	O	IC	5/9		F204R31	2G7
FF204R51	O	IC	5/9		F204R51	2G8
FF304RB1	O	IC	5/9		F304RB1	3G3
FF304RD1	O	IC	5/9		F304RD1	3G3
FF304RE1	O	IC	5/9		F304RE1	2G7
FF304R71	O	IC	5/9		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2

SYMBOL NO. 4 (CONT)

R0-R15
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1305	06-14	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
GB050	OT	214	2/4		TGB.A0	8H5
GB050	I	008	2/4		GB.AI0	2A5
GB130	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
IGB05E0	I	IC	5/9		TA8	8A5
IGB05F0	I	IC	5/9		TB8	8A6
IGB051C	O	IC	5/9		GB.AD1C	2H5
IGB0510	O	IC	5/9		GB.AD10	2H5
IGB051E	O	IC	5/9		GB.AD1A	2H4
IGB13E0	I	IC	5/9		TA9	8A5
IGB13F0	I	IC	5/9		TB9	8A6
IGB131C	O	IC	5/9		GB.BD1C	2H3
IGB1310	O	IC	5/9		GB.BD10	2H3
IGB131E	O	IC	5/9		GB.BD1A	2H4
IOD050	I	307	10/1	202	IOD.AI0	2A5
IOD130	I	108	10/2	202	IOD.BI0	2A4
MDIOORB0	I	218	1/12		IOD.R110	6A6
R10.050	O	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.130	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.050	O	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.130	O	015	10/6,10/10 TO CONN CKT	202	R9.BN10A	8H4
TF204R31	O	IC	5/9		T204R31	2H0
TF204R51	O	IC	5/9		T204R51	2H0
TF204R61	O	IC	5/9		T204R61	2H1
TF204R91	O	IC	5/9		T204R91	2H1
TF304RB1	O	IC	5/9		T304RB1	3G1
TF304RD1	O	IC	5/9		T304RD1	3G2
TF304RE1	O	IC	5/9		T304RE1	2H0
TF304R71	O	IC	5/9		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T058A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0614T	GRD	012			GRD012	2H3
	GRD	017			GRD017	2H2
	GRD	114			GRD114	2H2
	GRD	212			GRD212	2H3
	GRD	217			GRD217	2H2
	GRD	314			GRD314	2H2
	GRD	319			GRD	
3V058A	PWR	000	(X)14/4	203	+3	

SYMBOL NO. 4 (CONT)

R0-R15
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1305	06-14	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V058A	PWR	119	(X)14/4	203	+3	
3V058B	PWR	000	14/4		+3	
	PWR	119	14/4		+3	

PART OF FS 3
SYMBOL(S) 3 4

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B3CB

PRINTED IN U. S. A.

12/01/77

PART OF FS 3

GENERAL REGISTERS(R0-R15)

SYMBOL NO. 5

R0-R15
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1204	06-13	FA1010	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FE204R31	0	1C	5/10		F204R31	2G7
FE204R51	0	1C	5/10		F204R51	2G8
FE304RB1	0	1C	5/10		F304RB1	3G3
FE304RD1	0	1C	5/10		F304RD1	3G3
FE304RE1	0	1C	5/10		F304RE1	2G7
FE304R71	0	1C	5/10		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2
GB040	OT	214	2/4		TGB.A0	8H5
	I	008	2/4		GB.AI0	2A5
GB120	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
1GB04E0	I	1C	5/10		TA8	8A5
1GB04F0	I	1C	5/10		TB8	8A6
1GB041C	0	1C	5/10		GB.AD1C	2H5
1GB0410	0	1C	5/10		GB.AD10	2H5
1GB041E	0	1C	5/10		GB.AD1A	2H4
1GB12E0	I	1C	5/10		TA9	8A5
1GB12F0	I	1C	5/10		TB9	8A6
1GB121C	0	1C	5/10		GB.B01C	2H3
1GB1210	0	1C	5/10		GB.B010	2H3
1GB121E	0	1C	5/10		GB.B01A	2H4
10D040	I	307	10/1	202	10D.AI0	2A5
10D120	I	108	10/2	202	10D.BI0	2A4
MD10DRB0	I	218	1/12		10D.R110	6A6
R10.040	0	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.120	0	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.040	0	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.120	0	015	10/2,10/10 TO CONN CKT	202	R9.BN10A	8H4
TE204R31	0	1C	5/10		T204R31	2H0
TE204R51	0	1C	5/10		T204R51	2H0
TE204R61	0	1C	5/10		T204R61	2H1
TE204R91	0	1C	5/10		T204R91	2H1
TE304RB1	0	1C	5/10		T304RB1	3G1
TE304RD1	0	1C	5/10		T304RD1	3G2
TE304RE1	0	1C	5/10		T304RE1	2H0
TE304R71	0	1C	5/10		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2

SYMBOL NO. 5 (CONT)

R0-R15
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1204	06-13	FA1010	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T058A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0613T	GRD	012			GRD012	2H3
	GRD	017			GRD017	2H2
	GRD	114			GRD114	2H2
	GRD	212			GRD212	2H3
	GRD	217			GRD217	2H2
	GRD	314			GRD314	2H2
	GRD	319			GRD	
3V058A	PWR	000	(X)14/4	203	+3	
	PWR	119	(X)14/4	203	+3	
3V058B	PWR	000	14/4		+3	
	PWR	119	14/4		+3	

SYMBOL NO. 6

R0-R15
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1103	06-12	FA1010	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F0204R31	0	1C	5/11		F204R31	2G7
F0204R51	0	1C	5/11		F204R51	2G8
F0304RB1	0	1C	5/11		F304RB1	3G3
F0304RD1	0	1C	5/11		F304RD1	3G3
F0304RE1	0	1C	5/11		F304RE1	2G7
F0304R71	0	1C	5/11		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2

SYMBOL NO. 6 (CONT)

R0-R15
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1103	06-12	FA1010	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
GB030	OT	214	2/4		TGB.A0	8H5
GB030	I	008	2/4		GB.AI0	2A5
GB110	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
1GB03E0	I	1C	5/11		TA8	8A5
1GB03F0	I	1C	5/11		TB8	8A6
1GB031C	0	1C	5/11		GB.AD1C	2H5
1GB0310	0	1C	5/11		GB.AD10	2H5
1GB031E	0	1C	5/11		GB.AD1A	2H4
1GB11E0	I	1C	5/11		TA9	8A5
1GB11F0	I	1C	5/11		TB9	8A6
1GB111C	0	1C	5/11		GB.B01C	2H3
1GB1110	0	1C	5/11		GB.B010	2H3
1GB111E	0	1C	5/11		GB.B01A	2H4
10D030	I	307	10/1	202	10D.AI0	2A5
10D110	I	108	10/1	202	10D.BI0	2A4
MD10DRB0	I	218	1/12		10D.R110	6A6
R10.030	0	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.110	0	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.030	0	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.110	0	015	10/2,10/6 TO CONN CKT	202	R9.BN10A	8H4
T0204R31	0	1C	5/11		T204R31	2H0
T0204R51	0	1C	5/11		T204R51	2H0
T0204R61	0	1C	5/11		T204R61	2H1
T0204R91	0	1C	5/11		T204R91	2H1
T0304RB1	0	1C	5/11		T304RB1	3G1
T0304RD1	0	1C	5/11		T3G4RD1	3G2
T0304RE1	0	1C	5/11		T304RE1	2H0
T0304R71	0	1C	5/11		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T058A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0612T	GRD	012			GRD012	2H3
	GRD	017			GRD017	2H2
	GRD	114			GRD114	2H2
	GRD	212			GRD212	2H3
	GRD	217			GRD217	2H2
	GRD	314			GRD314	2H2
	GRD	319			GRD	
3V058A	PWR	000	(X)14/4	203	+3	

SYMBOL NO. 6 (CONT)

R0-R15
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1103	06-12	FA1010	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V058A	PWR	119	(X)14/4	203	+3	
3V058B	PWR	000	14/4		+3	
	PWR	119	14/4		+3	

PART OF FS 3
SYMBOL(S) 5 6

3A CENTRAL CONTROL
DWG SIZE C2
ISSUE 7D
BELL LABORATORIES
SD-1C900-01
B3CC
PRINTED IN U. S. A.
12/01/77

PART OF FS 3

GENERAL REGISTERS(R0-R15)

SYMBOL NO. 7

R0-R15
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1002	06-11	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FC204R31	O	IC	5/12		F204R31	2G7
FC204R51	O	IC	5/12		F204R51	2G8
FC304RB1	O	IC	5/12		F304RB1	3G3
FC304RD1	O	IC	5/12		F304RD1	3C3
FC304RE1	O	IC	5/12		F304RE1	2G7
FC304R71	O	IC	5/12		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2
GB020	OT	214	2/4		TGB.A0	8H5
	I	008	2/4		GB.AI0	2A5
GB100	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
IGB02E0	I	IC	5/12		TA8	8A5
IGB02F0	I	IC	5/12		TB8	8A6
IGB021C	O	IC	5/12		GB.AD1C	2H5
IGB0210	O	IC	5/12		GB.AD10	2H5
IGB021E	O	IC	5/12		GB.AD1A	2H4
IGB10E0	I	IC	5/12		TA9	8A5
IGB10F0	I	IC	5/12		TB9	8A6
IGB101C	O	IC	5/12		GB.B01C	2H3
IGB101D	O	IC	5/12		GB.B010	2H3
IGB101E	O	IC	5/12		GB.B01A	2H4
IOD020	I	307	10/1	202	IOD.AI0	2A5
IOD100	I	1C8	10/1	202	IOD.BI0	2A4
MOIOORB0	I	218	1/12		IOD.R110	6A6
R10.020	O	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.100	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.020	O	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.100	O	015	10/2,10/6 10/10 TO CONN CKT	202	R9.BN10A	8H4
TC204R31	O	IC	5/12		T204R31	2H0
TC204R51	O	IC	5/12		T204R51	2H0
TC204R61	O	IC	5/12		T204R61	2H1
TC204R91	O	IC	5/12		T204R91	2H1
TC304RB1	O	IC	5/12		T304RB1	3G1
TC304RD1	O	IC	5/12		T304RD1	3G2
TC304RE1	O	IC	5/12		T304RE1	2H0
TC304R71	O	IC	5/12		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2

SYMBOL NO. 7 (CONT)

R0-R15
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT1002	06-11	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T0588	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0611T	GRD	314	5/12		GRD314	2H2
	GRD	012	3/7		GRD012	2H3
	GRD	017	3/7		GRD017	2H2
	GRD	114	3/7		GRD114	2H2
	GRD	212	3/7		GRD212	2H3
	GRD	217	3/7		GRD217	2H2
	GRD	319	3/7		GRD	
3V0588	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 8

R0-R15
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT0901	06-10	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FB204R31	O	IC	5/13		F204R31	2G7
FB204R51	O	IC	5/13		F204R51	2G8
FB304RB1	O	IC	5/13		F304RB1	3G3
FB304RD1	O	IC	5/13		F304RD1	3G3
FB304RE1	O	IC	5/13		F304RE1	2G7
FB304R71	O	IC	5/13		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F204L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F204L60A	I	205	1/13		F204L60A	2A7
F204L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F204RC0	2A6
F204R30A	I	310	1/13		F204R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F204R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F204R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304RD0A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F304R70	3A2

SYMBOL NO. 8 (CONT)

R0-R15
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT0901	06-10	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
GB010	OT	214	2/4		TGB.A0	8H5
GB010	I	008	2/4		GB.AI0	2A5
GB090	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
IGB01E0	I	IC	5/13		TA8	8A5
IGB01F0	I	IC	5/13		TB8	8A6
IGB011C	O	IC	5/13		GB.AD1C	2H5
IGB0110	O	IC	5/13		GB.AD10	2H5
IGB011E	O	IC	5/13		GB.AD1A	2H4
IGB09E0	I	IC	5/13		TA9	8A5
IGB09F0	I	IC	5/13		TB9	8A6
IGB091C	O	IC	5/13		GB.B01C	2H3
IGB0910	O	IC	5/13		GB.B010	2H3
IGB091E	O	IC	5/13		GB.B01A	2H4
IOD010	I	307	10/1	202	IOD.AI0	2A5
IOD090	I	108	10/1	202	IOD.BI0	2A4
MDIOORB0	I	218	1/12		IOD.R110	6A6
R10.010	O	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.090	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.010	O	014	10/1,10/5 10/9 TO CONN CKT	202	R9.AN10A	8H4
R9.090	O	015	10/1,10/5 10/9 TO CONN CKT	202	R9.BN10A	8H4
TB204R31	O	IC	5/13		T204R31	2H0
TB204R51	O	IC	5/13		T204R51	2H0
TB204R61	O	IC	5/13		T204R61	2H1
TB204R91	O	IC	5/13		T204R91	2H1
TB304RB1	O	IC	5/13		T304RB1	3G1
TB304RD1	O	IC	5/13		T304RD1	3G2
TB304RE1	O	IC	5/13		T304RE1	2H0
TB304R71	O	IC	5/13		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T204L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2
T204RC0A	I	111	1/11		T204RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304RB0A	I	002	1/11		T304RB0	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T304RE0A	I	101	1/11		T304RE0	2A0
T304R70A	I	202	1/11		T304R70	3A2
3T0588	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0610T	GRD	012			GRD012	2H3
	GRD	017			GRD017	2H2
	GRD	114			GRD114	2H2
	GRD	212			GRD212	2H3
	GRD	217			GRD217	2H2
	GRD	314			GRD314	2H2
	GRD	319			GRD	
3V0588	PWR	000		203	+3	

SYMBOL NO. 8 (CONT)

R0-R15
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GRBT0901	06-10	FA1010	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V0588	PWR	119		203	+3	

PART OF FS 3
SYMBOL(S) 7 8

3A CENTRAL CONTROL

DWG SIZE C2	ISSUE 7D	
BELL LABORATORIES	SD-1C900-01	B3CD

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12/01/77

PART OF FS 3

GENERAL REGISTERS(R0-R15)

SYMBOL NO. 9

R0-R15
(BITS 08 AND 00)

OESIG	EQPT LOC	COOE	ELEM IOENT	OPT
GRBT0800	06-09	FA1010	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LDC
	---- FS INFD				---- CP INFD ----	
FA204R31	D	IC	5/14		F204R31	2G7
FA2D4R51	D	IC	5/14		F204R51	2G8
FA304RB1	O	IC	5/14		F304RB1	3G3
FA304R01	O	IC	5/14		F304R01	3G3
FA304RE1	D	IC	5/14		F304RE1	2G7
FA304R71	D	IC	5/14		F304R71	3G2
F104L40	I	302	1/13		F104L40	3A4
F204L50A	I	005	1/13		F2D4L50A	2A7
F204L50B	I	203	1/13		F204L50B	3A5
F2D4L60A	I	205	1/13		F204L60A	2A7
F2D4L60B	I	103	1/13		F204L60B	3A5
F204RA0A	I	305	1/13		F204RA0	2A6
F204RC0A	I	105	1/13		F2D4RC0	2A6
F204R30A	I	310	1/13		F2D4R30	2A8
F204R50A	I	110	1/13		F204R50	2A8
F2D4R60A	I	206	1/13		F204R60	2A5
F204R90A	I	006	1/13		F2D4R90	2A6
F304RB0A	I	001	1/13		F304RB0	3A3
F304R00A	I	300	1/13		F304RD0	3A3
F304RE0A	I	100	1/13		F304RE0	2A7
F304R70A	I	201	1/13		F3D4R70	3A2
GB000	DT	214	2/4		TGB.A0	8H5
	I	008	2/4		GB.AI0	2A5
GB080	OT	113	2/3		TGB.B0	8H6
	I	208	2/3		GB.BI0	2A4
IGB00E0	I	IC	5/14		TA8	8A5
IGB00F0	I	IC	5/14		TB8	8A6
IGB001C	O	IC	5/14		GB.AD1C	2H5
IGB001D	O	IC	5/14		GB.AD1D	2H5
IGB001E	O	IC	5/14		GB.A01A	2H4
IGB08E0	I	IC	5/14		TA9	8A5
IGB08F0	I	IC	5/14		TB9	8A6
IGB081C	O	IC	5/14		GB.BD1C	2H3
IGB081D	O	IC	5/14		GB.BD1D	2H3
IGB081E	O	IC	5/14		GB.BD1A	2H4
IOD000	I	307	10/1	202	IOD.AI0	2A5
IOD080	I	108	10/1	202	IOD.BI0	2A4
MDIODR80	I	218	1/12		IOD.R110	6A6
R10.000	D	313	10/2,10/6 10/10 TO CONN CKT	202	R10AN10A	8H3
R10.080	O	215	10/2,10/6 10/10 TO CONN CKT	202	R10BN10A	8H2
R9.000	O	014	10/1,10/5 10/9 TD CONN CKT	202	R9.AN10A	8H4
R9.080	O	015	10/1,10/5 10/9 TD CONN CKT	202	R9.BN10A	8H4
TA204R31	O	IC	5/14		T204R31	2H0
TA204R51	O	IC	5/14		T2D4R51	2H0
TA204R61	O	IC	5/14		T204R61	2H1
TA204R91	D	IC	5/14		T204R91	2H1
TA304RB1	O	IC	5/14		T304RB1	3G1
TA304RD1	D	IC	5/14		T304RD1	3G2
TA304RE1	D	IC	5/14		T304RE1	2H0
TA304R71	O	IC	5/14		T304R71	3G1
T104L40	I	211	1/11		T104L40	2A2
T204L50A	I	303	1/11		T2D4L50	3A4
T204L60A	I	102	1/11		T204L60	3A4
T204RA0A	I	311	1/11		T204RA0	2A2

SYMBOL NO. 9 (CONT)

R0-R15
(BITS 08 AND 00)

OESIG	EDPT LOC	COOE	ELEM IOENT	OPT
GRBT0800	06-09	FA1010	A	

LEAD OESIG	FUNC	TERM.	DESTINATIDN	NOTE	TERM. MOD	LDC
	---- FS INFO				---- CP INFD ----	
T2D4RC0A	I	111	1/11		T2D4RC0	2A2
T204R30A	I	213	1/11		T204R30	2A0
T204R50A	I	013	1/11		T204R50	2A1
T204R60A	I	312	1/11		T204R60	2A1
T204R90A	I	112	1/11		T204R90	2A1
T304R80A	I	002	1/11		T304R80	3A1
T304RD0A	I	301	1/11		T304RD0	3A2
T3D4RE0A	I	101	1/11		T3D4RE0	2A0
T304R70A	I	202	1/11		T3D4R70	3A2
3T058B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0609T	GRD	012			GR0012	2H3
	GRD	017			GR0017	2H2
	GRD	114			GR0114	2H2
	GRD	212			GR0212	2H3
	GRO	217			GR0217	2H2
	GRD	314			GRD314	2H2
	GRO	319			GRD	
3V058B	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 3
SYMBOL(S) 9

3A CENTRAL CONTROL

		DWG SIZE	ISSUE
		C2	7D
BELL LABORATORIES	SD-1C900-01		B3CE

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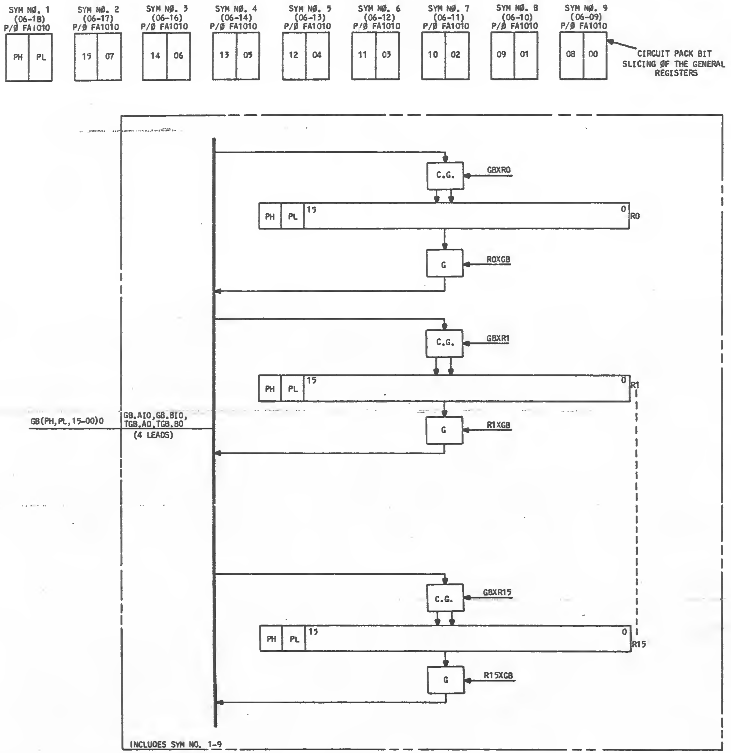
12/01/77

PART OF FS 3

GENERAL REGISTERS (R0-R15)

COMPOSITE DIAGRAM 1

16 GENERAL REGISTERS (R0-R15)


SYM NO. 1 (06-18) P/O FA1010
PH PL
SYM NO. 2 (06-17) P/O FA1010
15 07
SYM NO. 3 (06-16) P/O FA1010
14 06
SYM NO. 4 (06-14) P/O FA1010
13 05
SYM NO. 5 (06-13) P/O FA1010
12 04
SYM NO. 6 (06-12) P/O FA1010
11 03
SYM NO. 7 (06-11) P/O FA1010
10 02
SYM NO. 8 (06-10) P/O FA1010
09 01
SYM NO. 9 (06-09) P/O FA1010
08 00
CIRCUIT PACK BIT SLICING OF THE GENERAL REGISTERS
C.G.
GBXR0
PH PL 15 0
R0
G
R0XGB
C.G.
GBXR1
PH PL 15 0
R1
G
R1XGB
GB(PH,PL,15-00)0
GB.AIO,GB.BIO,
TGB.AO,TGB.BO
(4 LEADS)
C.G.
GBXR15
PH PL 15 0
R15
G
R15XGB
INCLUDES SYM NO. 1-9

CIRCUIT OPERATION

THERE ARE 16 GENERAL REGISTERS IN THE 3ACC. THESE REGISTERS ARE 18-BITS WIDE WITH 16 BITS OF DATA AND 2 PARITY BITS. THEY ARE PRIMARILY USED FOR HIGH SPEED SCRATCH PAD STORAGE FOR MAIN MEMORY PROGRAMS. THEY ARE DESIGNATED R0 THROUGH R15. THE GENERAL REGISTERS LIKE MOST OF THE OTHER REGISTERS IN THE 3ACC ARE BIT SLICED. THE BIT SLICING OR PARTITIONING OF THE INDIVIDUAL BITS OF THE GENERAL REGISTERS IS INDICATED IN THE UPPER PORTION OF COMPOSITE DIAGRAM NO. 1. BIT SLICING ENSURES THAT ALL FAULTS, INCLUDING MULTIPLE FAULTS, AS LONG AS THEY OCCUR WITHIN A SINGLE CIRCUIT PACK, WILL BE DETECTED BY THE PARITY CHECK CODE. ACCESS TO THE GENERAL REGISTERS IS PROVIDED VIA THE GB. THE CONTROL ONTO AND THEN OFF OF THE GB IS ACTIVATED BY FROM-AND TO-FIELD CROSSPOINTS RESPECTIVELY AS DESCRIBED ON SHEET B3GB. THE CONTROL REQUIRES A PAIR OF FROM-FIELD CONTROL SIGNALS AND A PAIR OF TO-FIELD CONTROL SIGNALS TO PERFORM A REGISTER TO REGISTER GATING FUNCTION VIA THE GB. TABLE A SHOWS THE FROM-AND TO-FIELD CONTROL SIGNALS THAT ARE REQUIRED TO ENABLE DATA FROM A GIVEN GENERAL REGISTER ONTO THE GB AND THEN TO ENABLE DATA ON THE GB TO A GENERAL REGISTER.

TABLE A

TO AND FROM FIELD DECODER ASSIGNMENTS

GENERAL REGISTER	GB X GENERAL REGISTER (TO FIELD PAIR)		GENERAL REGISTER X GB (FROM FIELD PAIR)	
	NET NAME	(PIN NO.)	NET NAME	(PIN NO.)
R0	T204L50A (303)	T204R30A (213)	F204L50B (203)	F204R30A (310)
R1	T204L50A (308)	T204R50A (013)	F204L50A (005)	F204R50A (110)
R2	T204L50A (303)	T204R60A (312)	F204L50A (005)	F204R60A (206)
R3	T204L50A (303)	T204R90A (112)	F204L50A (005)	F204R90A (006)
R4	T204L50A (303)	T204RA0A (311)	F204L50A (005)	F204RA0A (305)
R5	T204L50A (303)	T204RC0A (111)	F204L50A (005)	F204RC0A (105)
R6	T204L60A (102)	T204R30A (213)	F204L60A (205)	F204R30A (310)
R7	T204L60A (102)	T204R50A (013)	F204L60A (205)	F204R50A (110)
R8	T204L60A (102)	T204R60A (312)	F204L60A (205)	F204R60A (206)
R9	T204L60A (102)	T204R90A (112)	F204L60A (205)	F204R90A (006)
R10	T204L60A (102)	T204RA0A (311)	F204L60A (205)	F204RA0A (305)
R11	T204L60A (102)	T204RC0A (111)	F204L60A (205)	F204RC0A (105)
R12	T104L40 (211)	T204R70A (202)	F104L40A (302)	F304R70A (201)
R13	T104L40 (211)	T304RB0A (002)	F104L40A (302)	F304RB0A (001)
R14	T104L40 (211)	T304RD0A (301)	F104L40A (302)	F304RD0A (300)
R15	T104L40 (211)	T304RE0A (101)	F104L40A (302)	F304RE0A (100)

PART OF FS 3
COMPOSITE DIAGRAM 1

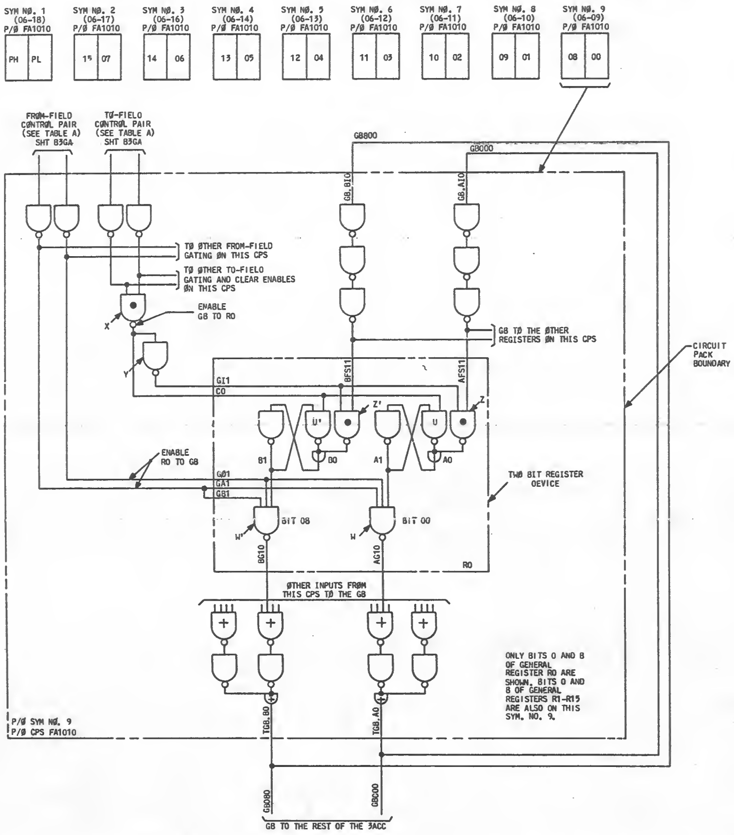
3A CENTRAL CONTROL ②
DWG SIZE 6S
ISSUE 3A
BELL LABORATORIES
SD-1C900-01
B3GA

PART OF FS 3

GENERAL REGISTERS (R0-R15)

COMPOSITE DIAGRAM 2

BIT SLICED PARTITIONING OF GENERAL REGISTERS
AND IMPLEMENTATION OF THE BASIC REGISTER CELL
SYM NO. 9 (06-09)


SYM NO. 1 (06-18) P/O FA1010
PH
PL
SYM NO. 2 (06-17) P/O FA1010
15
07
SYM NO. 3 (06-16) P/O FA1010
14
06
SYM NO. 4 (06-14) P/O FA1010
13
05
SYM NO. 5 (06-13) P/O FA1010
12
04
SYM NO. 6 (06-12) P/O FA1010
11
03
SYM NO. 7 (06-11) P/O FA1010
10
02
SYM NO. 8 (06-10) P/O FA1010
09
01
SYM NO. 9 (06-09) P/O FA1010
08
00
FROM-FIELD CONTROL PAIR (SEE TABLE A) SHT B3GA
TO-FIELD CONTROL PAIR (SEE TABLE A) SHT B3GA
GB800
GB000
GB.BI0
GB.AI0
TO OTHER FROM-FIELD GATING ON THIS CPS
TO OTHER TO-FIELD GATING AND CLEAR ENABLES ON THIS CPS
ENABLE GB TO R0
X
Y
GB TO THE OTHER REGISTERS ON THIS CPS
CIRCUIT PACK BOUNDARY
BFS11
AFS11
GI1
C0
Z'
Z
U'
U
B1
B0
A1
A0
ENABLE R0 TO GB
G01
GA1
GB1
TWO BIT REGISTER DEVICE
BIT 08
BIT 00
W'
W
BG10
AG10
R0
OTHER INPUTS FROM THIS CPS TO THE GB
+
TGB.B0
TGB.A0
P/O SYM NO. 9
P/O CPS FA1010
GB080
GB000
GB TO THE REST OF THE 3ACC

ONLY BITS 0 AND 8 OF GENERAL REGISTER R0 ARE SHOWN. BITS 0 AND 8 OF GENERAL REGISTERS R1-R15 ARE ALSO ON THIS SYM. NO. 9.

CIRCUIT OPERATION

COMPOSITE DIAGRAM NO. 2 SHOWS A DETAILED DESCRIPTION OF THE GATING OPERATION FOR THE GENERAL REGISTER CELLS, AND THE CONTROL NECESSARY TO PERFORM THAT GATING. AS INDICATED IN TABLE A (SHEET B3GA), IT TAKES A PAIR OF TO-FIELD AND A PAIR OF FROM-FIELD CONTROL SIGNALS TO PERFORM THE REGISTER TO REGISTER GATING FUNCTION. FOR EXAMPLE, IF DATA IS TO BE GATED INTO GENERAL REGISTER R0 VIA THE GB, THEN THE TO-FIELD CONTROL PAIR THAT MUST BE ENABLED IS T204L50A AND T204R30A. THEY MUST BE LOW IN THE BACKPLANE (i.e. AT THE INPUT TO THE CIRCUIT PACK) IN ORDER TO BE ACTIVE. IF THE TO-FIELD CONTROL PAIR IS ACTIVE, GATE X WILL BE ACTIVE, THAT IS, ITS OUTPUT WILL BE LOW. GATE X LOW WILL CLEAR BIT 0 OF GENERAL REGISTER R0 BY PUTTING A LOW AT THE INPUT TO GATE U. NOTE THAT WHATEVER IS TRUE FOR U, IS ALSO TRUE FOR U', WHICH IN THIS CASE, IS BIT 8 OF GENERAL REGISTER R0. SINCE BOTH BIT 0 AND BIT 8 ARE ON THE SAME CIRCUIT PACK, THEY SHARE COMMON CONTROL SIGNALS. WITH THE OUTPUT OF GATE Y ACTIVE (i.e. HIGH), GATE Z WILL BE ENABLED TO ALLOW DATA, ORIGINATING FROM THE GB, TO FLOW INTO THE REGISTER CELL. IF A "ONE" IS CONTAINED ON THE GB. NET GB000 WILL BE LOW ACTIVE AND, AS A RESULT, GATE Z WILL BE ACTIVE (OUTPUT LOW). THIS WILL FORCE NODE A0 LOW, (WITH A0 LOW, A1 WILL BE HIGH WHICH IS DEFINED AS A "ONE" IN THE REGISTER CELL), DESPITE THE FACT THAT THE CLEAR SIGNAL AT THE INPUT OF GATE U FROM GATE X IS ATTEMPTING TO KEEP A0 HIGH. NOTE THAT AS LONG AS THE SIGNAL AT THE OUTPUT OF GATE X IS REMOVED BEFORE THE SIGNAL AT THE OUTPUT OF GATE Y, A "ONE" IS MAINTAINED IN THE REGISTER CELL. THIS IS GUARANTEED BY THE LOGIC DELAY THROUGH GATE Y. THE DESCRIBED OPERATION IS CALLED THE "CLEAR AND GATE" GATING FUNCTION. THIS GATING FUNCTION IS USED THROUGHOUT THE 3A CC.

DATA IS PLACED ONTO THE GB BY ENABLING A PAIR OF FROM-FIELD CONTROL SIGNALS. SPECIFICALLY, TO ALLOW THE OUTPUT OF GENERAL REGISTER R0 ONTO THE GB, IT IS NECESSARY FOR THE CONTROL SIGNALS F204L50B AND F204R30A TO BE ACTIVE SIMULTANEOUSLY. WHEN THESE CONTROL SIGNALS ARE ACTIVE, THE CONTENTS OF GENERAL REGISTER R0 WILL BE OUTPUTED ONTO THE GB THROUGH GATE W. NOTE THAT GATE W GOES THROUGH TWO MORE GATES BEFORE IT ACTUALLY REACHES THE GB. THESE TWO GATE DELAYS ALLOW SUFFICIENT "FAN-IN" SO THAT MOST OF THE REGISTERS WITHIN THE 3A CC CAN BE "OR"ED ONTO THE GB. SIMILARLY THE THREE GATES OF INVERSION ON THE INPUT FROM THE GB ALLOW THE GB TO "FANOUT" TO MOST OF THE REGISTERS IN THE 3A CC.

IT SHOULD BE NOTED THAT BECAUSE OF THE METHOD OF GATING FROM A REGISTER ONTO THE GB AND THEN OFF OF THE GB TO A REGISTER, IT IS NOT MEANINGFUL TO GATE A REGISTER TO ITSELF. THAT IS, IT WILL CAUSE THE REGISTER TO GO TO SOME INDETERMINED STATE BECAUSE OF THE RACE CONDITION THAT WILL BE SET UP BY THAT OPERATION. NOTE ALSO THAT THE METHOD OF BIT SLICING THE INDIVIDUAL BITS OF THE GENERAL REGISTERS IS THE SAME METHOD USED FOR MOST OF THE OTHER REGISTERS IN THE 3A CC. OF THOSE REGISTERS THAT ARE NOT BIT SLICED, MOST ARE DUPLICATE. THE METHOD DESCRIBED FOR REGISTER-TO-REGISTER GATING IS THE PRIMARY METHOD USED THROUGHOUT THE 3A CC FOR GATING DATA BETWEEN REGISTERS WHETHER THEY ARE BIT SLICED OR NOT.

THE 2-BIT REGISTER DEVICE THAT IS INDICATED IN COMPOSITE DIAGRAM NO. 2 IS A BASIC LOGIC BLOCK PROVIDED IN A 1A LOGIC FAMILY. COMPOSITE DIAGRAM NO. 2 SHOWS THE METHOD IN WHICH THE INTERCONNECTING OF TWO CELLS IN THE 2-BIT REGISTER DEVICE ARE TYPICALLY USED. THE INTERCONNECTIONS SHOWN "WITHIN" THE 2-BIT REGISTERS DEVICE ARE FIXED, AND HENCE CANNOT CHANGE FROM ONE FUNCTION APPLICATION TO ANOTHER. THE CONNECTIONS SHOWN BETWEEN THE CIRCUIT PACK BOUNDARY AND THE BOUNDARY OF THE 2-BIT REGISTER DEVICE ARE UNIQUE TO A GIVEN CIRCUIT PACK CODE, BUT THESE CONNECTIONS MAY CHANGE FROM ONE CIRCUIT PACK TO ANOTHER (i.e. FROM ONE CODE TO ANOTHER). NOTE THAT AS FAR AS THE GENERAL REGISTERS ARE CONCERNED, THE ONLY ACCESS THAT IS AVAILABLE TO THE GENERAL REGISTERS IS THE ACCESS SHOWN AT THE CIRCUIT PACK BOUNDARIES OF COMPOSITE DIAGRAM NO. 2 AND COMPOSITE DIAGRAM NO. 3.

PART OF FS 3
COMPOSITE DIAGRAM 2

3A CENTRAL CONTROL

DWG SIZE
65

ISSUE
5A

BELL LABORATORIES
SD-1C900-01
B3GB

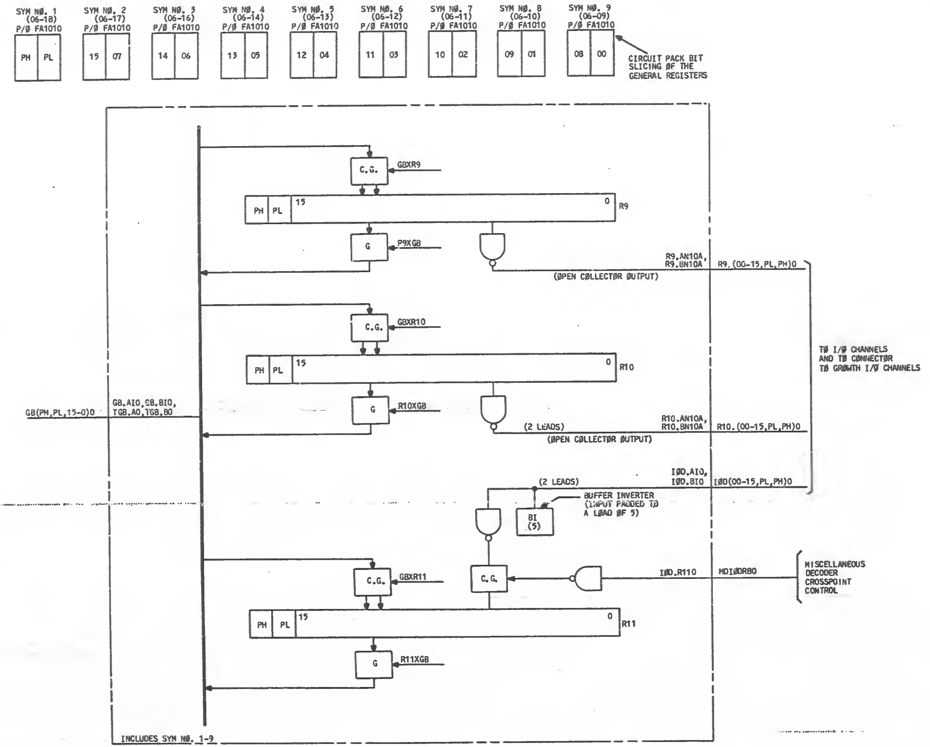
PRINTED IN U.S.A.

PART OF FS 3

GENERAL REGISTERS (R0-R15)

COMPOSITE DIAGRAM 3

GENERAL REGISTERS R9,R10 AND R11 INTERFACE
TO I/O CHANNELS
(SYMBOLS 1-9)



CIRCUIT OPERATION

THERE ARE THREE GENERAL REGISTERS THAT ARE USED FOR COMMUNICATING TO THE I/O CHANNELS, R9,R10, AND R11. FOR THIS FUNCTION, SPECIAL ACCESS IS PROVIDED INTO AND OUT OF THESE REGISTERS. THIS ACCESS IS INDICATED IN COMPOSITE DIAGRAM NO. 3. R9 TYPICALLY CONTAINS THE CONTROL INFORMATION THAT SELECTS WHICH I/O MAIN CHANNEL IS ACTIVE, WHICH I/O SUBCHANNEL IS ACTIVE, AND WHAT TYPE OF STATE THE I/O MAIN CHANNEL IS TO BE PLACED IN. THEREFORE, THE INDIVIDUAL OUTPUTS OF THE R9 BITS APPEAR ON THE BACKPLANE. R10 TYPICALLY CONTAINS THE DATA. THAT IS TO BE SENT TO A PERIPHERAL UNIT. THEREFORE THE INDIVIDUAL OUTPUTS OF R10 APPEAR ON THE BACKPLANE ALSO. R11 TYPICALLY CONTAINS DATA RETURNED FROM A PERIPHERAL UNIT. THEREFORE INPUTS ARE PROVIDED TO THE INDIVIDUAL BITS OF R11 TOGETHER WITH A MISCELLANEOUS DECODER CONTROL SIGNAL THAT ALLOWS THE GATING OF THE I/O DATA BUS INTO R11. IN ORDER TO TERMINATE THE INPUT LEADS OF THE DATA BUS BEING RETURNED FROM THE I/O CHANNELS, BUFFER INVERTER PADDING IS ATTACHED TO THE INPUTS OF R11. THIS PROVIDES ESSENTIALLY A RESISTIVE TERMINATION THAT MINIMIZES THE CAPACITANCE EFFECTS OF THE LONGER LEAD LENGTHS ASSOCIATED WITH CONNECTING THE I/O CHANNELS WITH THE INPUT TO R11. NOTE THAT THE MISCLLLANEOUS DECODER CROSSPOINT USED TO LOAD R11 IS NOT ONE OF THE EIGHT MISCELLANEOUS DECODER CROSSPOINTS THAT ARE SENT TO THE I/O CHANNELS, BUT IS INSTEAD A SEPARATE ONE THAT IS CONTAINED COMPLETELY WITH THE 3ACC. AS SUCH, THAT LATTER DOES NOT HAVE THE SPECIAL TIMING PROVIDED FOR THE I/O MISCELLANEOUS DECODER CROSSPOINTS SENT TO THE I/O CHANNELS. (SEE SHEET B1HA).

PART OF FS 3
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-0:	B3GC

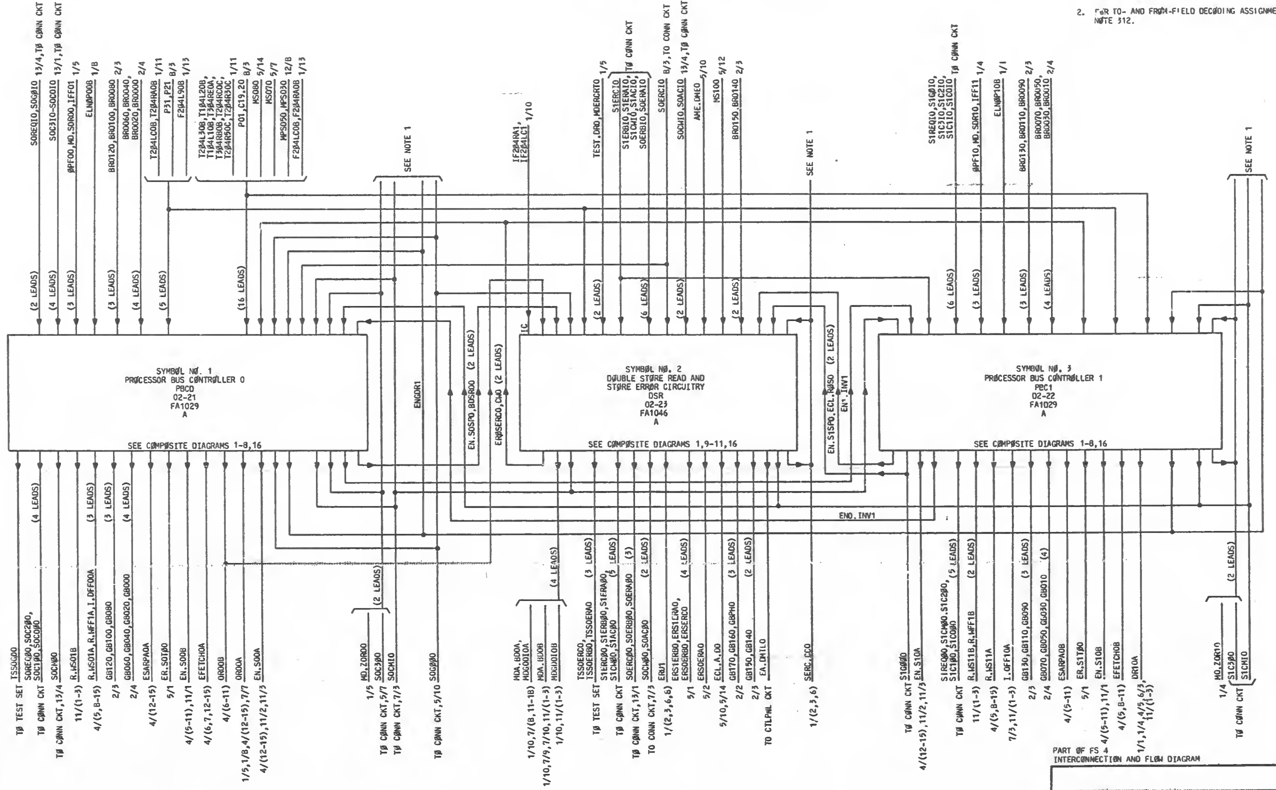
PART OF FS 4

PROCESSOR BUS CONTROLLER
INTERCONNECTION AND FLOW DIAGRAM

CW16B0

NØTES:

1. LEADS SHØWN CØULD FUNCTIØN AS EITHER ØUTPUTS ØR INPUTS (ØI). ALL ØFF-PAGE REFERENCING WILL BE SHØWN ØN ØUTPUT LEAD.
2. FØR TO- AND FRØM-FIELD DECØDING ASSIGNMENTS SEE NØTE 312.



PART ØF FS 4
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL	DWG SIZE 6S	ISSUE 8A
BELL LABORATORIES	SD-1C900-01	B4AA

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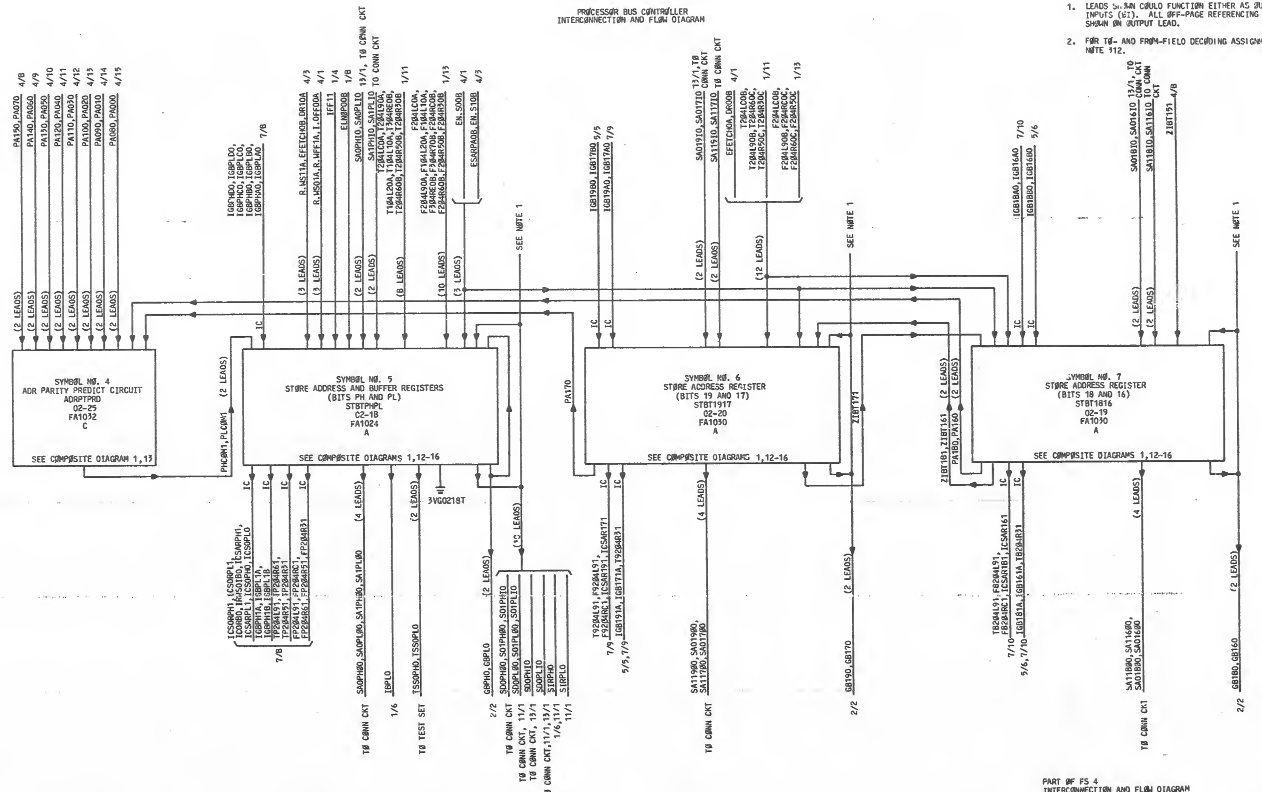
E - 7621 (12 - 73)

PART OF FS 4

PRØCESSØR BUS CØNTRØLLER
INTERCØNNECTIØN AND FLØW OIAGRAM

NØTES:

1. LEADS SHØWN CØULO FUNCTIØN EITHER AS ØUTPUTS ØR INPUTS (EI). ALL ØFF-PAGE REFERENCING WILL BE SHØWN ØN ØUTPUT LEAD.
2. FØR TØ- AND FRØM-FIELO DECØDING ASSIGNMENTS SEE NØTE 312.


PA150,PA070 4/8
PA140,PA060 4/9
PA130,PA050 4/10
PA120,PA040 4/11
PA110,PA030 4/12
PA100,PA020 4/13
PA090,PA010 4/14
PA080,PA000 4/15
(2 LEAOS)
IGBPHDO,IGBPLDO, IGBPHCO,IGBPLCO, IGBPHBO,IGBPLBO, IGBPHAO,IGBPLAO 7/8
IC
R.WS11A,EFETCHOB,DR10A 4/3
R.WS01A,R.WFF1A,I.OFFOOA 4/1
IFF11 1/4
ELNØPOOB 1/8
SAOPHIO,SAOPLIO 13/1, TØ CØNN CKT
SA1PHIO,SA1PLIO TO CONN CKT
T2Ø4LCOA,T2Ø4L90A, T1Ø4L20A,T1Ø4L10A,T3Ø4REOB, T2Ø4R60B,T2Ø4R50B,T2Ø4R30B 1/11
F2Ø4LCOA, F2Ø4L90A,F1Ø4L20A,F1Ø4L10A, F3Ø4REOB,F3Ø4R70B,F2Ø4RCOB, F2Ø4R60B,F2Ø4R50B,F2Ø4R30B 1/13
EN.SOOB 4/1
ESARPAOB,EN.S10B 4/3
(3 LEADS)
(2 LEADS)
(8 LEAOS)
(10 LEAOS)
(3 LEAOS)
SEE NØTE 1
IGB19BO,IGB17BO 5/5
IGB19AO,IGB17AO 7/9
SA01910,SA01710 13/1,TØ CØNN CKT
SA11910,SA11710 TØ CØNN CKT
EFETCHOA,DROOB 4/1
T2Ø4LCOB, T2Ø4L90B,T2Ø4R60C, T2Ø4R50C,T2Ø4R30C 1/11
F2Ø4LCOB, F2Ø4L90B,F2Ø4RCOC, F2Ø4R60C,F2Ø4R50C 1/13
(12 LEAOS)
IGB18AO,IGB16AO 7/10
IGB18BO,IGB16BO 5/6
SA018IO,SA016IO 13/1, TO CONN CKT
SA118IO,SA116IO TO CONN CKT
ZIBT151 4/8
SYMBØL NØ. 4
ADR PARITY PREDICT CIRCUIT
ADRPTPRD
02-25
FA1032
C
SEE CØMPØSITE OIAGRAM 1,13
PHCØM1,PLCØM1
(2 LEAOS)
SYMBØL NØ. 5
STØRE ADDRESS AND BUFFER REGISTERS
(BITS PH AND PL)
STBTPHPL
C2-1B
FA1024
A
SEE CØMPØSITE OIAGRAMS 1,12-16
PA170
SYMBØL NØ. 6
STØRE ACDRESS REGISTER
(BITS 19 ANO 17)
STBT1917
02-20
FA1030
A
SEE CØMPØSITE OIAGRAMS 1,12-16
ZIBT171
ZIBT1B1,ZIBT161
PA1B0,PA160
(2 LEADS)
SYMBØL NØ. 7
STØRE ADDRESS REGISTER
(BITS 18 AND 16)
STBT1816
02-19
FA1030
A
SEE CØMPØSITE DIAGRAMS 1,12-16
3VG0218T
ICSORPH1,ICSORPL1, ICORBO,IRWSOIBO,ICSARPH1, ICSARPL1,ICSOPHO,ICSOPLO
IGBPH1A,IGBPL1A, IGBPH1B,IGBPL1B
TP2Ø4L91,TP2Ø4R61, TP2Ø4R51,TP2Ø4R31
FP2Ø4L91,FP2Ø4RC1, FP2Ø4R61,FP2Ø4R51,FP2Ø4R31
7/B
(4 LEADS)
SAOPHØO,SAOPLØO,SA1PHØO,SA1PLØO TØ CØNN CKT
IBPLO 1/6
(2 LEAOS)
TSSOPHO,TSSOPLO TØ TEST SET
(12 LEAOS)
GBPHO,GBPLO 2/2
SDOPHØO,SO1PHØO,SO1PHIO TØ CØNN CKT
SDOPLØO,SO1PLØO,SO1PLIO TØ CØNN CKT, 11/1
SDOPHIO TØ CØNN CKT, 13/1
SDOPLIO TØ CØNN CKT,11/1,13/1
SIRPHO 1/6,11/1
SIRPLO 11/1
T92Ø4L91,F92Ø4L91, F92Ø4RC1,ICSAR191,ICSAR171 7/9
IGB191A,IGB171A,T92Ø4R31 5/5,7/9
SA119ØO,SA019ØO, SA117ØO,SA017ØO TØ CØNN CKT
GB190,GB170 2/2
TB2Ø4L91,FB2Ø4L91, FB2Ø4RC1,ICSAR1B1,ICSAR161 7/10
IGB181A,IGB161A,TB2Ø4R31 5/6,7/10
SA11BØO,SA116ØO, SA01BØO,SA016ØO TØ CØNN CKT
GB1BO,GB160 2/2

PART ØF FS 4
INTERCØNNECTIØN AND FLØW OIAGRAM

3A CENTRAL CØNTRØL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4AB

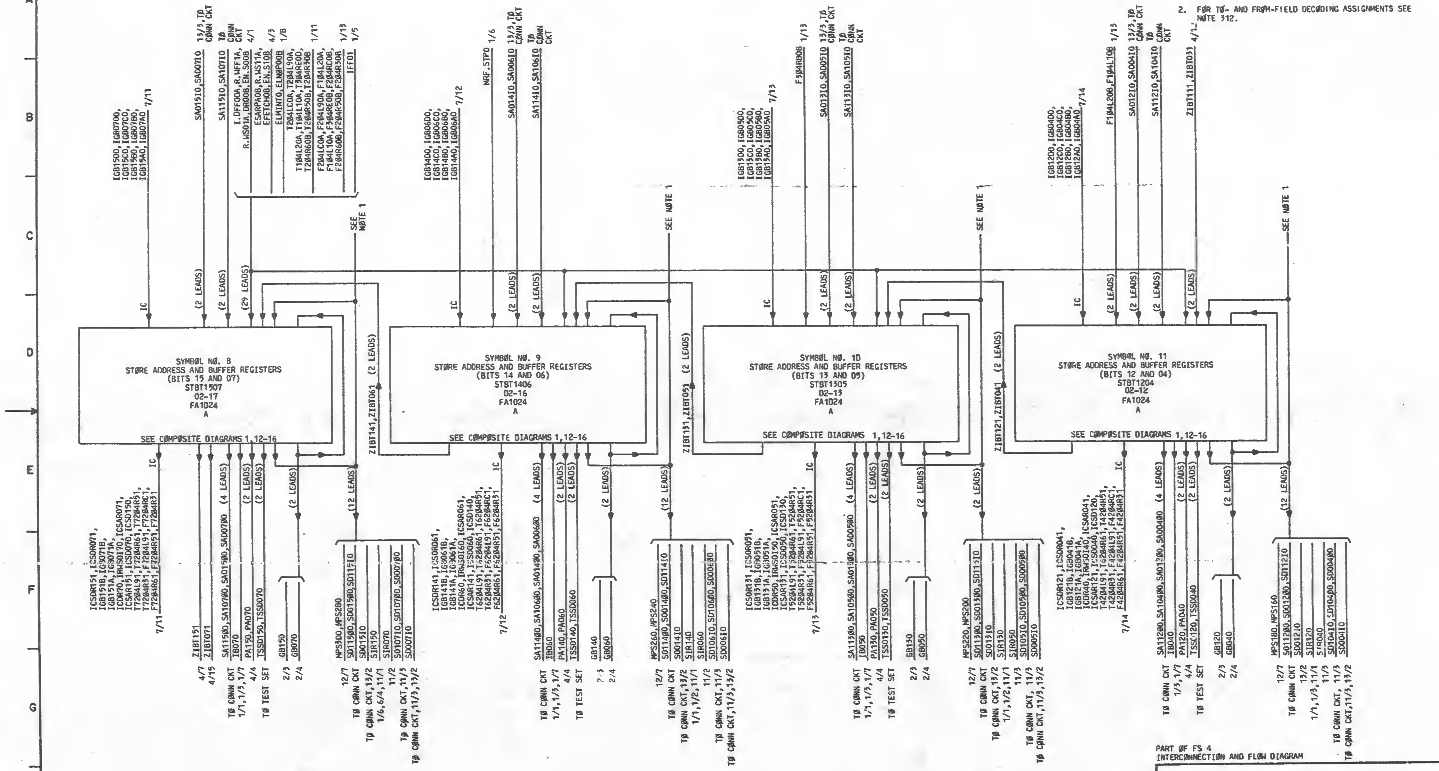
PART OF FS 4

PROCESSOR BUS CONTROLLER
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (OI). ALL OFF-PAGE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.

2. FOR TO- AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 4
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

②

DWG SIZE	ISSUE
6S	5A

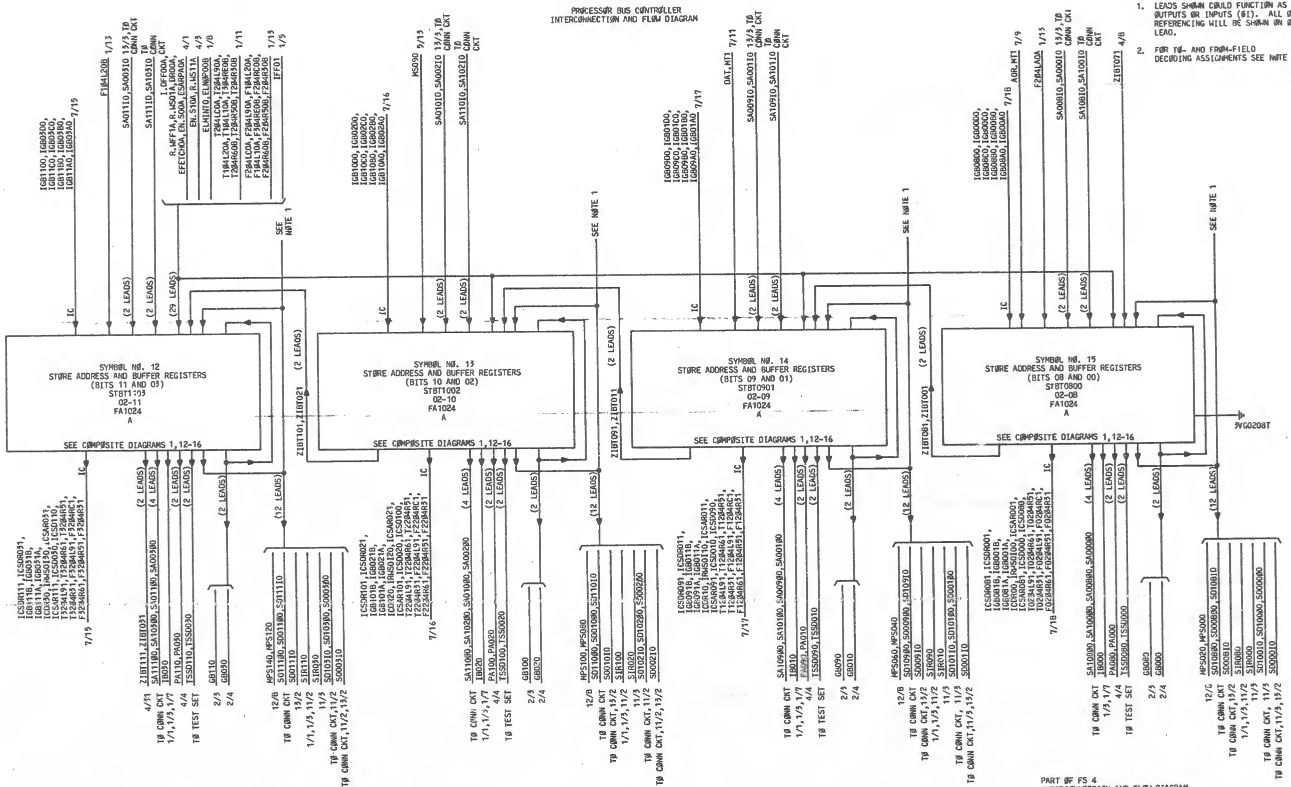
BELL LABORATORIES | SD-1C900-01 | B4AC

PART OF FS 4

PRØCESSØR BUS CØNTRØLLER
INTERCØNNECTIØN AND FLØW DIAGRAM

NØTES:

1. LEADS SHØWN CØULD FUNCTIØN AS EITHER ØUTPUTS ØR INPUTS (ØI). ALL ØFF-PAGE REFERENCING WILL BE SHØWN ØN ØUTPUT LEAD.
2. FØR TØ- AND FRØM-FIELD DECØDING ASSIGNMENTS SEE NØTE 312.



PART ØF FS 4
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL

②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES

SD-1C900-01

B4AD

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ADR.MT1	ADDRESSED MATCH OF MAIN MEMORY (UNSTROBED)
AME.OME0	INDICATION THAT THE ADDRESS AND/OR DATA MATCH BITS (AME OR OME) IN THE SS REGISTER ARE ACTIVE
BOSR00	BLOCK DOUBLE STORE READ (COPY 0)
BDSR10	BLOCK DOUBLE STORE READ (COPY 1)
BR0000-BR0150	BITS 0-15 OF THE BR REGISTER (COPY 0)
CW0	COMPLEMENT WRITE BIT IN MMS REGISTER
C19.20	CLOCK PULSE OF 19.20 USEC
OAT.MT1	DATA MATCH ON MAIN MEMORY (UNSTROBED)
OR00A	DATA READY FLIP-FLOP (COPY 0)
OR00B	DATA READY FLIP-FLOP (COPY 0)
OR10A	DATA READY FLIP-FLOP (COPY 1)
OR10B	DATA READY FLIP-FLOP (COPY 1)
EA.OMTL0	PANEL ENABLE ADDRESS AND/OR DATA MATCHER LAMP INDICATOR
ECL.A.00	ENABLE CLEARING OF THE ADDRESS MATCH ENABLE BIT AND THE DATA MATCH ENABLE BIT IN THE SS REGISTER. (ENABLING IS PERFORMED WHEN A PARITY ERROR IS DETECTED IN THE ON-LINE STORE AND A COMPLEMENT CORRECTION IS TO BE PERFORMED.)
ECL.ROS0	ENABLE CLEARING OF THE READ OTHER STORE RETRY MODE
EFETCH0A	CONDITIONAL ENABLE MAIN MEMORY FETCH (CONDITIONED ON IFF=0)
EFETCH0B	CONDITIONAL ENABLE MAIN MEMORY FETCH (CONDITIONED ON IFF=0)
ELMINT0	ENABLE LOAD MICROINTERPRET INSTRUCTIONS
ELNOP00B	ENABLE LOAD NEW OPCODE (COPY 0)
ELNOP10B	ENABLE LOAD NEW OPCODE (COPY 1)
EN.S0SP0	ENABLE MY STORE (CONTROLLED BY SEZ FLIP-FLOP)
EN.S00(A,B)	ENABLE MY STORE
EN.S1SP0	ENABLE OTHER STORE (CONTROLLED BY SEZ FLIP-FLOP)
EN.S10(A,B)	ENABLE OTHER STORE
ENGDR1	ENABLE GATING TO THE OR FLIP-FLOPS (COPY 0 AND COPY 1)
EN(0,1).INV1	ENABLE THE INVERSION OF THE IOLE FLIP-FLOP DURING A DOUBLE STORE READ
ER.S0T00	MY STORE FAST TIMEOUT ERROR
ER.S1T00	OTHER STORE FAST TIMEOUT ERROR
EROSERC0	STORE ERROR C SIGNAL FROM THE DOUBLE STORE READ PACK. (INDICATE THAT A PARITY ERROR HAS OCCURED ON THE PRESENT MEMORY CYCLE, EITHER IN A READ COMMAND TO THE ON-LINE STORE OR THE OFF-LINE STORE)
ERSERC0	MY STORE ERROR C OR OTHER STORE ERROR C (READ PARITY ERROR)
ERS0ERA0	MY STORE ERROR A (ALL MAIN STORE ERRORS EXCEPT WRITE PROTECT)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ERS0ERB0	MY STORE ERROR B (WRITE PROTECT ERROR)
ERS1ERA0	OTHER STORE ERROR A (ALL MAIN STORE ERRORS EXCEPT, WRITE PROTECT)
ERS1ERB0	OTHER STORE ERROR B (WRITE PROTECT ERROR)
ERU1	ERROR RETURN ADDRESS REGISTER UPDATE BIT
ESARPA0(A,B)	ENABLE GATING FROM THE SAR TO THE PA
GBPH0	PARITY HIGH OF THE GATING BUS
GBPL0	PARITY LOW OF THE GATING BUS
GB000-GB190	BITS 0-19 OF THE GATING BUS
I.OFF00A	OUTPUT OF THE INSTRUCTION OR DATA FLIP-FLOP (COPY 0)
I.OFF10A	OUTPUT OF THE INSTRUCTION OR DATA FLIP-FLOP (COPY 1)
IBPH0	PARITY BIT OF THE INSTRUCTION BUFFER
IBPL0	PARITY LOW OF THE IB REGISTER
IB000-IB070	BITS 0-7 OF THE IB REGISTER
IB150	BIT 15 OF THE IB REGISTER
ICDR00-ICOR80	OUTPUT OF OR FLIP-FLOP [IC]
ICSARPH1	PARITY HIGH, SAR REGISTER [IC]
ICSARPL1	PARITY LOW, SAR REGISTER [IC]
ICSAR001-ICSAR191	BITS 0-19 OF THE SAR REGISTER [IC]
ICSOPH0	PARITY HIGH OF THE MAIN STORE DATA BUS [IC]
ICSOPL0	PARITY LOW OF THE MAIN STORE DATA BUS [IC]
ICSORPH1	PARITY HIGH OF THE SDRO [IC]
ICSDRPL1	PARITY LOW OF THE SORO [IC]
ICSOR001-ICSOR151	BITS 0-15 OF THE SDRO [IC]
ICS0000-ICS0150	BITS 0-15 OF THE MAIN STORE DATA BUS [IC]
IFF01	I FLIP-FLOP (COPY 0)
IFF11	I FLIP-FLOP (COPY 1)
IGBPH(A-0)0	INPUTS TO PARITY HIGH OF THE GATING BUS [IC]
IGBPH1(A,B)	OUTPUTS OF PARITY HIGH OF THE GATING BUS [IC]
IGBPLA0-IGBPL00	OUTPUTS OF GATING BUS BIT P2 [IC]
IGBPL1(A,B)	OUTPUTS FROM PARITY LOW OF THE GATING BUS [IC]
IGB00A0-IGB19A0	INPUTS TO GATING BUS BITS 0-19 [IC]
IGB00B0-IGB19B0	INPUTS TO GATING BUS BITS 0-19 [IC]
IGB00C0-IGB15C0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB00D0-IGB15D0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB001A-IGB191A	OUTPUTS OF GATING BUS BITS 0-19 [IC]
IGB001B-IGB151B	OUTPUTS OF GATING BUS BITS 0-15 [IC]
IRWS0I00-IRWS0I80	READ-WRITE CONTROL FOR MY STORE BUS, BITS 0-8 [IC]

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MD.SOR00	MISC. DECODER, SET DATA READY FLIP-FLOP (COPY 0)
MD.SDR10	MISC. DECODER, SET DATA READY FLIP-FLOP (COPY 1)
MD.ZOR00	MISC. DECODER, ZERO DATA READY FLIP-FLOP (COPY 0)
MD.ZDR10	MISC. DECODER, ZERO DATA READY FLIP-FLOP (COPY 1)
MOA.BD0(A,B)	ENABLE GATING OF THE BAD DATA AND THE ADDRESS OF A DOUBLE STORE READ OPERATION TO THE DK AND AK REGISTERS RESPECTIVELY
MOERCRT0	MISCELLANEOUS DECODER RETURN FROM COMPLEMENT CORRECTION MICROSUBROUTINE
MOGDDI0(A,B)	ENABLE GATING OF THE GOOD DATA OF THE DOUBLE STORE READ OPERATION TO THE OI REGISTER
MPS000	BIT 0 OF THE MICRO-PROGRAM STORE OUTPUT
MPS020-MPS060	BITS 2-6 OF THE MICRO-PROGRAM STORE OUTPUT
MPS(08,10,12,14,16,18,20,22,24,26,28,30)0	BITS (08,10,12,14,16,18,20,22,24,26,28,30) OF THE MICRO-PROGRAM STORE OUTPUT
MRF.STP0	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF), 'OR' OF THE MRF SIGNAL AND THE STOP FLIP-FLOP
MS070	BIT 7 MAINTENANCE STATE REGISTER (ACTIVATE MY STORE)
MS080	BIT 8 MAINTENANCE STATE REGISTER (ACTIVATE OTHER STORE)
MS090	BIT 9 MAINTENANCE STATE REGISTER (ENABLE IB 3 OF 6 TRANSLATORS AND DISABLE FROM FIELD OF CHECK)
MS100	BIT 10 MAINTENANCE STATE REGISTER (ENABLE MAR-RAR MATCH)
OPF00	OPCODE FIL BIT (COPY 0)
OPF10	OPCODE FIL BIT (COPY 1)
PAPH0	PARITY HIGH OF PROGRAM ADDRESS REGISTER
PAPL0	PARITY LOW OF PROGRAM ADDRESS REGISTER
PA000-PA180	BITS 0-18 OF PROGRAM ADDRESS REGISTER
PHCOM1	COMPLEMENT PARITY HIGH OF THE PA (PARITY PREDICT LOGIC) ATTACHED TO PA OUTPUTS
PLCOM1	COMPLIMENT PARITY LOW OF THE PA (PARITY PREDICT LOGIC ATTACHED TO PA(7-0) OUTPUTS)
P01	CLOCK PHASE P1 (POSITIVE ACTIVE)
P21	CLOCK PHASE P2 (POSITIVE ACTIVE)
P31	CLOCK PHASE P3 (POSITIVE ACTIVE)
R.WFF1A	READ/WRITE FLIP-FLOP (COPY 0)
R.WFF1B	READ/WRITE FLIP-FLOP (COPY 1)
R.WS01(A,B)	READ OR WRITE FUNCTION FOR MAIN STORE 0 (DEFINED BY SC300)
R.WS11(A,B)	READ OR WRITE FUNCTION OF MAIN STORE 1 (DEFINED BY SC310)
SA0PHI0	MY MAIN STORE ADDRESS BUS INPUT PARITY HIGH (FUSED)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SA0PH00	MY MAIN STORE ADDRESS BUS OUTPUT PARITY HIGH
SA0PLI0	MY MAIN STORE ADDRESS BUS INPUT PARITY LOW (FUSED)
SA0PL00	MY MAIN STORE ADDRESS BUS OUTPUT PARITY LOW
SA000I0-SA019I0	MY MAIN STORE ADDRESS BUS INPUTS BITS 0-19 (FUSED)
SA00000-SA01900	MY MAIN STORE ADDRESS BUS OUTPUTS BITS 0-19
SA1PHI0	OTHER MAIN STORE ADDRESS BUS INPUT PARITY HIGH
SA1PH00	OTHER MAIN STORE ADDRESS BUS OUTPUT PARITY HIGH
SA1PLI0	OTHER MAIN STORE ADDRESS BUS INPUT PARITY LOW
SA1PL00	OTHER MAIN STORE ADDRESS BUS OUTPUT PARITY LOW
SA100I0-SA119I0	OTHER MAIN STORE ADDRESS BUS INPUTS BITS 0-19
SA10000-SA11900	OTHER MAIN STORE ADDRESS BUS OUTPUT BITS 0-19
SORPH1	PARITY HIGH OF THE SDRO
SORPL1	PARITY LOW OF THE SORO
SOR001-SDR151	BITS 0-15 OF THE SORO
S00PHI0	MY MAIN STORE DATA BUS PARITY HIGH INPUT (FUSED)
S00PH00	MY MAIN STORE DATA BUS PARITY HIGH OUTPUT
SD0PLI0	MY MAIN STORE DATA BUS PARITY LOW INPUT (FUSED)
S00PL00	MY MAIN STORE DATA BUS PARITY LOW OUTPUT
S000I0-S0015I0	MY MAIN STORE DATA BUS INPUT LEADS 0-15 (FUSED)
SD00000-S001500	MY MAIN STORE DATA BUS OUTPUT LEADS 0-15
SD1PHI0	OTHER MAIN STORE DATA BUS INPUT LEAD PH
S01PH00	OTHER MAIN STORE DATA BUS OUTPUT LEAD PH
SD1PLI0	OTHER MAIN STORE DATA BUS INPUT LEAD PL
SD1PL00	OTHER MAIN STORE DATA BUS OUTPUT LEAD PL
SD100I0-S0115I0	OTHER MAIN STORE DATA BUS INPUT LEADS 0-15
SD10000-SD11500	OTHER MAIN STORE DATA BUS OUTPUT LEADS 0-15
SERC.CC0	STORE ERROR C RECALLING IN THE INVOCATION OF THE COMPLEMENT CORRECTION MICROSUBROUTINE
SIRPH0	PARITY HIGH OF SIR'S (SIR0 IF IFF=0, SIR1 IF IFF=1)

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4AE

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02/21/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SIRPL0	PARITY LOW OF SIR'S (SIR0 IF IFF=0, SIR1 IF IFF=1)
SIR000-SIR150	BITS 0-15 OF THE SIR'S (SIR0 IF IFF=0, SIR1 IF IFF=1)
S0ACI0	MY MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL INPUT (FUSED)
S0AC00	MY MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL OUTPUT
S0CMI0	MY MAIN STORE BUS STORE COMPLETE SIGNAL INPUT
S0CM00	MY MAIN STORE BUS STORE COMPLETE SIGNAL OUTPUT (FUSED)
S0CWI0	MY MAIN STORE BUS COMPLEMENT WRITE SIGNAL INPUT (FUSED)
S0CW00	MY MAIN STORE BUS COMPLEMENT WRITE SIGNAL OUTPUT
S0C0I0-S0C3I0	MY MAIN STORE BUS CONTROL LEAD INPUTS (FUSED)
S0C000-S0C300	MY MAIN STORE BUS CONTROL LEAD OUTPUTS
S0ERAI0	MY MAIN STORE BUS ERROR SIGNAL A INPUT (FUSED)
S0ERA00	MY MAIN STORE ERROR SIGNAL A OUTPUT (FUSED)
S0ERBI0	MY MAIN STORE ERROR SIGNAL B INPUT
S0ERB00	MY MAIN STORE BUS ERROR SIGNAL B OUTPUT (FUSED)
S0ERCI0	MY MAIN STORE BUS ERROR SIGNAL C INPUT
S0ERC00	MY MAIN STORE BUS ERROR SIGNAL C OUTPUT (FUSED)
S0G0I0	MY MAIN STORE BUS STORE GO SIGNAL INPUT (FUSED)
S0G000	MY MAIN STORE BUS STORE GO SIGNAL OUTPUT
S0REQI0	MY MAIN STORE BUS STORE REQUEST SIGNAL INPUT (FUSED)
S0REQ00	MY MAIN STORE BUS STORE REQUEST SIGNAL OUTPUT
S1ACI0	OTHER MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL INPUT
S1AC00	OTHER MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL OUTPUT
S1CMI0	OTHER MAIN STORE BUS STORE COMPLETE INPUT
S1CM00	OTHER MAIN STORE BUS STORE COMPLETE SIGNAL OUTPUT
S1CWI0	OTHER MAIN STORE BUS COMPLEMENT CORRECTION SIGNAL INPUT
S1CW00	OTHER MAIN STORE BUS COMPLEMENT CORRECTION SIGNAL OUTPUT
S1C0I0-S1C3I0	OTHER MAIN STORE BUS CONTROL LEAD INPUTS, BITS 0-3
S1C000-S1C300	OTHER MAIN STORE BUS CONTROL LEAD OUTPUTS, BITS 0-3
S1ERAI0	OTHER MAIN STORE BUS ERROR SIGNAL A INPUT

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
S1ERA00	OTHER MAIN STORE BUS ERROR SIGNAL A OUTPUT
S1ERBI0	OTHER MAIN STORE BUS ERROR SIGNAL B INPUT
S1ERB00	OTHER MAIN STORE BUS ERROR SIGNAL B OUTPUT
S1ERCI0	OTHER MAIN STORE BUS ERROR SIGNAL C INPUT
S1ERC00	OTHER MAIN STORE BUS ERROR SIGNAL C OUTPUT
S1G0I0	OTHER MAIN STORE BUS STORE GO SIGNAL INPUT
S1G000	OTHER MAIN STORE BUS STORE GO SIGNAL OUTPUT
S1REQI0	OTHER MAIN STORE BUS STORE REQUEST SIGNAL INPUT
S1REQ00	OTHER MAIN STORE BUS STORE REQUEST SIGNAL OUTPUT
TEST.DR0	CONTROL SIGNAL THAT INDICATES DR IS BEING TESTED
TSS0PH0	TEST SET ACCESS POINT, PARITY HIGH ON THE STORE DATA BUS
TSS0PL0	TEST SET ACCESS POINT, PARITY LOW ON THE STORE DATA BUS
TSSD000-TSSD150	TEST SET ACCESS POINT, BITS 0 THROUGH 15 OF THE STORE DATA BUS
TSS0ERA0-TSS0ERC0	TEST SET ACCESS POINT, MY STORE ERROR SIGNAL A-C
TSS0G00	TEST SET ACCESS POINT, MY STORE GO SIGNAL
ZIBT001-ZIBT181	ZERO TO THE RIGHT OF BIT 0-18 (PA PLUS 1 CIRCUITRY ATTACHED TO PA REGISTER)

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

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PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 1

PROCESSOR BUS CONTROLLER 0

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PBC0	02-21	FA1029	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		111			SE2.REL0	8H4
BOSR00	0	100	4/2		BOSR0	4F2
BR0000	I	118	2/4	202	BR0I0	3A6
BR0020	I	018	2/4	202	BR1I0	3A6
BR0040	I	317	2/4	202	BR2I0	3A5
BR0060	I	014	2/4	202	BR3I0	3A4
BR0080	I	313	2/3	202	BR4I0	3A3
BR0100	I	113	2/3	202	BR5I0	3A3
BR0120	I	010	2/3	202	BR6I0	3A1
CW0	I	309	4/2		CWI0	5A3
C19.20	I	002	8/3		CONT161	9A2
DR00A	0	307	1/5,1/8 4/12,4/13 4/14,4/15 7/7		OR0A	7H5
OR00B	0	107	4/2,4/6 4/7,4/8 4/9,4/10 4/11		OR0B	7H4
EFETCH0A	0	019	4/6,4/7 4/12,4/13 4/14,4/15		FETCH0	6H2
ELNOP00B	I	300	1/8		LNOP0	6A5
EN.S0SP0	0	109	4/2		RE010C	12G8
EN.S00A	0	011	4/12,4/13 4/14,4/15 11/2,11/3		TRE0.0A	11H3
EN.S00B	0	310	4/5,4/6 4/7,4/8 4/9.4/10 4/11,11/1		TRE0.0B	11H2
ENGDR1	0I	308	4/3		ENGDR1	7H3
EN0.INV1	I	211	4/3		INHINVI1	10A5
EN1.INV1	0	301	4/3		ENENGOR1	10H5
ER.S0T00	0	204	5/1		T0.CK0	9H2
EROSERC0	I	303	4/2		IN.IOLI0	7A6
ESARPA0A	0	009	4/12,4/13 4/14,4/15		GSARPA0	6H4
F204LC0B	I	216	1/13		F204LC0	2A2
F204L90B	I	217	1/13		F204L90	2A1
F204RA0B	I	115	1/13		F204RA0	2A1
GB000	OT	212	2/4		MM1.GB0	4F7
GB020	OT	112	2/4		MM2.GB0	4F6
GB040	OT	312	2/4		RW.GB0	4F6
GB060	OT	013	2/4		IOLE.GB0	4F4
GB080	OT	114	2/3		UP0.GB0	4F3
GB100	OT	214	2/3		IS0.GB0	4F3
GB120	OT	007	2/3		BOSR.GB0	4F1
I.OFF00A	0	207	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15		I.00A	6H3
IFF01	I	001	1/5		IFFI1	6A4
MD.SDR00	I	006	1/5		ST.ORI0	7A4
MO.ZOR00	0I	202	1/5		CL.DR0	6H4
MPS030	I	105	12/8		MPSCB0	6A2
MPS050	I	205	12/8		MPSCA0	6A2
MS070	I	103	5/7		MSAI0	10A3
MS080	I	003	5/14		MSBI0	10A4
OPF00	I	201	1/5		FIL0	6A3
P01	I	104	8/3		P01	2A7
P21	I	004	8/3		P21	7A1

SYMBOL NO. 1 (CONT)

PROCESSOR BUS CONTROLLER 0

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PBC0	02-21	FA1029	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
P31	I	203	8/3		P31	5A1
R.WFF1A	0	305	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15		R.WFF1	12H2
R.WS01A	0	304	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15		R.W1A	12H2
R.WS01B	0	005	11/1,11/2 11/3		R.W1B	12H1
S0CMI0	I0	302	4/2 4/3,7/3 TO CONN CKT		TSCMI0	10A2
S0CM00	0	210	13/4 TO CONN CKT		SCM0	12G8
S0C0I0	I	102	13/1 TO CONN CKT		SC0I0	12A7
S0C000	0	012	TO CONN CKT		TSC00	12G7
S0C1I0	I	017	13/1 TO CONN CKT		SC1I0	12A5
S0C100	0	110	TO CONN CKT		TSC10	12H5
S0C2I0	I	316	13/1 TO CONN CKT		SC2I0	12A3
S0C200	0	108	TO CONN CKT		TSC20	12H3
S0C3I0	I	219	13/1 TO CONN CKT		SC3I0	12A1
S0C300	0I	311	5/7 TO CONN CKT		TSC30	12H2
S0ERCI0	I	213	4/2		SERCI0	8A3
S0GDI0	I	306	13/4 TO CONN CKT		SGDI0	11A5
S0GD00	0I	209	5/10 4/2 TO CONN CKT		TSG00	11H5
S0REOI0	I	106	13/4 TO CONN CKT		SREOI0	11A4
S0RE000	0	008	TO CONN CKT		TSRE00	11H4
S1CMI0	I	206	4/3		OSCMI0	7A8
TSS0G00	0	208			SGOD60	11H7
T104L10B	I	314	1/11		T104L10	2A0
T104L20B	I	318	1/11		T104L20	2A8
T204LC0B	I	015	1/11		T204LC0	2A3
T204L30B	I	016	1/11		T204L30	2A2
T204RA0B	I	315	1/11		T204RA0	2A5
T204RC0C	I	116	1/11		T204RC0	2A1
T204R30C	I	215	1/11		T204R30	2A3
T204R50C	I	117	1/11		T204R50	2A4
T304RB0B	I	101	1/11		T304RB0	2A0
T304RE0A	I	218	1/11		T304RE0	2A8
3T0540	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054C	PWR	000	14/2		+3	
	PWR	119	14/2		+3	
3V0540	PWR	000	(X)14/2	203	+3	
	PWR	119	(X)14/2	203	+3	

SYMBOL NO. 2

DOUBLE STORE READ AND STORE ERROR CIRCUITRY

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DSR	02-23	FA1046	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
AME.OME0	I	308	5/10		MSPHI0	2A8
BOSR00	I	008	4/1		BOSRI0	2A5
BR0140	I	210	2/3		BR14I0	5A4
BR0150	I	113	2/3	202	BR15I0	5A3
CW0	0	100	4/1,4/3		CW0	5H5
OR00B	I	218	4/1		OR0I0	5A2
EA.DMTL0	0	007	TO CTLPNL CKT	202	MSPH0	2H8
ECL.A.00	0	304	5/10,5/14		S0ERCEC0	3H2
ECL.ROS0	I	108	4/3		CL.ROSI0	2A1
EN.S0SP0	I	214	4/1		S0ENI0	3A0
EN.S1SP0	I	314	4/3		S1ENI0	4A0
EROSERC0	0	004	4/1,4/3		SERCROS0	2H1
ERSERC0	0	215	5/1		TSERC0	3H0
ERS0ERA0	0	013	5/2		S0ERA0A	3H6
ERS0ERB0	0	313	5/1		TS0ERB0A	3H4
ERS1ERA0	0	117	5/1		S1ERA0	4H4
ERS1ERB0	0	018	5/1		TS1ERB0	4H3
ERU1	0	107	1/2,1/3 1/6,1/8		ERU1	2H7
F204L90B	I	116	1/13		F204L90	5A1
GBPH0	OT	206	2/2		MMSP.GB0	5H4
GB140	OT	105	2/3		CW0.GB0	5H4
GB150	OT	211	2/3		BEC0.GB0	5H3
GB160	OT	006	2/2		CW1.GB0	5H4
GB170	OT	205	2/2		BEC1.GB0	5H3
IF204LC1	I	IC	1/10		F204LC1	5C0
IF204RA1	I	IC	1/10		F204RA1	5C0
MDA.BD0A	OT	IC203	4/2		TSERCB0B	2H2
	OT I	203	1/10 7/8,7/11 7/12,7/13 7/14,7/15 7/16,7/17 7/18		TSERCB0B	2H2
MDA.BD0B	OT	IC103	4/2		TSERCB0A	2H2
	OT I	103	1/10 7/9,7/10 11/1,11/2 11/3		TSERCB0A	2H3
MDERCRT0	I	216	1/5		ST.ERUI0	2A7
MDGD0I0A	OT	IC104	4/2		TSERCG0A	2H0
	OT I	104	1/10 7/8,7/11 7/12,7/13 7/14,7/15 7/16,7/17 7/18		TSERCG0A	2H1
MDGD0I0B	OT	IC204	4/2		TSERCG0B	2H0
	OT I	204	1/10 11/1,11/2 11/3		TSERCG0B	2H0
MS100	I	307	5/12		MS0	3A3
P21	I	208	8/3		P21	2A3
P31	I	118	8/3		P31	2A6
SERC.CC0	0I	300	1/2,1/3 1/6		SERC.CC0	2H5
S0ACI0	I	213	13/4 TO CONN CKT		S0ACI0	3A7
S0AC00	0	111	7/3 TO CONN CKT		TS0AC0	3G8
S0CMI0	0	311	4/1		S0ERC.M0	3H3
S0CWI0	I	212	13/4 TO CONN CKT		S0CWI0	3A8
S0CW00	0	009	7/3 TO CONN CKT		TS0CW0	3G9
S0ERAI0	I	219	TO CONN CKT		S0ERAI0	3A6

SYMBOL NO. 2 (CONT)

DOUBLE STORE READ AND STORE ERROR CIRCUITRY

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DSR	02-23	FA1046	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
S0ERA00	0	312	13/1 TO CONN CKT		S0ERA00	3H6
S0ERBI0	I	019	TO CONN CKT		S0ERBI0	3A4
S0ERB00	0	112	13/1 TO CONN CKT		S0ERB00	3H4
S0ERCI0	I	014	8/3 4/1 TO CONN CKT		S0ERCIA0	3A1
S0ERC00	0	115	13/1 TO CONN CKT		S0ERC00	3H1
S0G000	I	109	4/1		S0GOI0	3A4
S1ACI0	I	309	TO CONN CKT		S1ACI0	4A6
S1AC00	0	106	TO CONN CKT		TS1AC0	4H6
S1CMI0	0	317	4/3		S1ERC.M0	4H1
S1CWI0	I	306	TO CONN CKT		S1CWI0	4A7
S1CW00	0	209	TO CONN CKT		TS1CW0	4G7
S1ERAI0	I	012	TO CONN CKT		S1ERAI0	4A4
S1ERA00	0	217	TO CONN CKT		S1ERA00	4H5
S1ERBI0	I	005	TO CONN CKT		S1ERBI0	4A3
S1ERB00	0	017	TO CONN CKT		S1ERB00	4H3
S1ERCI0	I	318	4/3 TO CONN CKT		S1ERCIA0	4A1
S1ERC00	0	316	TO CONN CKT		S1ERC00	4H1
S1G000	I	114	4/3		S1GOI0	4A2
TEST.DR0	I	207	1/5		TEST.OR0	2A5
TSS0ERA0	0	016			S0ERA0B	3H6
TSS0ERB0	0	315			S0ERB0B	3H5
TSS0ERC0	0	015			S0ERC0B	3H2
T204LC0B	I	011	1/11		T204LC0	5A2
T204RA0B	I	010	1/11		T204RA0	5A2
3T054D	GRD	0GD		203	GRD	
	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054C	PWR	000	14/2		+3	
	PWR	119	14/2		+3	
3V0540	PWR	000	(X)14/2	203	+3	
	PWR	119	(X)14/2	203	+3	

PART OF FS 4
SYMBOL(S) 1 2

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	8A

BELL LABORATORIES
SD-1C900-01
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02/08/79

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 3

PROCESSOR BUS CONTROLLER 1

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PBC1	02-22	FA1029	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
		209			TSGD0	11H5
BOSR10		100			BOSR0	4F2
BR0010	I	118	2/4	202	BR010	3A6
BR0030	I	018	2/4	202	BR110	3A6
BR0050	I	317	2/4	202	BR210	3A5
BR0070	I	014	2/4	202	BR310	3A4
BR0090	I	313	2/3	202	BR410	3A3
BR0110	I	113	2/3	202	BR510	3A3
BR0130	I	010	2/3	202	BR610	3A1
CW0	I	309	4/2		CHI0	5A3
C19.20	I	002	8/3		CONT161	9A2
OR10A	0	307	1/1,1/4 4/5,6/3 11/1,11/2 11/3		OR0A	7H5
OR10B		107			OR0B	7H4
ECL.ROS0	0	111	4/2		SEZ.REL0	8H4
EFETCH0B	0	019	4/5,4/8 4/9,4/10 4/11		FETCH0	6H2
ELNDP10B	I	300	1/1		LNOP0	6A5
EN.S1SP0	0	109	4/2		RED10C	12G8
EN.S10A	0	011	4/12,4/13 4/14,4/15 11/2,11/3		TRED.0A	11H3
EN.S10B	0	310	4/5.4/6 4/7,4/8 4/9,4/10 4/11,11/1		TRE0.0B	11H2
ENGDR1	0I	308	4/1		ENGDR1	7H3
ENO.INV1	0	301	4/1		ENENGDR1	10H5
EN1.INV1	I	211	4/1		INHINV11	10A5
ER.S1TD0	0	204	5/1		TO.CK0	9H2
EROSERC0	I	303	4/2		IN.IOLI0	7A6
ESARPA0B	0	009	4/5,4/6 4/7,4/8 4/9,4/10 4/11		GSARPA0	6H4
F204LC0B	I	216	1/13		F204LC0	2A2
F204L90B	I	217	1/13		F204L90	2A1
F204RA0B	I	115	1/13		F204RA0	2A1
GB010	OT	212	2/4		MM1.GB0	4F7
GB030	OT	112	2/4		MM2.GB0	4F6
GB050	OT	312	2/4		RW.GB0	4F6
GB070	OT	013	2/4		IOLE.GB0	4F4
GB090	OT	114	2/3		UP0.GB0	4F3
GB110	OT	214	2/3		ISO.GBD	4F3
GB130	OT	007	2/3		BOSR.GB0	4F1
1.OFF10A	0	207	7/3,11/1 11/2,11/3		1.D0A	6H3
IFF11	I	001	1/4		IFF11	6A4
MO.SOR10	I	006	1/4		ST.ORI0	7A4
MD.ZOR10	DI	202	1/4		CL.OR0	6H4
MPS030	I	105	12/8		MPSCB0	6A2
MPS050	I	205	12/8		MPSCA0	6A2
MS070	I	003	5/7		MSBI0	10A4
MS080	I	103	5/14		MSAI0	10A3
OPF10	I	201	1/4		FIL0	6A3
P01	I	104	8/3		P01	2A7
P21	I	004	8/3		P21	7A1
P31	I	203	8/3		P31	5A1
R.WFF1B	0	305	11/1,11/2 11/3		R.WFF1	12H2

SYMBOL NO. 3 (CONT)

PROCESSOR BUS CONTROLLER 1

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PBC1	02-22	FA1029	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
R.WS11A	0	304	4/5,4/8 4/9,4/10 4/11,4/12 4/13,4/14 4/15		R.W1A	12H2
R.WS11B	0	005	11/1,11/2 11/3		R.W1B	12H1
S0CMI0	I	206	4/1		OSCMI0	7A8
S1CMI0	I0	302	4/2 4/1 TO CONN CKT		TSCMI0	10A2
S1CM00	0	210	TO CONN CKT		SCM0	12G8
S1C0I0	I	102	TO CONN CKT		SC0I0	12A7
S1C000	0	012	TO CONN CKT		TSC00	12G7
S1C1I0	I	017	TO CONN CKT		SC1I0	12A5
S1C100	0	110	TO CONN CKT		TSC10	12H5
S1C2I0	I	316	TO CONN CKT		SC2I0	12A3
S1C200	0	108	TO CONN CKT		TSC20	12H3
S1C3I0	I	219	TO CONN CKT		SC3I0	12A1
S1C300	0I	311	TO CONN CKT		TSC30	12H2
S1ERCI0	I	213	4/2		SERCI0	8A3
S1G0I0	I	306	TO CONN CKT		SG0I0	11A5
S1G000	0	208	4/2 TO CONN CKT		SGOD60	11H7
S1REOI0	I	106	TO CONN CKT		SREDI0	11A4
S1REQ00	0	008	TO CONN CKT		TSRE00	11H4
T104L10B	I	314	1/11		T104L10	2A0
T104L20B	I	318	1/11		T104L20	2A8
T204LC0B	I	015	1/11		T204LC0	2A3
T204L30B	I	016	1/11		T204L30	2A2
T204RA0B	I	315	1/11		T204RA0	2A5
T204RC0C	I	116	1/11		T204RC0	2A1
T204R30C	I	215	1/11		T204R30	2A3
T204R50C	I	117	1/11		T204R50	2A4
T304RB0B	I	101	1/11		T304RB0	2A0
T304RE0A	I	218	1/11		T304RE0	2A8
3T0540	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V056C	PWR	000	14/2		+3	
	PWR	119	14/2		+3	
3V0540	PWR	000	(X)14/2	203	+3	
	PWR	119	(X)14/2	203	+3	

SYMBOL NO. 4

ADR PARITY PREDICT CIRCUIT

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
ADRPTPRO	02-25	FA1032	C	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
PA000	I	216	4/15	202	PA.0010	5A1
PA010	I	016	4/14	202	PA.0110	5A2
PA020	I	315	4/13	202	PA.0210	5A3
PA030	I	115	4/12	202	PA.0310	5A4
PA040	I	215	4/11	202	PA.0410	5A5
PA050	I	019	4/10	202	PA.0510	5A5
PA060	I	318	4/9	202	PA.0610	5A6
PA070	I	118	4/8	202	PA.0710	5A7
PA080	I	218	4/15	202	PA.0810	6A1
PA090	I	018	4/14	202	PA.0910	6A2
PA100	I	317	4/13	202	PA.1010	6A3
PA110	I	117	4/12	202	PA.1110	6A4
PA120	I	217	4/11	202	PA.1210	6A5
PA130	I	207	4/10	202	PA.1310	6A5
PA140	I	007	4/9	202	PA.1410	6A6
PA150	I	306	4/8	202	PA.1510	6A7
PA160	I	106	4/7	202	PA.1610	6A8
PA170	I	206	4/6	202	PA.1710	6A9
PA180	I	006	4/7	202	PA.1810	6A9
PHCOM1	0	312	4/5		TOPH1	6G9
PLCOM1	0	304	4/5		TOPL1	3G7

SYMBOL NO. 5

STORE ADDRESS AND BUFFER REGISTERS
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBTPHPL	02-18	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
		106			ZTRA1	9H5
		204			XSIROB0	8H5
		205			SOBI0	3A8
		303			XSIROA0	8H6
		306			ZTRB1	9H1
		316			MINTRP0	8A5
OR10A	I	300	4/3		ORI0	6A4
EFETCH0B	I	311	4/3		NFETI0	5A5
ELNDP00B	I	013	1/8		LNOPI0	8A2
EN.S00B	I	201	4/1		REQS010	2A1
EN.S10B	I	001	4/3		REQS110	2A5
ESARPA0B	I	111	4/3		SAR.PAI0	6A2
FP204L91	0	IC	7/8		F204L91	5H0
FP204RC1	0	IC	7/8		F204RC1	9F7
FP204R31	0	IC	7/8		F204R31	5H6
FP204R51	0	IC	7/8		F204R51	5H0
FP204R61	0	IC	7/8		F204R61	6H1
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC0B	I	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1

SYMBOL NO. 5 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBTPHPL	02-18	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
F204R60B	I	315	1/13		F204R60	6A1
F3D4RE0B	I	214	1/13		F304RE0	7A2
F3D4R70B	I	005	1/13		PAD0	3A8
GBPH0	OT	207	2/2		GB.BS10	9H3
	I	312	2/2		GB.BI0	5A1
GBPL0	OT	007	2/2		GB.AS10	9H6
	I	112	2/2		GB.AI0	5A2
1.OFF00A	I	100	4/1		1.OFF10	6A4
IBPH0		206			IB.B10	8H2
IBPL0	0	006	1/6	202	IB.A10	8H2
ICDR80	0	IC	7/8		OR0	6D8
ICSARPH1	0	IC	7/8		SARB1	5H4
ICSARPL1	0	IC	7/8		SARA1	5H5
ICSOPH0	0	IC	7/8		TS00B	4H4
ICSOPL0	0	IC	7/8		TS00A	4E9
ICSORPH1	0	IC017	7/8		SORB1	7H5
ICSDRPL1	0	IC314	7/8		SORA1	7H5
IFF11	I	210	1/4		IFF1	8A4
IGBPHA0	I	IC	7/8		AKBG10	9A2
IGBPHB0	I	IC	7/8		AIBG10	9A2
IGBPHC0	I	IC	7/8		DKBG10	9A3
IGBPHD0	I	IC	7/8		OIBG10	9A3
IGBPH1A	0	IC	7/8		GB.BD1A	5H1
IGBPH1B	0	IC	7/8		GB.BD1B	7E8
IGBPLA0	I	IC	7/8		AKAG10	9A6
IGBPLB0	I	IC	7/8		AIAG10	9A6
IGBPLC0	I	IC	7/8		OKAG10	9A6
IGBPLD0	I	IC	7/8		OIAG10	9A6
IGBPL1A	0	IC	7/8		GB.AD1A	5H2
IGBPL1B	0	IC	7/8		GB.AD1B	7E8
IRWSO180	0	IC	7/8		R.WS010	3B9
PAPH0		104			PA.B10	6H3
PAPL0		304			PA.A10	6H3
PHCOM1	I	011	4/4		COMBI0	9A1
PLCOM1	I	211	4/4		COMAI0	9A4
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS011	3A1
R.WS11A	I	110	4/3		R.WS111	4A0
SA0PHI0	I	202	13/1 TO CONN CKT		SA0BI0	2A1
SA0PH00	0	102	TO CONN CKT		TSA0BD0	2G3
SA0PL10	I	002	13/1 TO CONN CKT		SA0AI0	2G3
SA0PLD0	0	003	TO CONN CKT		TSA0A00	2G4
SA1PHI0	I	301	TO CONN CKT		SA1BI0	2A6
SA1PH00	0	203	TO CONN CKT		TSA1BC0	2G7
SA1PLI0	I	101	TO CONN CKT		SA1AI0	2A7
SA1PL00	0	103	TO CONN CKT		TSA1A00	2G9
SDRPH1		017			SDRB1	3H0
SDRPL1		314			SORA1	3H5

PART OF FS 4
SYMBOL(S) 3 4 5

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

BELL LABORATORIES
SD-1C900-01
B4CB

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12/01/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 5 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBTPHPL	02-18	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SD0PHI0	01	018	13/1 TO CONN CKT		SD0BR0	3H4
SD0PH00	01	218	TO CONN CKT		TSD0BWD0	3H1
SD0PL10	01	117	11/1 13/1 TO CONN CKT		SD0AR0	3H8
SD0PL00	01	317	11/1 TO CONN CKT		TSD0AWD0	3H5
SD1PHI0	01	019	TO CONN CKT		SD1BR0	4H4
SD1PH00	01	219	TO CONN CKT		TSD1BW00	4H1
SD1PLI0	01	118	11/1 TO CONN CKT		SD1AR0	4H8
SD1PL00	01	318	11/1 TO CONN CKT		TSD1AW00	4H5
SIRPH0	01	004	11/1 1/6	202	SIR0.B0	8H4
SIRPL0	01	105	11/1	202	SIR0.A0	8H5
TP2D4L91	0	1C	7/8		T2D4L91	5H2
TP2D4R31	0	1C	7/8		T2D4R31	5H3
TP2D4R51	0	1C	7/8		T2D4R51	5B7
TP2D4R61	0	1C	7/8		T2D4R61	6C0
TSSDPH0	0	217			SD0B0	3H1
TSSDPL0	0	114			SD0A0	3H6
T1D4L10A	I	215	1/11		T1D4L10	7A1
T1D4L20A	I	015	1/11		T1D4L20	7A5
T2D4LC0A	I	108	1/11		T2D4LC0	5A4
T2D4L90A	I	009	1/11		T2D4L90	5A2
T2D4R30B	I	010	1/11		T2D4R30	5A3
T2D4R50B	I	309	1/11		T2D4R50	5A3
T2D4R60B	I	109	1/11		T2D4R60	6A0
T3D4RE0B	I	208	1/11		T3D4RE0	7A1
3T054A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0218T	I	012			2TRA11	9A5
	I	212			2TRB11	9A1
	GRD	319			GRD	
3V054A	PWR	000	(X)14/1	203	+3	
	PWR	119	(X)14/1	203	+3	
3V054B	PWR	000	14/1		+3	
	PWR	119	14/1		+3	

SYMBOL NO. 6

STORE ADDRESS REGISTER
(BITS 19 AND 17)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1917	02-20	FA1030	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		002			PA.B10	3H1
		308			2TRB1	4H1
DR00B	I	116	4/1		DR0	3A5
EFETCH0A	I	216	4/1		NFETI0	3A7
EN.S00B	I	210	4/1		REQS0I0	2A1
EN.S10B	I	307	4/3		REQS1I0	2A0
ESARPA0B	I	016	4/3		SAR.PAI0	3A2
F2D4LC0B	I	012	1/13		F2D4LC0	4A3
F2D4L90B	I	111	1/13		F2D4L90	3A0
F2D4RC0C	I	014	1/13		F2D4RC0	4A2
F2D4R50C	I	313	1/13		F2D4R50	3A4
F2D4R60C	I	113	1/13		F2D4R60	3A0
F92D4L91	0	1C	7/9		F2D4L91	3H0
F92D4RC1	0	1C	7/9		F2D4RC1	4H2
GB170	01	007	2/2		GB.AS10	4H6
GB190	01	106	2/2		GB.BS10	4H6
ICSAR171	0	1C	7/9		SAR.A1	3H7
ICSAR191	0	1C	7/9		SAR.B1	3H6
IGB17A0	I	1C	7/9		TIGBAA0	4A6
IGB17B0	I	1C	5/5		TIGBAC0	4A6
IGB171A	0	1C	5/5,7/9		GB.A01	4H7
IGB19A0	I	1C	7/9		TIGBBA0	4A6
IGB19B0	I	1C	5/5		TIGBBC0	4A6
IGB191A	0	1C	5/5,7/9		GB.B01	4H5
PA170	0	301	4/4	202	PA.A10	3H2
SA01710	I	217	13/1 TO CONN CKT		SA0A10	2A7
SA01700	0	101	TO CONN CKT		TSA0A00	2H7
SA01910	I	207	13/1 TO CONN CKT		SA0B10	2A3
SA01900	0	201	TO CONN CKT		TSA0B00	2H3
SA11710	I	019	TO CONN CKT		SA1AI0	2A5
SA11700	0	001	TO CONN CKT		TSA1A00	2H5
SA11910	I	219	TO CONN CKT		SA1BI0	2A1
SA11900	0	300	TO CONN CKT		TSA1B00	2H2
T2D4LC0B	I	017	1/11		T2D4LC0	3A5
T2D4L90B	I	316	1/11		T2D4L90	3A1
T2D4R30C	I	118	1/11		T2D4R30	3A4
T2D4R50C	I	018	1/11		T2D4R50	3A5
T2D4R60C	I	317	1/11		T2D4R60	3A1
T92D4L91	0	1C	7/9		T2D4L91	3B9
T92D4R31	0	1C	5/5,7/9		T2D4R31	3B9
2IBT161	I	212	4/7		2TRAI1	4A4
2IBT171	0	306	4/7		2TRA1	4H4
2IBT181	I	112	4/7		2TRB11	4A1
3T054D	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054C	PWR	000	14/2		+3	
	PWR	119	14/2		+3	
3V054D	PWR	000	(X)14/2	203	+3	
	PWR	119	(X)14/2	203	+3	

SYMBOL NO. 7

STORE ADDRESS REGISTER
(BITS 18 AND 16)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1816	02-19	FA1030	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
DR00B	I	116	4/1		DR0	3A5
EFETCH0A	I	216	4/1		NFETI0	3A7
EN.S00B	I	210	4/1		REQS0I0	2A1
EN.S10B	I	307	4/3		REQS1I0	2A0
ESARPA0B	I	016	4/3		SAR.PAI0	3A2
F2D4LC0B	I	012	1/13		F2D4LC0	4A3
F2D4L90B	I	111	1/13		F2D4L90	3A0
F2D4RC0C	I	014	1/13		F2D4RC0	4A2
F2D4R50C	I	313	1/13		F2D4R50	3A4
F2D4R60C	I	113	1/13		F2D4R60	3A0
F82D4L91	0	1C	7/10		F2D4L91	3H0
F82D4RC1	0	1C	7/10		F2D4RC1	4H2
GB160	01	007	2/2		GB.AS10	4H6
GB180	01	106	2/2		GB.BS10	4H6
ICSAR161	0	1C	7/10		SAR.A1	3H7
ICSAR181	0	1C	7/10		SAR.B1	3H6
IGB16A0	I	1C	7/10		TIGBAA0	4A6
IGB16B0	I	1C	5/6		TIGBAC0	4A6
IGB161A	0	1C	5/6,7/10		GB.A01	4H7
IGB18A0	I	1C	7/10		TIGBBA0	4A6
IGB18B0	I	1C	5/6		TIGBBC0	4A6
IGB181A	0	1C	5/6,7/10		GB.B01	4H5
PA160	0	301	4/4	202	PA.A10	3H2
PA180	0	002	4/4	202	PA.B10	3H1
SA01610	I	217	13/1 TO CONN CKT		SA0AI0	2A7
SA01600	0	101	TO CONN CKT		TSA0A00	2H7
SA01810	I	207	13/1 TO CONN CKT		SA0BI0	2A3
SA01800	0	201	TO CONN CKT		TSA0B00	2H3
SA11610	I	019	TO CONN CKT		SA1AI0	2A5
SA11600	0	001	TO CONN CKT		TSA1A00	2H5
SA11810	I	219	TO CONN CKT		SA1BI0	2A1
SA11800	0	300	TO CONN CKT		TSA1B00	2H2
T2D4LC0B	I	017	1/11		T2D4LC0	3A5
T2D4L90B	I	316	1/11		T2D4L90	3A1
T2D4R30C	I	118	1/11		T2D4R30	3A4
T2D4R50C	I	018	1/11		T2D4R50	3A5
T2D4R60C	I	317	1/11		T2D4R60	3A1
T82D4L91	0	1C	7/10		T2D4L91	3B9
T82D4R31	0	1C	5/6,7/10		T2D4R31	3B9
2IBT151	I	212	4/8		2TRAI1	4A4
2IBT161	0	306	4/6		2TRA1	4H4
2IBT171	I	112	4/6		2TRBI1	4A1
2IBT181	0	308	4/6		2TRB1	4H1
3T054D	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054C	PWR	000	14/2		+3	
	PWR	119	14/2		+3	
3V054D	PWR	000	(X)14/2	203	+3	
	PWR	119	(X)14/2	203	+3	

PART OF FS 4
SYMBOL(S) 5 6 7

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B4CC

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12/01/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 8

STORE ADDRESS AND BUFFER REGISTERS
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1507	02-17	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		005			PAD0	3A8
		011			COMBI0	9A1
		205			SDBI0	3A8
		211			COMAI0	9A4
DR008	I	300	4/1		DRI0	6A4
EFETCH08	I	311	4/3		NFETI0	5A5
ELMINT0	I	316	1/8		MINTRP0	8A5
ELNOP008	I	013	1/8		LNOPI0	8A2
EN.S008	I	201	4/1		REDS0I0	2A1
EN.S108	I	001	4/3		REDS1I0	2A5
ESARPA08	I	111	4/3		SAR.PAI0	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC08	I	113	1/13		F204RC0	9A2
F204R308	I	213	1/13		F204R30	5A7
F204R508	I	115	1/13		F204R50	5A1
F204R608	I	315	1/13		F204R60	6A1
F304RE08	I	214	1/13		F304RE0	7A2
F7204L91	O	IC	7/11		F204L91	5H0
F7204RC1	O	IC	7/11		F204RC1	9F7
F7204R31	O	IC	7/11		F204R31	5H6
F7204R51	O	IC	7/11		F204R51	5H0
F7204R61	O	IC	7/11		F204R61	6H1
GB070	OT	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AI0	5A2
GB150	OT	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BI0	5A1
I.OFF00A	I	100	4/1		I.OFFI0	6A4
IB070	O	006	1/1,1/3 1/7	202	IB.A10	8H2
IB150		206			IB.B10	8H2
ICDR70	O	IC	7/11		DR0	608
ICSAR071	O	IC	7/11		SARA1	5H5
ICSAR151	O	IC	7/11		SARB1	5H4
ICSDR071	O	IC314	7/11		SDRA1	7H5
ICSDR151	O	IC017	7/11		SDRB1	7H5
ICSD070	O	IC	7/11		TSD0A	4E9
ICSD150	O	IC	7/11		TSD0B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB07A0	I	IC	7/11		AKAG10	9A6
IGB07B0	I	IC	7/11		AIAG10	9A6
IGB07C0	I	IC	7/11		DKAG10	9A6
IGB07D0	I	IC	7/11		DIAG10	9A6
IGB071A	O	IC	7/11		GB.AD1A	5H2
IGB071B	O	IC	7/11		GB.AD1B	7E8
IGB15A0	I	IC	7/11		AKBG10	9A2
IGB15B0	I	IC	7/11		AIBG10	9A2
IGB15C0	I	IC	7/11		DKBG10	9A3
IGB15D0	I	IC	7/11		DIBG10	9A3
IGB151A	O	IC	7/11		GB.BD1A	5H1
IGB151B	O	IC	7/11		GB.BD1B	7E8
IRWS0170	O	IC	7/11		R.WS0I0	3B9
MPS280	OI	303	12/7		XSIR0A0	8H6
MPS300	OI	204	12/7		XSIR0B0	8H5
PA070	O	304	4/4	202	PA.A10	6H3
PA150	O	104	4/4	202	PA.B10	6H3

SYMBOL NO. 8 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1507	02-17	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS0I1	3A1
R.WS11A	I	110	4/3		R.WS1I1	4A0
SA007I0	I	002	13/3 TO CONN CKT		SA0AI0	2A3
SA00700	O	003	TO CONN CKT		TSA0A00	2G4
SA015I0	I	202	13/3 TO CONN CKT		SA0BI0	2A1
SA01500	O	102	TO CONN CKT		TSA0B00	2G3
SA107I0	I	101	TO CONN CKT		SA1AI0	2A7
SA10700	O	103	TO CONN CKT		TSA1A00	2G9
SA115I0	I	301	TO CONN CKT		SA1BI0	2A6
SA11500	O	203	TO CONN CKT		TSA1B00	2G7
SDR071		314			SDRA1	3H5
SDR151		017			SDRB1	3H0
SD007I0	OI	117	11/3 13/2 TO CONN CKT		SD0AR0	3H8
SD00700	OI	317	11/3 TO CONN CKT		TSD0AW00	3H5
SD015I0	OI	018	13/2 TO CONN CKT		SD0BR0	3H4
SD01500	OI	218	TO CONN CKT		TSD0BW00	3H1
SD107I0	OI	118	11/3 TO CONN CKT		SD1AR0	4H8
SD10700	OI	318	11/3 TO CONN CKT		TSD1AW00	4H5
SD115I0	OI	019	TO CONN CKT		SD1BR0	4H4
SD11500	OI	219	TO CONN CKT		TSD1BW00	4H1
SIR070	OI	105	11/2	202	SIR0.A0	8H5
SIR150	OI	004	11/1 1/6,6/4	202	SIR0.B0	8H4
TSSD070	O	114			SD0A0	3H6
TSSD150	O	217			SD0B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R308	I	010	1/11		T204R30	5A3
T204R508	I	309	1/11		T204R50	5A3
T204R608	I	109	1/11		T204R60	6A0
T304RE08	I	208	1/11		T304RE0	7A1
T7204L91	O	IC	7/11		T204L91	5H2
T7204R31	O	IC	7/11		T204R31	5H3
T7204R51	O	IC	7/11		T204R51	5B7
T7204R61	O	IC	7/11		T204R61	6C0
2IBT061	I	012	4/9		2TRAI1	9A5
2IBT071	O	106	4/15		2TRA1	9H5
2IBT141	I	212	4/9		2TRBI1	9A1
2IBT151	O	306	4/7		2TRB1	9H1
3T054A	GRD	0GD		203	GRD	
	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054A	PWR	000	(X)14/1	203	+3	
	PWR	119	(X)14/1	203	+3	
3V054B	PWR	000	14/1		+3	
	PWR	119	14/1		+3	

SYMBOL NO. 9

STORE ADDRESS AND BUFFER REGISTERS
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1406	02-16	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		005			PAD0	3A8
		011			COMBI0	9A1
		206			IB.B10	8H2
		211			COMAI0	9A4
DR008	I	300	4/1		DRI0	6A4
EFETCH08	I	311	4/3		NFETI0	5A5
ELMINT0	I	316	1/8		MINTRP0	8A5
ELNOP008	I	013	1/8		LNOPI0	8A2
EN.S008	I	201	4/1		REDS0I0	2A1
EN.S108	I	001	4/3		REDS1I0	2A5
ESARPA08	I	111	4/3		SAR.PAI0	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC08	I	113	1/13		F204RC0	9A2
F204R308	I	213	1/13		F204R30	5A7
F204R508	I	115	1/13		F204R50	5A1
F204R608	I	315	1/13		F204R60	6A1
F304RE08	I	214	1/13		F304RE0	7A2
F6204L91	O	IC	7/12		F204L91	5H0
F6204RC1	O	IC	7/12		F204RC1	9F7
F6204R31	O	IC	7/12		F204R31	5H6
F6204R51	O	IC	7/12		F204R51	5H0
F6204R61	O	IC	7/12		F204R61	6H1
GB060	OT	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AI0	5A2
GB140	OT	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BI0	5A1
I.OFF00A	I	100	4/1		I.OFFI0	6A4
IB060	O	006	1/1,1/3 1/7	202	IB.A10	8H2
ICDR60	O	IC	7/12		DR0	608
ICSAR061	O	IC	7/12		SARA1	5H5
ICSAR141	O	IC	7/12		SARB1	5H4
ICSDR061	O	IC314	7/12		SDRA1	7H5
ICSDR141	O	IC017	7/12		SDRB1	7H5
ICSD060	O	IC	7/12		TSD0A	4E9
ICSD140	O	IC	7/12		TSD0B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB06A0	I	IC	7/12		AKAG10	9A6
IGB06B0	I	IC	7/12		AIAG10	9A6
IGB06C0	I	IC	7/12		DKAG10	9A6
IGB06D0	I	IC	7/12		DIAG10	9A6
IGB061A	O	IC	7/12		GB.AD1A	5H2
IGB061B	O	IC	7/12		GB.AD1B	7E8
IGB14A0	I	IC	7/12		AKBG10	9A2
IGB14B0	I	IC	7/12		AIBG10	9A2
IGB14C0	I	IC	7/12		DKBG10	9A3
IGB14D0	I	IC	7/12		DIBG10	9A3
IGB141A	O	IC	7/12		GB.BD1A	5H1
IGB141B	O	IC	7/12		GB.BD1B	7E8
IRWS0160	O	IC	7/12		R.WS0I0	3B9
MPS240	OI	303	12/7		XSIR0A0	8H6
MPS260	OI	204	12/7		XSIR0B0	8H5
MRF.STP0	I	205	1/6		SDBI0	3A8
PA060	O	304	4/4	202	PA.A10	6H3
PA140	O	104	4/4	202	PA.B10	6H3

SYMBOL NO. 9 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1406	02-16	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS0I1	3A1
R.WS11A	I	110	4/3		R.WS1I1	4A0
SA006I0	I	002	13/3 TO CONN CKT		SA0AI0	2A3
SA00600	O	003	TO CONN CKT		TSA0A00	2G4
SA014I0	I	202	13/3 TO CONN CKT		SA0BI0	2A1
SA01400	O	102	TO CONN CKT		TSA0B00	2G3
SA106I0	I	101	TO CONN CKT		SA1AI0	2A7
SA10600	O	103	TO CONN CKT		TSA1A00	2G9
SA114I0	I	301	TO CONN CKT		SA1BI0	2A6
SA11400	O	203	TO CONN CKT		TSA1B00	2G7
SDR061		314			SDRA1	3H5
SDR141		017			SDRB1	3H0
SD006I0	OI	117	11/3 13/2 TO CONN CKT		SD0AR0	3H8
SD00600	OI	317	11/3 TO CONN CKT		TSD0AW00	3H5
SD014I0	OI	018	13/2 TO CONN CKT		SD0BR0	3H4
SD01400	OI	218	TO CONN CKT		TSD0BW00	3H1
SD106I0	OI	118	11/3 TO CONN CKT		SD1AR0	4H8
SD10600	OI	318	11/3 TO CONN CKT		TSD1AW00	4H5
SD114I0	OI	019	TO CONN CKT		SD1BR0	4H4
SD11400	OI	219	TO CONN CKT		TSD1BW00	4H1
SIR060	OI	105	11/2	202	SIR0.A0	8H5
SIR140	OI	004	11/1 1/1,1/2	202	SIR0.B0	8H4
TSSD060	O	114			SD0A0	3H6
TSSD140	O	217			SD0B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R308	I	010	1/11		T204R30	5A3
T204R508	I	309	1/11		T204R50	5A3
T204R608	I	109	1/11		T204R60	6A0
T304RE08	I	208	1/11		T304RE0	7A1
T6204L91	O	IC	7/12		T204L91	5H2
T6204R31	O	IC	7/12		T204R31	5H3
T6204R51	O	IC	7/12		T204R51	5B7
T6204R61	O	IC	7/12		T204R61	6C0
2IBT051	I	012	4/10		2TRAI1	9A5
2IBT061	O	106	4/8		2TRA1	9H5
2IBT131	I	212	4/10		2TRBI1	9A1
2IBT141	O	306	4/8		2TRB1	9H1
3T054A	GRD	0GD		203	GRD	

PART OF FS 4
SYMBOL(S) 8 9

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	B4CD

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12/01/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 9 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1406	02-16	FA1024	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T054A	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054A	PWR	000	(X)14/1	203	+3	
	PWR	119	(X)14/1	203	+3	
3V054B	PWR	000	14/1		+3	
	PWR	119	14/1		+3	

SYMBOL NO. 10

STORE ADDRESS AND BUFFER REGISTERS
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1305	02-13	FA1024	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		005			PADO	3A8
		011			COMBIO	9A1
		206			IB.B10	8H2
		211			COMAIO	9A4
OR00B	I	300	4/1		ORIO	6A4
EFETCH0B	I	311	4/3		NFETIO	5A5
ELMINTO	I	316	1/8		MINTRPO	8A5
ELNOP00B	I	013	1/8		LNOPIO	8A2
EN.S00B	I	201	4/1		REOSOIO	2A1
EN.S10B	I	001	4/3		REOS1IO	2A5
ESARPA0B	I	111	4/3		SAR.PAIO	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC0B	I	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1
F204R60B	I	315	1/13		F204R60	6A1
F304RB0B	I	205	1/13		SOBIO	3A8
F304RE0B	I	214	1/13		F304RE0	7A2
F5204L91	O	IC	7/13		F204L91	5H0
F5204RC1	O	IC	7/13		F204RC1	9F7
F5204R31	O	IC	7/13		F204R31	5H6
F5204R51	O	IC	7/13		F204R51	5H0
F5204R61	O	IC	7/13		F204R61	6H1
GB050	OT	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AIO	5A2
GB130	OT	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BIO	5A1
I.OFF00A	I	100	4/1		I.OFFIO	6A4
IB050	O	006	1/1,1/3 1/7	202	IB.A10	8H2
ICOR50	O	IC	7/13		ORO	608
ICSAR051	O	IC	7/13		SARA1	5H5
ICSAR131	O	IC	7/13		SARB1	5H4
ICSDR051	O	IC314	7/13		SDRA1	7H5

SYMBOL NO. 10 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1305	02-13	FA1024	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ICSDR131	O	IC017	7/13		SDRB1	7H5
ICS0050	O	IC	7/13		TS00A	4E9
ICS0130	O	IC	7/13		TS00B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB05A0	I	IC	7/13		AKAG10	9A6
IGB05B0	I	IC	7/13		AIAG10	9A6
IGB05C0	I	IC	7/13		DKAG10	9A6
IGB0500	I	IC	7/13		DIAG10	9A6
IGB051A	O	IC	7/13		GB.AD1A	5H2
IGB051B	O	IC	7/13		GB.AD1B	7E8
IGB13A0	I	IC	7/13		AKBG10	9A2
IGB13B0	I	IC	7/13		AIBG10	9A2
IGB13C0	I	IC	7/13		DKBG10	9A3
IGB1300	I	IC	7/13		DIBG10	9A3
IGB131A	O	IC	7/13		GB.BD1A	5H1
IGB131B	O	IC	7/13		GB.BD1B	7E8
IRWS0150	O	IC	7/13		R.WS010	3B9
MPS200	OI	303	12/7		XSIR0A0	8H6
MPS220	OI	204	12/7		XSIR0B0	8H5
PA050	O	304	4/4	202	PA.A10	6H3
PA130	O	104	4/4	202	PA.B10	6H3
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS011	3A1
R.WS11A	I	110	4/3		R.WS111	4A0
SA00510	I	002	13/3 TO CONN CKT		SA0AIO	2A3
SA00500	O	003	TO CONN CKT		TSA0A00	2G4
SA01310	I	202	13/3 TO CONN CKT		SA0BIO	2A1
SA01300	O	102	TO CONN CKT		TSA0B00	2G3
SA10510	I	101	TO CONN CKT		SA1AIO	2A7
SA10500	O	103	TO CONN CKT		TSA1A00	2G9
SA11310	I	301	TO CONN CKT		SA1BIO	2A6
SA11300	O	203	TO CONN CKT		TSA1B00	2G7
SDR051		314			SDRA1	3H5
SDR131		017			SDRB1	3H0
SD00510	OI	117	11/3 13/2 TO CONN CKT		SD0AR0	3H8
SD00500	OI	317	11/3 TO CONN CKT		TS00AW00	3H5
SD01310	OI	018	13/2 TO CONN CKT		SD0BR0	3H4
SD01300	OI	218	TO CONN CKT		TS00BW00	3H1
SD10510	OI	118	11/3 TO CONN CKT		SD1AR0	4H8
SD10500	OI	318	11/3 TO CONN CKT		TS01AW00	4H5
SD11310	OI	019	TO CONN CKT		SD1BR0	4H4
SD11300	OI	219	TO CONN CKT		TS01BW00	4H1
SIR050	OI	105	11/3	202	SIR0.A0	8H5
SIR130	OI	004	11/1 1/1,1/2	202	SIR0.B0	8H4
TSSD050	O	114			SD0A0	3H6
TSSD130	O	217			SD0B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R30B	I	010	1/11		T204R30	5A3

SYMBOL NO. 10 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1305	02-13	FA1024	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T204R50B	I	309	1/11		T204R50	5A3
T204R60B	I	109	1/11		T204R60	6A0
T304RE0B	I	208	1/11		T304RE0	7A1
T5204L91	O	IC	7/13		T204L91	5H2
T5204R31	O	IC	7/13		T204R31	5H3
T5204R51	O	IC	7/13		T204R51	5B7
T5204R61	O	IC	7/13		T204R61	6C0
2IBT041	I	012	4/11		ZTRAI1	9A5
2IBT051	O	106	4/9		ZTRA1	9H5
2IBT121	I	212	4/11		2TRBI1	9A1
2IBT131	O	306	4/9		2TRB1	9H1
3T054A	GRD	0G0		203	GRD	
	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054A	PWR	000	(X)14/1	203	+3	
	PWR	119	(X)14/1	203	+3	
3V054B	PWR	000	14/1		+3	
	PWR	119	14/1		+3	

SYMBOL NO. 11

STORE ADDRESS AND BUFFER REGISTERS
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1204	02-12	FA1024	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		011			COMBIO	9A1
		206			IB.B10	8H2
		211			COMAIO	9A4
OR00B	I	300	4/1		ORIO	6A4
EFETCH0B	I	311	4/3		NFETIO	5A5
ELMINTO	I	316	1/8		MINTRPO	8A5
ELNOP00B	I	013	1/8		LNOPIO	8A2
EN.S00B	I	201	4/1		REOSOIO	2A1
EN.S10B	I	001	4/3		REOS1IO	2A5
ESARPA0B	I	111	4/3		SAR.PAIO	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L10B	I	005	1/13		PADO	3A8
F104L20A	I	313	1/13		F104L20	7A4
F104L20B	I	205	1/13		SOBIO	3A8
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC0B	I	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1
F204R60B	I	315	1/13		F204R60	6A1
F304RE0B	I	214	1/13		F304RE0	7A2
F4204L91	O	IC	7/14		F204L91	5H0
F4204RC1	O	IC	7/14		F204RC1	9F7
F4204R31	O	IC	7/14		F204R31	5H6

SYMBOL NO. 11 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1204	02-12	FA1024	A	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F4204R51	O	IC	7/14		F204R51	5H0
F4204R61	O	IC	7/14		F204R61	6H1
GB040	OT	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AIO	5A2
GB120	OT	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BIO	5A1
I.OFF00A	I	100	4/1		I.OFFIO	6A4
IB040	O	006	1/3,1/7	202	IB.A10	8H2
ICOR40	O	IC	7/14		ORO	608
ICSAR041	O	IC	7/14		SARA1	5H5
ICSAR121	O	IC	7/14		SARB1	5H4
ICSDR041	O	IC314	7/14		SDRA1	7H5
ICSDR121	O	IC017	7/14		SDRB1	7H5
ICS0040	O	IC	7/14		TS00A	4E9
ICS0120	O	IC	7/14		TS00B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB04A0	I	IC	7/14		AKAG10	9A6
IGB04B0	I	IC	7/14		AIAG10	9A6
IGB04C0	I	IC	7/14		DKAG10	9A6
IGB0400	I	IC	7/14		DIAG10	9A6
IGB041A	O	IC	7/14		GB.AD1A	5H2
IGB041B	O	IC	7/14		GB.AD1B	7E8
IGB12A0	I	IC	7/14		AKBG10	9A2
IGB12B0	I	IC	7/14		AIBG10	9A2
IGB12C0	I	IC	7/14		DKBG10	9A3
IGB1200	I	IC	7/14		DIBG10	9A3
IGB121A	O	IC	7/14		GB.BD1A	5H1
IGB121B	O	IC	7/14		GB.BD1R	7E8
IRWS0140	O	IC	7/14		R.WS010	3B9
MPS160	OI	303	12/7		XSIR0A0	8H6
MPS180	OI	204	12/7		XSIR0B0	8H5
PA040	O	304	4/4	202	PA.A10	6H3
PA120	O	104	4/4	202	PA.B10	6H3
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS011	3A1
R.WS11A	I	110	4/3		R.WS111	4A0
SA00410	I	002	13/3 TO CONN CKT		SA0AIO	2A3
SA00400	O	003	TO CONN CKT		TSA0A00	2G4
SA01210	I	202	13/3 TO CONN CKT		SA0BIO	2A1
SA01200	O	102	TO CONN CKT		TSA0B00	2G3
SA10410	I	101	TO CONN CKT		SA1AIO	2A7
SA10400	O	103	TO CONN CKT		TSA1A00	2G9
SA11210	I	301	TO CONN CKT		SA1BIO	2A6
SA11200	O	203	TO CONN CKT		TSA1B00	2G7
SDR041		314			SDRA1	3H5
SDR121		017			SDRB1	3H0
SD00410	OI	117	11/3 13/2		SD0AR0	3H8

PART OF FS 4
SYMBOL(S) 9 10 11

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 7D

BELL LABORATORIES

SD-1C900-01

B4CE

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12/01/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 11 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1204	02-12	FA1024	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
			TO CONN CKT			
S000400	OI	317	11/3		TSD0AW00	3H5
			TO CONN CKT			
S001210	OI	018	13/2		S00BR0	3H4
			TO CONN CKT			
S001200	OI	218	TO CONN CKT		TS00BW00	3H1
S010410	OI	118	11/3		S01AR0	4H8
			TO CONN CKT			
S010400	OI	318	11/3		TS01AW00	4H5
			TO CONN CKT			
S011210	OI	019	TO CONN CKT		S01BR0	4H4
S011200	OI	219	TO CONN CKT		TS01BW00	4H1
SIR040	OI	105	11/3	202	SIR0.A0	8H5
SIR120	OI	004	11/1	202	SIR0.B0	8H4
			1/1,1/3			
TSS0040	0	114			S00A0	3H6
TSS0120	0	217			S00B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R30B	I	010	1/11		T204R30	5A3
T204R50B	I	309	1/11		T204R50	5A3
T204R60B	I	109	1/11		T204R60	6A0
T304RE0B	I	208	1/11		T304RE0	7A1
T4204L91	0	IC	7/14		T204L91	5H2
T4204R31	0	IC	7/14		T204R31	5H3
T4204R51	0	IC	7/14		T204R51	5B7
T4204R61	0	IC	7/14		T204R61	6C0
2IBT031	I	012	4/12		2TRAI1	9A5
2IBT041	0	106	4/10		2TRA1	9H5
2IBT111	I	212	4/12		2TRBI1	9A1
2IBT121	0	306	4/10		2TRB1	9H1
3T054A	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054A	PWR	000	(X)14/1	203	+3	
	PWR	119	(X)14/1	203	+3	
3V054B	PWR	0GD	14/1		+3	
	PWR	119	14/1		+3	

SYMBOL NO. 12

STORE ADDRESS AND BUFFER REGISTERS
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1103	02-11	FA1024	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
		011			COMBIO	9A1
		206			IB.B10	8H2
		211			COMAIO	9A4
OR00A	I	300	4/1		DRIO	6A4
EFETCH0A	I	311	4/1		NFETIO	5A5
ELMINT0	I	316	1/8		MINTRP0	8A5
ELNOP00B	I	013	1/8		LNOPIO	8A2
EN.S00A	I	201	4/1		REQS0IO	2A1
EN.S10A	I	001	4/3		NEQS1IO	2A5
ESARPA0A	I	111	4/1		SAR.PAIO	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F104L20B	I	005	1/13		PAD0	3A8
	I	205	1/13		SOBIO	3A8
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC0B	I	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1
F204R60B	I	315	1/13		F204R60	6A1
F304RE0B	I	214	1/13		F304RE0	7A2
F3204L91	u	IC	7/15		F204L91	5H0
F3204RC1	0	IC	7/15		F204RC1	9F7
F3204R31	0	IC	7/15		F204R31	5H6
F3204R51	0	IC	7/15		F204R51	5H0
F3204R61	0	IC	7/15		F204R61	6H1
GB030	OT	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AI0	5A2
GB110	OT	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BI0	5A1
I.OFF00A	I	100	4/1		I.OFFI0	6A4
IB030	0	006	1/1,1/3	202	IB.A10	8H2
			1/7			
ICDR30	0	IC	7/15		OR0	6D8
ICSAR031	0	IC	7/15		SARA1	5H5
ICSAR111	0	IC	7/15		SARB1	5H4
ICSOR031	0	IC314	7/15		SDRA1	7H5
ICSOR111	0	IC017	7/15		SORB1	7H5
ICSO030	0	IC	7/15		TSD0A	4E9
ICSD110	0	IC	7/15		TSD0B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB03A0	I	IC	7/15		AKAG10	9A6
IGB03B0	I	IC	7/15		AIAG10	9A6
IGB03C0	I	IC	7/15		DKAG10	9A6
IGB03D0	I	IC	7/15		OIAG10	9A6
IGB031A	0	IC	7/15		GB.AD1A	5H2
IGB031B	0	IC	7/15		GB.AD1B	7E8
IGB11A0	I	IC	7/15		AKBG10	9A2
IGB11B0	I	IC	7/15		AIBG10	9A2
IGB11C0	I	IC	7/15		OKBG10	9A3
IGB11D0	I	IC	7/15		OIBG10	9A3
IGB111A	0	IC	7/15		GB.BD1A	5H1
IGB111B	0	IC	7/15		GB.BD1B	7E8
IRWS0I30	0	IC	7/15		R.WS0I0	3B9
MPS120	OI	303	12/8		XSIR0A0	8H6
MPS140	OI	204	12/8		XSIR0B0	8H5
PA030	0	304	4/4	202	PA.A10	6H3
PA110	0	104	4/4	202	PA.B10	6H3

SYMBOL NO. 12 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1103	02-11	FA1024	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS0I1	3A1
R.WS11A	I	110	4/3		R.WS1I1	4A0
SA003I0	I	002	13/3		SA0AI0	2A3
			TO CONN CKT			
SA00300	0	003	TO CONN CKT		TSA0AD0	2G4
SA011I0	I	202	13/3		SA0BI0	2A1
			TO CONN CKT			
SA01100	0	102	TO CONN CKT		TSA0B00	2G3
SA103I0	I	101	TO CONN CKT		SA1AI0	2A7
SA10300	0	103	TO CONN CKT		TSA1A00	2G9
SA111I0	I	301	TO CONN CKT		SA1BI0	2A6
SA11100	0	203	TO CONN CKT		TSA1B00	2G7
SOR031		314			SORA1	3H5
SOR111		017			SDRB1	3H0
S0003I0	OI	117	11/2		S00AR0	3H8
			13/2			
			TO CONN CKT			
SD00300	OI	317	11/2		TS00AW00	3H5
			TO CONN CKT			
S001110	OI	018	13/2		SD0BR0	3H4
			TO CONN CKT			
S001100	UI	218	TO CONN CKT		TSD0BW00	3H1
SD103I0	OI	118	11/2		S01AR0	4H8
			TO CONN CKT			
S010300	OI	318	11/2		TSD1AW00	4H5
			TO CONN CKT			
S0111I0	OI	019	TO CONN CKT		S01BR0	4H4
S011100	OI	219	TO CONN CKT		TSD1BW00	4H1
SIR030	OI	105	11/3	202	SIR0.A0	8H5
SIR110	OI	004	11/2	202	SIR0.B0	8H4
			1/1,1/3			
TSSD030	0	114			SD0A0	3H6
TSS0110	0	217			SD0B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R30B	I	010	1/11		T204R30	5A3
T204R50B	I	309	1/11		T204R50	5A3
T204R60B	I	109	1/11		T204R60	6A0
T304RE0B	I	208	1/11		T304RE0	7A1
T3204L91	0	IC	7/15		T204L91	5H2
T3204R31	0	IC	7/15		T204R31	5H3
T3204R51	0	IC	7/15		T204R51	5B7
T3204R61	0	IC	7/15		T204R61	6C0
2IBT021	I	012	4/13		2TRAI1	9A5
2IBT031	0	106	4/11		2TRA1	9H5
2IBT101	I	212	4/13		2TRBI1	9A1
2IBT111	0	306	4/11		2TRB1	9H1
3T054B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054B	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 4
SYMBOL(S) 11 12

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B4CF

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PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 13

STORE ADDRESS AND BUFFER REGISTERS
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1002	02-10	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		011			COMBI0	9A1
		206			IB.B10	8H2
		211			COMAI0	9A4
OR00A	I	300	4/1		DRI0	6A4
EFETCH0A	1	311	4/1		NFETI0	5A5
ELMINT0	I	316	1/8		MINTRP0	8A5
ELNOP00B	I	013	1/8		LNOPI0	8A2
EN.S00A	I	201	4/1		REQS0I0	2A1
EN.S10A	I	001	4/3		REQS1I0	2A5
ESARPA0A	I	111	4/1		SAR.PAI0	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	005	1/13		PAD0	3A8
	I	016	1/13		F204L90	5A0
F204RC0B	1	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1
F204R60B	I	315	1/13		F204R60	6A1
F2204L91	0	IC	7/16		F204L91	5H0
F2204RC1	0	IC	7/16		F204RC1	9F7
F2204R31	0	IC	7/16		F204R31	5H6
F2204R51	0	IC	7/16		F204R51	5H0
F2204R61	0	IC	7/16		F204R61	6H1
F304RE0B	I	214	1/13		F304RE0	7A2
GB020	0T	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AI0	5A2
GB100	0T	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BI0	5A1
I.OFF00A	I	100	4/1		I.OFFI0	6A4
IB020	0	006	1/1,1/3 1/7	202	IB.A10	8H2
IC0R20	0	IC	7/16		0R0	608
ICSAR021	0	1C	7/16		SARA1	5H5
ICSAR101	0	IC	7/16		SARB1	5H4
ICS0R021	0	IC314	7/16		S0RA1	7H5
ICSDR101	0	IC017	7/16		S0RB1	7H5
ICS0020	0	IC	7/16		TS00A	4E9
ICSD100	0	IC	7/16		TS00B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB02A0	I	IC	7/16		AKAG10	9A6
IGB02B0	I	IC	7/16		AIAG10	9A6
IGB02C0	I	IC	7/16		OKAG10	9A6
IGB0200	1	IC	7/16		OIAG10	9A6
IGB021A	0	IC	7/16		GB.AD1A	5H2
IGB021B	0	1C	7/16		GB.AD1B	7E8
IGB10A0	I	IC	7/16		AKBG10	9A2
IGB10B0	I	IC	7/16		AIBG10	9A2
IGB10C0	I	1C	7/16		DKBG10	9A3
IGB1000	I	IC	7/16		OIBG10	9A3
IGB101A	0	IC	7/16		GB.B01A	5H1
IGB101B	0	IC	7/16		GB.BD1B	7E8
IRWS0I20	0	IC	7/16		R.WS010	3B9
MPS080	0I	303	12/8		XSIR0A0	8H6
MPS100	0I	204	12/8		XSIR0B0	8H5
MS090	I	205	5/13		SDBI0	3A8
PA020	0	304	4/4	202	PA.A10	6H3
PA100	0	104	4/4	202	PA.B10	6H3

SYMBOL NO. 13 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT1002	02-10	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R.WFF1A	I	302	4/1		R.WFF1	6A5
R.WS01A	I	310	4/1		R.WS0I1	3A1
R.WS11A	I	110	4/3		R.WS1I1	4A0
SA002I0	I	002	13/3 TO CONN CKT		SA0AI0	2A3
SA00200	0	003	TO CONN CKT		TSA0A00	2G4
SA010I0	I	202	13/3 TO CONN CKT		SA0BI0	2A1
SA01000	0	102	TO CONN CKT		TSA0B00	2G3
SA102I0	I	101	TO CONN CKT		SA1AI0	2A7
SA10200	0	103	TO CONN CKT		TSA1A00	2G9
SA110I0	I	301	TO CONN CKT		SA1BI0	2A6
SA11000	0	203	TO CONN CKT		TSA1B00	2G7
S0R021		314			S0RA1	3H5
S0R101		017			S0RB1	3H0
SD002I0	0I	117	11/2 13/2 TO CONN CKT		SD0AR0	3H8
SD00200	0I	317	11/2 TO CONN CKT		TSD0AW00	3H5
SD010I0	0I	018	13/2 TO CONN CKT		SD0BR0	3H4
SD01000	0I	218	TO CONN CKT		TSD0BW00	3H1
SD102I0	0I	118	11/2 TO CONN CKT		SD1AR0	4H8
SD10200	0I	318	11/2 TO CONN CKT		TSD1AW00	4H5
SD110I0	0I	019	TO CONN CKT		SD1BR0	4H4
SD11000	0I	219	TO CONN CKT		TSD1BW00	4H1
SIR020	0I	105	11/3	202	SIR0.A0	8H5
SIR100	0I	004	11/2 1/1,1/3	202	SIR0.B0	8H4
TSSD020	0	114			SD0A0	3H6
TSSD100	0	217			SD0B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R30B	I	010	1/11		T204R30	5A3
T204R50B	1	309	1/11		T204R50	5A3
T204R60B	I	109	1/11		T204R60	6A0
T2204L91	0	IC	7/16		T204L91	5H2
T2204R31	0	IC	7/16		T204R31	5H3
T2204R51	0	IC	7/16		T204R51	5B7
T2204R61	0	IC	7/16		T204R61	6C0
T304RE0B	I	208	1/11		T304RE0	7A1
21BT011	I	012	4/14		2TRA11	9A5
21BT021	0	106	4/12		2TRA1	9H5
21BT091	1	212	4/14		2TRBI1	9A1
21BT101	0	306	4/12		2TRB1	9H1
3T054B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054B	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 14

STORE ADDRESS AND BUFFER REGISTERS
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT0901	02-09	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		011			COMBI0	9AI
		206			IB.B10	8H2
		211			COMAI0	9A4
DAT.MT1	I	205	7/11		SDBI0	3A8
OR00A	I	300	4/1		ORI0	6A4
EFETCH0A	I	311	4/1		NFETI0	5A5
ELMINT0	I	316	1/8		MINTRP0	8A5
ELNOP00B	I	013	1/8		LNOPI0	8A2
EN.S00A	I	201	4/1		REQS0I0	2A1
EN.S10A	I	001	4/3		REQS1I0	2A5
ESARPA0A	I	111	4/1		SAR.PAI0	6A2
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A4
F1204L91	0	IC	7/17		F204L91	5H0
F1204RC1	0	IC	7/17		F204RC1	9F7
F1204R31	0	IC	7/17		F204R31	5H6
F1204R51	0	1C	7/17		F204R51	5H0
F1204R61	0	IC	7/17		F204R61	6H1
F204LC0A	I	005	1/13		PAD0	3A8
	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC0B	I	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1
F204R60B	I	315	1/13		F204R60	6A1
F304RE0B	I	214	1/13		F304RE0	7A2
GB010	0T	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AI0	5A2
GB090	0T	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BI0	5A1
I.OFF00A	I	100	4/1		I.OFFI0	6A4
IB010	0	006	1/1,1/3 1/7	202	IB.A10	8H2
IC0R10	0	IC	7/17		DR0	6D8
ICSAR011	0	IC	7/17		SARA1	5H5
ICSAR091	0	IC	7/17		SARB1	5H4
ICSDR011	0	IC314	7/17		SDRA1	7H5
ICS0R091	0	IC017	7/17		S0RB1	7H5
ICSD010	0	IC	7/17		TSD0A	4E9
ICS0090	0	IC	7/17		TSD0B	4H4
IFF01	I	210	1/5		IFF1	8A4
IGB01A0	I	IC	7/17		AKAG10	9A6
IGB01B0	I	IC	7/17		AIAG10	9A6
IGB01C0	I	1C	7/17		DKAG10	9A6
IGB01D0	I	IC	7/17		OIAG10	9A6
IGB011A	0	IC	7/17		GB.AD1A	5H2
IGB011B	0	IC	7/17		GB.A01B	7E8
IGB09A0	I	IC	7/17		AKBG10	9A2
IGB09B0	I	1C	7/17		AIBG10	9A2
IGB09C0	I	IC	7/17		OKBG10	9A3
IGB09D0	I	IC	7/17		OIBG10	9A3
IGB091A	0	IC	7/17		GB.B01A	5H1
IGB091B	0	IC	7/17		GB.B01B	7E8
IRWS0I10	0	IC	7/17		R.WS0I0	3B9
MPS040	0I	303	12/8		XSIR0AC	8H6
MPS060	0I	204	12/8		XSIR0B0	8H5
PA010	0	304	4/4	202	PA.A10	6H3
PA090	0	104	4/4	202	PA.B10	6H3

SYMBOL NO. 14 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT0901	02-09	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R.WFF1A	I	302	4/1		R.WFFI	6A5
R.WS01A	I	310	4/1		R.WS0I1	3A1
R.WS11A	I	110	4/3		R.WS1I1	4A0
SA001I0	I	002	13/3 TO CONN CKT		SA0AI0	2A3
SA00100	0	003	TO CONN CKT		TSA0AD0	2G4
SA009I0	I	202	13/3 TO CONN CKT		SA0BI0	2A1
SA00900	0	102	TO CONN CKT		TSA0B00	2G3
SA101I0	I	101	TO CONN CKT		SA1AI0	2A7
SA101D0	0	103	TO CONN CKT		TSA1AD0	2G9
SA109I0	I	301	TO CONN CKT		SA1BI0	2A6
SA10900	0	203	TO CONN CKT		TSA1B00	2G7
S0R011		314			S0RA1	3H5
S0R091		017			S0RB1	3H0
SD001I0	0I	117	11/3 13/2 TO CONN CKT		SD0AR0	3H8
SD00100	0I	317	11/3 TO CONN CKT		TSD0AW00	3H5
SD009I0	0I	018	13/2 TO CONN CKT		S00BR0	3H4
SD00900	0I	218	TO CONN CKT		TS00BW00	3H1
SD101I0	0I	118	11/3 TO CONN CKT		SD1AR0	4H8
SD10100	0I	318	11/3 TO CONN CKT		TSD1AW00	4H5
SD109I0	0I	019	TO CONN CKT		SD1BR0	4H4
SD10900	0I	219	TO CONN CKT		TSD1BW00	4H1
SIR010	0I	105	11/3	202	SIR0.A0	8H5
SIR090	0I	004	11/2 1/1,1/3	202	SIR0.B0	8H4
TSSD010	0	114			SD0A0	3H6
TSSD090	0	217			SD0B0	3H1
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T1204L91	0	1C	7/17		T204L91	5H2
T1204R31	0	IC	7/17		T204R31	5H3
T1204R51	0	IC	7/17		T204R51	5B7
T1204R61	0	IC	7/17		T204R61	6C0
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2
T204R30B	I	010	1/11		T204R30	5A3
T204R50B	I	309	1/11		T204R50	5A3
T204R60B	I	109	1/11		T204R60	6A0
T304RE0B	I	208	1/11		T304RE0	7A1
21BT001	I	012	4/15		2TRAI1	9A5
21BT011	0	106	4/13		2TRA1	9H5
21BT081	I	212	4/15		2TRBI1	9A1
21BT091	0	306	4/13		2TRB1	9H1
3T054B	GRD	0GD		203	GRD	

PART OF FS 4
SYMBOL(S) 13 14

3A CENTRAL CONTROL

	DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	B4CG

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12/01/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

SYMBOL NO. 14 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT0901	02-09	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T054B	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054B	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 15

STORE ADDRESS AND BUFFER REGISTERS
(BITS 08 AND 00)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT0800	02-08	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		011			COMBI0	9A1
		206			IB.B10	8H2
		211			COMAI0	9A4
ADR.MT1	I	205	7/9		SOBI0	3A8
OR00A	I	300	4/1		ORI0	6A4
EFETCH0A	I	311	4/1		NFETI0	5A5
ELMINT0	I	316	1/8		MINTRP0	8A5
ELNOP00B	I	013	1/8		LNOPI0	8A2
EN.S00A	I	201	4/1		REOS0I0	2A1
EN.S10A	I	001	4/3		REOS1I0	2A5
ESARPA0A	I	111	4/1		SAR.PAI0	6A2
F0204L91	0	IC	7/18		F204L91	5H0
F0204RC1	0	IC	7/18		F204RC1	9F7
F0204R31	0	IC	7/18		F204R31	5H6
F0204R51	0	IC	7/18		F204R51	5H0
F0204R61	0	IC	7/18		F204R61	6H1
F104L10A	I	014	1/13		F104L10	7A0
F104L20A	I	313	1/13		F104L20	7A6
F204LA0A	I	005	1/13		PAD0	3A8
F204LC0A	I	116	1/13		F204LC0	8A1
F204L90A	I	016	1/13		F204L90	5A0
F204RC0B	I	113	1/13		F204RC0	9A2
F204R30B	I	213	1/13		F204R30	5A7
F204R50B	I	115	1/13		F204R50	5A1
F204R60B	I	315	1/13		F204R60	6A1
F304RE0B	I	214	1/13		F304RE0	7A2
GB000	OT	007	2/4		GB.AS10	9H6
	I	112	2/4		GB.AI0	5A2
GB080	OT	207	2/3		GB.BS10	9H3
	I	312	2/3		GB.BI0	5A1
I.OFF00A	I	100	4/1		I.OFFI0	6A4
IB000	0	006	1/3,1/7	202	IB.A10	8H2
ICOR00	0	IC	7/18		OR0	6D8
ICSAR001	0	IC	7/18		SARA1	5H5
ICSAR081	0	IC	7/18		SARB1	5H4
ICSDR001	0	IC314	7/18		SDRA1	7H5
ICSOR081	0	IC017	7/18		SORB1	7H5
ICSD000	0	IC	7/18		TS00A	4E9
ICS0080	0	IC	7/18		TS00B	4H4

SYMBOL NO. 15 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 08 AND 00)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT0800	02-08	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IFF01	I	210	1/5		IFF1	8A4
IGB00A0	I	IC	7/18		AKAG10	9A6
IGB00B0	I	IC	7/18		AIAG10	9A6
IGB00C0	I	IC	7/18		OKAG10	9A6
IGB00D0	I	IC	7/18		DIAG10	9A6
IGB001A	0	IC	7/18		GB.AD1A	5H2
IGB001B	0	IC	7/18		GB.AD1B	7E8
IGB08A0	I	IC	7/18		AKBG10	9A2
IGB08B0	I	IC	7/18		AIBG10	9A2
IGB08C0	I	IC	7/18		OKBG10	9A3
IGB0800	I	IC	7/18		OIBG10	9A3
IGB081A	0	IC	7/18		GB.B01A	5H1
IGB081B	0	IC	7/18		GB.B01B	7E8
IRWS0I00	0	IC	7/18		R.WS0I0	3B9
MPS000	0I	303	12/8		XSIR0A0	8H6
MPS020	0I	204	12/8		XSIR0B0	8H5
PA000	0	304	4/4	202	PA.A10	6H3
PA080	0	104	4/4	202	PA.B10	6H3
R.WFF1A	I	302	4/1		R.WFFI	6A5
R.WS01A	I	310	4/1		R.WS0I1	3A1
R.WS11A	I	110	4/3		R.WS1I1	4A0
SA000I0	I	002	13/3 TO CONN CKT		SAGAI0	2A3
SA00000	0	003	TO CONN CKT		TSA0A00	2G4
SA008I0	I	202	13/3 TO CONN CKT		SA0BI0	2A1
SA00800	0	102	TO CONN CKT		TSA0B0C	2G3
SA100I0	I	101	TO CONN CKT		SA1AI0	2A7
SA10000	0	103	TO CONN CKT		TSA1A00	2G9
SA108I0	I	301	TO CONN CKT		SA1BI0	2A6
SA10800	0	203	TO CONN CKT		TSA1B00	2G7
SDR001		314			SORA1	3H5
SOR081		017			SORB1	3H0
S000010	0I	117	11/3 13/2 TO CONN CKT		S00AR0	3H8
SD00000	0I	317	11/3 TO CONN CKT		TSD0AW00	3H5
S000810	0I	018	13/2 TO CONN CKT		S00BR0	3H4
SD00800	0I	218	TO CONN CKT		TS00BW00	3H1
S01001O	0I	118	11/3 TO CONN CKT		S01AR0	4H8
SD10000	0I	318	11/3 TO CONN CKT		TSD1AW00	4H5
SD108I0	0I	019	TO CONN CKT		S01BR0	4H4
S010800	0I	219	TO CONN CKT		TSD1BW00	4H1
SIR000	0I	105	11/3	202	SIR0.A0	8H5
SIR080	0I	004	11/2 1/1,1/3	202	SIR0.B0	8H4
TSS0000	0	114			SD0A0	3H6
TSS0080	0	217			SD0B0	3H1
T0204L91	0	IC	7/18		T204L91	5H2
T0204R31	0	IC	7/18		T204R31	5H3
T0204R51	0	IC	7/18		T204R51	5B7
T0204R61	0	IC	7/18		T204R61	6C0
T104L10A	I	215	1/11		T104L10	7A1
T104L20A	I	015	1/11		T104L20	7A5
T204LC0A	I	108	1/11		T204LC0	5A4
T204L90A	I	009	1/11		T204L90	5A2

SYMBOL NO. 15 (CONT)

STORE ADDRESS AND BUFFER REGISTERS
(BITS 08 AND 00)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT0800	02-08	FA1024	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T204R30B	I	010	1/11		T204R30	5A3
T204R50B	I	309	1/11		T204R50	5A3
T204R60B	I	109	1/11		T204R60	6A0
T304RE0B	I	208	1/11		T304RE0	7A1
2IBT001	0	106	4/14		2TRA1	9H5
2IBT071	I	212	4/8		2TRBI1	9A1
2IBT081	0	306	4/14		2TRB1	9H1
3T054B	GRD	0G0		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0208T	I	012			2TRAI1	9A5
	GRD	319			GRD	
3V054B	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 4
SYMBOL(S) 14 15

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	B4CH

PRINTED IN U. S. A.

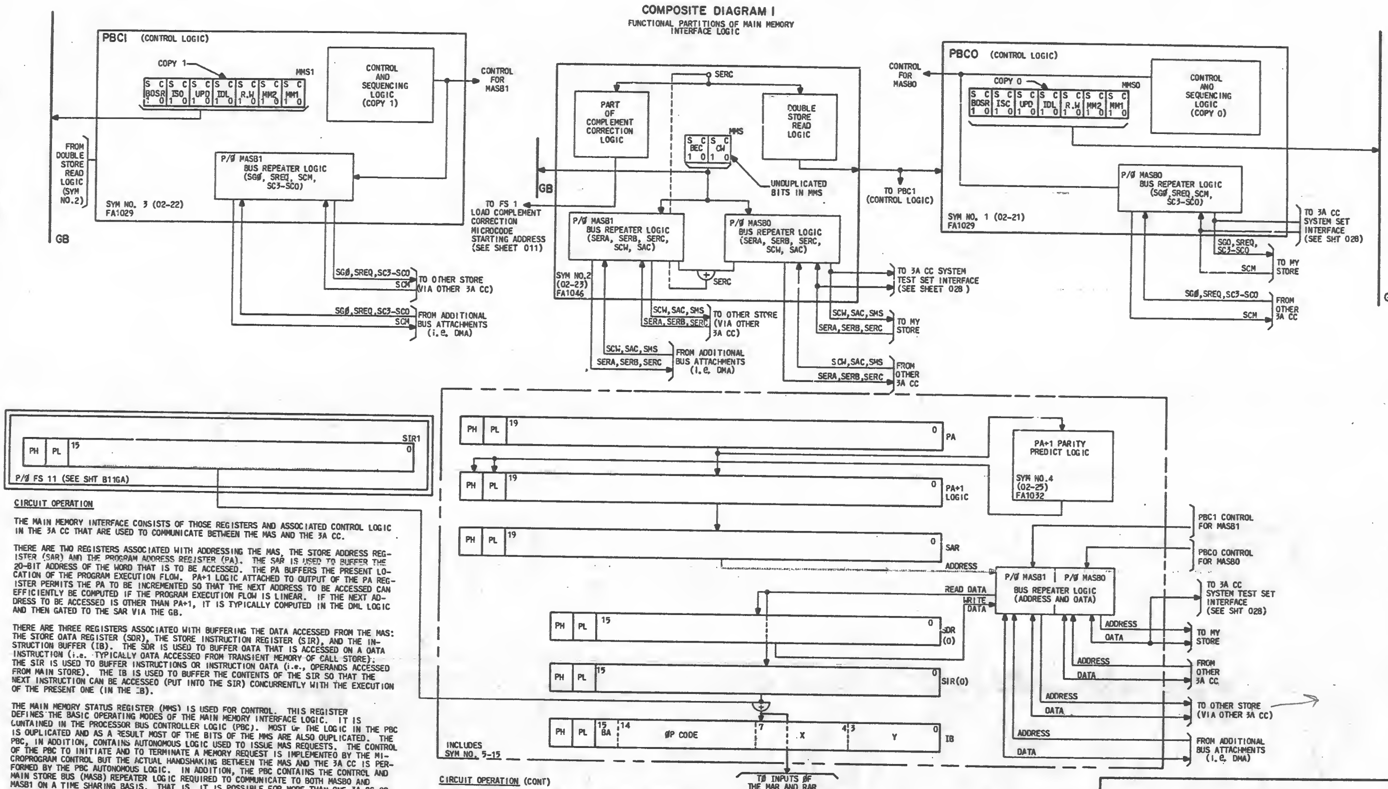
12/01/77

PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM I

FUNCTIONAL PARTITIONS OF MAIN MEMORY INTERFACE LOGIC



PBCI (CONTROL LOGIC)
COPY 1
MMS1
S C BOSR 1 0
S C ISO 1 0
S C UPD 1 0
S C IDL 1 0
S C R.W 1 0
S C MM2 1 0
S C MM1 1 0
CONTROL AND SEQUENCING LOGIC (COPY 1)
CONTROL FOR MASB1
FROM DOUBLE STORE READ LOGIC (SYM NO.2)
P/Ø MASB1 BUS REPEATER LOGIC (SGØ, SREQ, SCM, SC3-SCO)
SYM NO. 3 (02-22) FA1029
GB
SGØ,SREQ,SC3-SCO
SCM
TO OTHER STORE (VIA OTHER 3A CC)
FROM ADDITIONAL BUS ATTACHMENTS (i.e. DMA)
SERC
PART OF COMPLEMENT CORRECTION LOGIC
DOUBLE STORE READ LOGIC
MMS
S C BEC 1 0
S C CW 1 0
UNDUPLICATED BITS IN MMS
TO FS 1 LOAD COMPLEMENT CORRECTION MICROCODE STARTING ADDRESS (SEE SHEET 011)
P/Ø MASB1 BUS REPEATER LOGIC (SERA, SERB, SERC, SCW, SAC)
P/Ø MASBO BUS REPEATER LOGIC (SERA, SERB, SERC, SCW, SAC)
SYM NO.2 (02-23) FA1046
TO PBC1 (CONTROL LOGIC)
TO 3A CC SYSTEM TEST SET INTERFACE (SEE SHEET 028)
SCW,SAC,SMS
SERA,SERB,SERC
TO OTHER STORE (VIA OTHER 3A CC)
TO MY STORE
FROM ADDITIONAL BUS ATTACHMENTS (i.e. DMA)
FROM OTHER 3A CC
CONTROL FOR MASBO
PBCO (CONTROL LOGIC)
COPY 0
MMSO
CONTROL AND SEQUENCING LOGIC (COPY 0)
P/Ø MASBO BUS REPEATER LOGIC (SGØ, SREQ, SCM, SC3-SCO)
SYM NO. 1 (02-21) FA1029
TO 3A CC SYSTEM SET INTERFACE (SEE SHT 028)
SGO, SREQ, SC3-SCO
SCM
TO MY STORE
FROM OTHER 3A CC
PH PL 15 SIR1 0
P/Ø FS 11 (SEE SHT B11GA)
PH PL 19 0 PA
PA+1 PARITY PREDICT LOGIC
SYM NO.4 (02-25) FA1032
PH PL 19 0 PA+1 LOGIC
PH PL 19 0 SAR
ADDRESS
READ DATA
WRITE DATA
P/Ø MASB1 P/Ø MASBO BUS REPEATER LOGIC (ADDRESS AND DATA)
PBC1 CONTROL FOR MASB1
PBCO CONTROL FOR MASBO
TO 3A CC SYSTEM TEST SET INTERFACE (SEE SHT 028)
ADDRESS
DATA
TO MY STORE
FROM OTHER 3A CC
TO OTHER STORE (VIA OTHER 3A CC)
FROM ADDITIONAL BUS ATTACHMENTS (i.e. DMA)
PH PL 15 0 SDR (0)
PH PL 15 0 SIR(0)
PH PL 15 BA 14 ØP CODE 7 X 4 3 Y 0 IB
INCLUDES SYM NO. 5-15
TO INPUTS OF THE MAR AND RAR SEE SHT. B1GA

CIRCUIT OPERATION

THE MAIN MEMORY INTERFACE CONSISTS OF THOSE REGISTERS AND ASSOCIATED CONTROL LOGIC IN THE 3A CC THAT ARE USED TO COMMUNICATE BETWEEN THE MAS AND THE 3A CC.

THERE ARE TWO REGISTERS ASSOCIATED WITH ADDRESSING THE MAS, THE STORE ADDRESS REGISTER (SAR) AND THE PROGRAM ADDRESS REGISTER (PA). THE SAR IS USED TO BUFFER THE 20-BIT ADDRESS OF THE WORD THAT IS TO BE ACCESSED. THE PA BUFFERS THE PRESENT LOCATION OF THE PROGRAM EXECUTION FLOW. PA+1 LOGIC ATTACHED TO OUTPUT OF THE PA REGISTER PERMITS THE PA TO BE INCREMENTED SO THAT THE NEXT ADDRESS TO BE ACCESSED CAN EFFICIENTLY BE COMPUTED IF THE PROGRAM EXECUTION FLOW IS LINEAR. IF THE NEXT ADDRESS TO BE ACCESSED IS OTHER THAN PA+1, IT IS TYPICALLY COMPUTED IN THE DML LOGIC AND THEN GATED TO THE SAR VIA THE GB.

THERE ARE THREE REGISTERS ASSOCIATED WITH BUFFERING THE DATA ACCESSED FROM THE MAS: THE STORE DATA REGISTER (SDR), THE STORE INSTRUCTION REGISTER (SIR), AND THE INSTRUCTION BUFFER (IB). THE SDR IS USED TO BUFFER DATA THAT IS ACCESSED ON A DATA INSTRUCTION (i.e. TYPICALLY DATA ACCESSED FROM TRANSIENT MEMORY OF CALL STORE); THE SIR IS USED TO BUFFER INSTRUCTIONS OR INSTRUCTION DATA (i.e., OPERANDS ACCESSED FROM MAIN STORE). THE IB IS USED TO BUFFER THE CONTENTS OF THE SIR SO THAT THE NEXT INSTRUCTION CAN BE ACCESSED (PUT INTO THE SIR) CONCURRENTLY WITH THE EXECUTION OF THE PRESENT ONE (IN THE IB).

THE MAIN MEMORY STATUS REGISTER (MMS) IS USED FOR CONTROL. THIS REGISTER DEFINES THE BASIC OPERATING MODES OF THE MAIN MEMORY INTERFACE LOGIC. IT IS CONTAINED IN THE PROCESSOR BUS CONTROLLER LOGIC (PBC). MOST OF THE LOGIC IN THE PBC IS DUPLICATED AND AS A RESULT MOST OF THE BITS OF THE MMS ARE ALSO DUPLICATED. THE PBC, IN ADDITION, CONTAINS AUTONOMOUS LOGIC USED TO ISSUE MAS REQUESTS. THE CONTROL OF THE PBC TO INITIATE AND TO TERMINATE A MEMORY REQUEST IS IMPLEMENTED BY THE MICROPROGRAM CONTROL BUT THE ACTUAL HANDSHAKING BETWEEN THE MAS AND THE 3A CC IS PERFORMED BY THE PBC AUTONOMOUS LOGIC. IN ADDITION, THE PBC CONTAINS THE CONTROL AND MAIN STORE BUS (MASB) REPEATER LOGIC REQUIRED TO COMMUNICATE TO BOTH MASBO AND MASB1 ON A TIME SHARING BASIS. THAT IS, IT IS POSSIBLE FOR MORE THAN ONE 3A CC OR ADDITIONAL MASB ATTACHMENT TO ACCESS THE MAS SIMULTANEOUSLY. IN THIS CASE, MEMORY REQUESTS ARE INTERLEAVED ON THE MASB AND CONTROL LOGIC IN THE PBC PERFORMS THIS FUNCTION.

THE MAIN MEMORY INTERFACE LOGIC ALSO CONTAINS ALL THE LOGIC NECESSARY TO PROVIDE THE AUTOMATIC REREAD OF THE OFF-LINE STORE IN THE EVENT A READ PARITY IS INDICATED BY THE MAIN STORE. THE REREAD OPERATION IS REFERRED TO AS THE DOUBLE STORE READ (DSR) AND IS PERFORMED WHEN THE 3A CC SYSTEM IS IN DUPLEX MODE. IN ADDITION, THE LOGIC NECESSARY TO INITIATE THE AUTOMATIC ERROR RECOVERY TECHNIQUE, CALLED COMPLEMENT CORRECTION BY A SPECIAL MICROCODED SUBROUTINE, IS ALSO CONTAINED IN FS 4. THE AUTOMATIC CORRECTION TECHNIQUE IS INVOKED WHEN THE SYSTEM IS IN SIMPLEX AND A READ PARITY ERROR IS INDICATED BY THE MAIN STORE.

CIRCUIT OPERATION (CONT)

PART OF FS 4
COMPOSITE DIAGRAM 1

3A CENTRAL CONTROL ②

DWG SIZE 65

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4GA

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PART OF FS 4

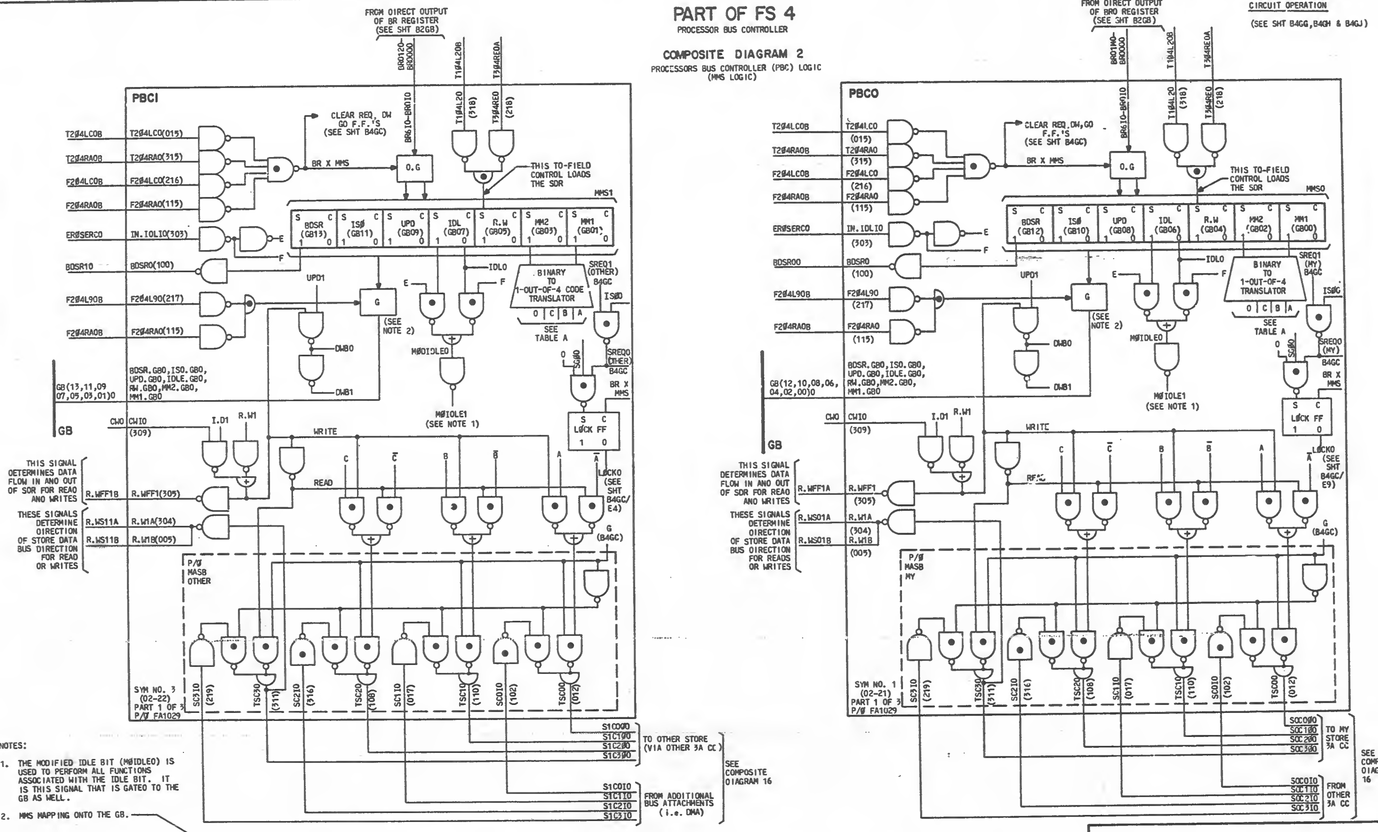
PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 2

PROCESSORS BUS CONTROLLER (PBC) LOGIC
(MMS LOGIC)

CIRCUIT OPERATION

(SEE SHT B4GG, B4GH & B4GJ)



FROM DIRECT OUTPUT OF BR REGISTER (SEE SHT B2GB)
BR0120-BR0000
T1Ø4L20B
T3Ø4REOA
PBCI
T2Ø4LC0B
T2Ø4RAOB
F2Ø4LC0B
F2Ø4RAOB
ERØSERCO
BDSR10
F2Ø4L90B
T2Ø4LCO(015)
T2Ø4RAO(315)
F2Ø4LCO(216)
F2Ø4RAO(115)
IN.IOLIO(303)
BDSRO(100)
F2Ø4L90(217)
CLEAR REQ, DW GO F.F.'S (SEE SHT B4GC)
BR X MMS
BR610-BR010
O.G
T1Ø4L20 (318)
T3Ø4REO (218)
THIS TO-FIELD CONTROL LOADS THE SDR
MMS1
BDSR (GB13)
ISØ (GB11)
UPD (GB09)
IDL (GB07)
R.W (GB05)
MM2 (GB03)
MM1 (GB01)
BINARY TO 1-OUT-OF-4 CODE TRANSLATOR
SEE TABLE A
SREQ1 (OTHER) B4GC
SREQO (OTHER) B4GC
LØCK FF
LØCKO (SEE SHT B4GC/E4)
UPD1
DWBO
DWB1
MØDIDLEO
MØIDLE1 (SEE NOTE 1)
(SEE NOTE 2)
IDLO
GB(13,11,09 07,05,03,01)0
GB
BDSR.GB0, ISO.GB0, UPD.GB0, IDLE.GB0, RW.GB0, MM2.GB0, MM1.GB0
CWO CWIO (309)
I.D1
R.W1
WRITE
READ
THIS SIGNAL DETERMINES DATA FLOW IN AND OUT OF SDR FOR READ AND WRITES
R.WFF1B R.WFF1(305)
THESE SIGNALS DETERMINE DIRECTION OF STORE DATA BUS DIRECTION FOR READ OR WRITES
R.WS11A R.W1A(304)
R.WS11B R.W1B(005)
P/Ø MASB OTHER
SYM NO. 3 (02-22) PART 1 OF 3 P/Ø FA1029
SC310 (219) TSC30 (311) SC210 (316) TSC20 (108) SC110 (017) TSC10 (110) SC010 (102) TSC00 (012)
S1C0Ø0 S1C1Ø0 S1C2Ø0 S1C3Ø0
TO OTHER STORE (VIA OTHER 3A CC)
S1C010 S1C110 S1C210 S1C310
FROM ADDITIONAL BUS ATTACHMENTS (i.e. DMA)
SEE COMPOSITE DIAGRAM 16
FROM DIRECT OUTPUT OF BRO REGISTER (SEE SHT B2GB)
BR01NO-BR0000
PBCO
T2Ø4LCO (015)
T2Ø4RAO (315)
F2Ø4LCO (216)
F2Ø4RAO (115)
IN.IDLIO (303)
BDSRO (100)
F2Ø4L90 (217)
MMSO
BDSR (GB12)
ISØ (GB10)
UPD (GB08)
IDL (GB06)
R.W (GB04)
MM2 (GB02)
MM1 (GB00)
SREQ1 (MY) B4GC
SREQO (MY) B4GC
BR X MMS
GB(12,10,08,06, 04,02,00)0
R.WFF1A R.WFF1 (305)
R.WS01A R.W1A (304)
R.WS01B R.W1B (005)
THESE SIGNALS DETERMINE DIRECTION OF STORE DATA BUS DIRECTION FOR READS OR WRITES
P/Ø MASB MY
SYM NO. 1 (02-21) PART 1 OF 3 P/Ø FA1029
SC310 (219) TSC30 (311) SC210 (316) TSC20 (108) SC110 (017) TSC10 (110) SC010 (102) TSC00 (012)
SOC0Ø0 SOC1Ø0 SOC2Ø0 SOC3Ø0
TO MY STORE 3A CC
SOC010 SOC110 SOC210 SOC310
FROM OTHER 3A CC
G (B4GC)

NOTES:

1. THE MODIFIED IDLE BIT (MØIDLEO) IS USED TO PERFORM ALL FUNCTIONS ASSOCIATED WITH THE IDLE BIT. IT IS THIS SIGNAL THAT IS GATED TO THE GB AS WELL.
2. MMS MAPPING ONTO THE GB.

15																	0
PH (1)	PL (0)	* BEC 0	* CW 0	BDSR 1	BDSR 0	1SØ 1	1SØ 0	UPD 1	UPD 0	IDL 1	IDL 0	R.W 1	R.W 0	MM2 1	MM2 0	MM1 1	MM1 0

* CWO GATED TO BITS 14 & 16 OF GB
BECO GATED TO BITS 15 & 17 OF GB
TO MAINTAIN GOOD PARITY

PART OF FS 4
COMPOSITE DIAGRAM 2

3A CENTRAL CONTROL

②

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4GB

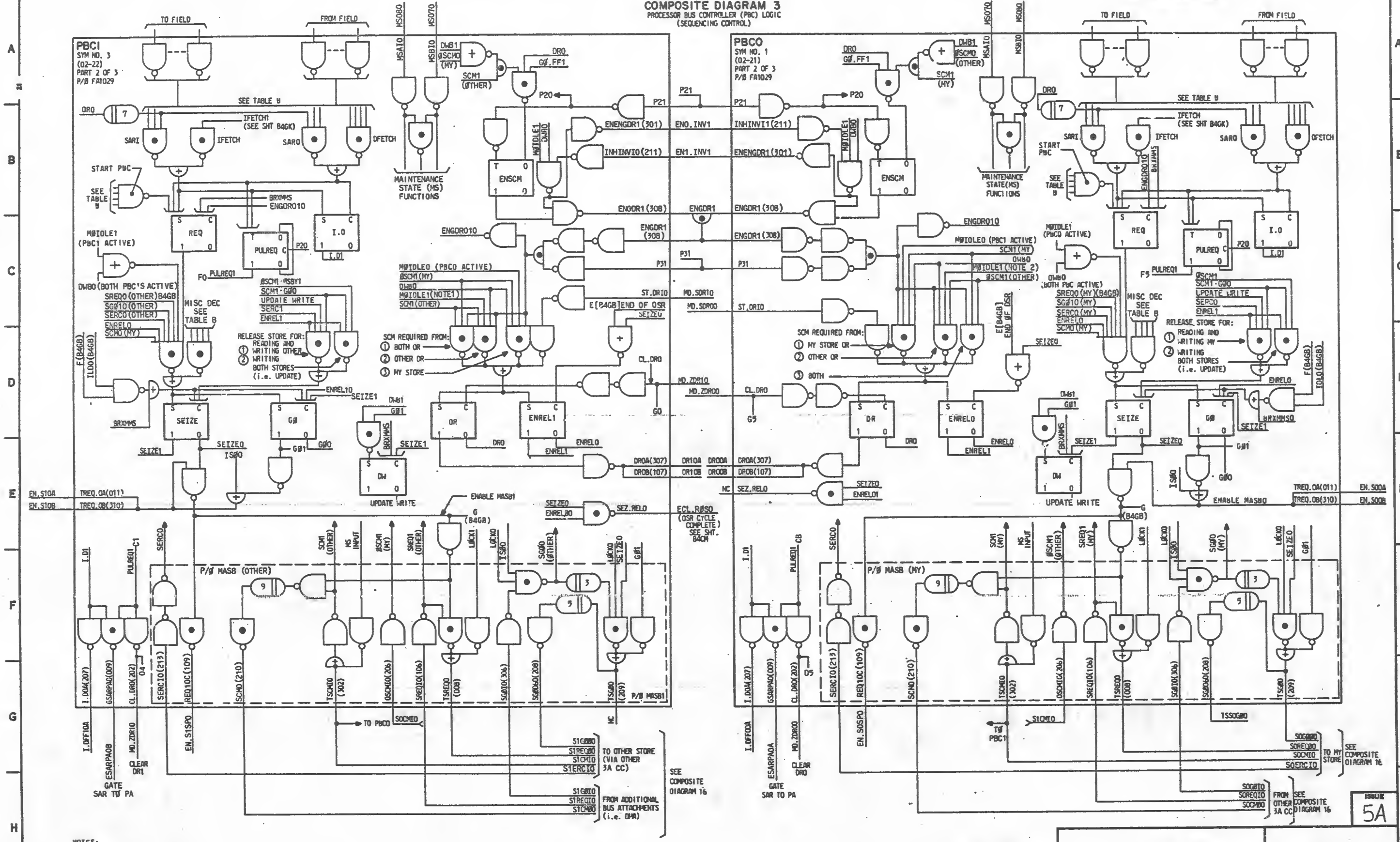
PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 3

PROCESSOR BUS CONTROLLER (PBC) LOGIC
(SEQUENCING CONTROL)

CIRCUIT OPERATION
(SEE SHEET B4GG, B4GH & B4GJ)



NOTES:

1. PBC1 ACTIVE
2. PBC0 ACTIVE

PART OF FS 4
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL

SD-1C900-01-B4GC

ISSUE 5A

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

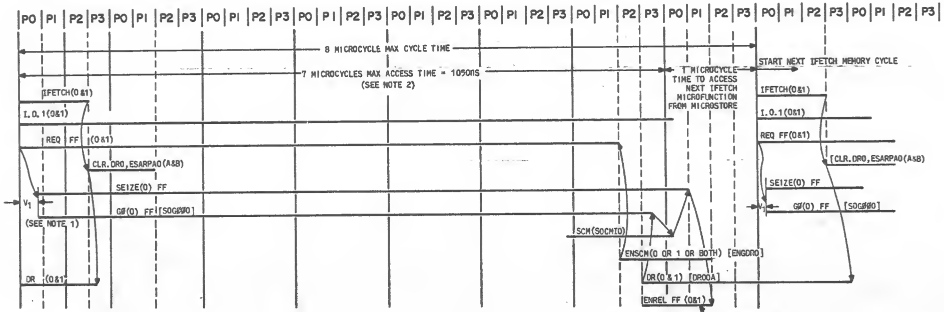
PART OF FS 4

PROCESSOR BUS CONTROLLER

CIRCUIT OPERATION
(SEE SHEETS B4GG, B4GH AND B4GJ)

COMPOSITE DIAGRAM 4

BASIC TIMING IN THE PBC ON AN INSTRUCTION (IFETCH)
MICROCONTROL COMMAND ISSUED BY THE 3A CC TO FETCH ON INSTRUCTION
FROM ITS ASSOCIATED (i.e. MY) MAIN STORE


P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3
8 MICROCYCLE MAX CYCLE TIME
7 MICROCYCLES MAX ACCESS TIME = 1050ns (SEE NOTE 2)
1 MICROCYCLE TIME TO ACCESS NEXT IFETCH MICROFUNCTION FROM MICROSTORE
START NEXT IFETCH MEMORY CYCLE
IFETCH(0&1)
I.O.1(0&1)
REQ FF (0&1)
CLR.DR0, ESARPA0(A&B)
SEIZE(0) FF
G0(0) FF [SOG000]
V_1
(SEE NOTE 1)
DR (0&1)
SCM(SOCMIO)
ENSCM(0 OR 1 OR BOTH) [ENGDR0]
DR(0 & 1) [DR00A]
ENREL FF (0&1)
IFETCH(0&1)
I.O.1(0&1)
REQ FF(0&1)
[CLR.DR0, ESARPA0(A&B)
SEIZE(0) FF
V_1
G0(0) FF [SOG000]

ANOTHER MAS CYCLE CANNOT BEGIN UNTIL THIS FLIP-FLOP IS RESET. (I.e. THIS FLIP-FLOP WILL INHIBIT THE SETTING OF THE SEIZE FF AND G0 FF WHEN ACTIVE.)

NOTES:

1. V - REPRESENTS A VARIABLE AMOUNT OF TIME.
   V_1 - TYPICALLY V_1 IS A FEW GATE DELAYS 10-30ns BUT IF ANOTHER USER IS OCCUPYING THE BUS V_1 TYPICALLY IS ABOUT 1 MEMORY CYCLE $\approx 1.2\mu S$

   0&1 / A&B } INDICATE WHICH PBC THESE SIGNALS COME FROM– 0 FOR PBC0 AND 1 FOR PBC1.

2. IT IS POSSIBLE FOR THE ACCESS TIME TO BE 6 MICROCYCLES IF GATE DELAYS ARE NOT WORST CASE (MAX) AND THE 3A CC AND MASC CLOCK HAPPEN TO BE SYNCHRONIZED.

PART OF FS 4
COMPOSITE DIAGRAM 4

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B4GD

E - 7021 (12 - 73)

PRINTED IN U.S.A.

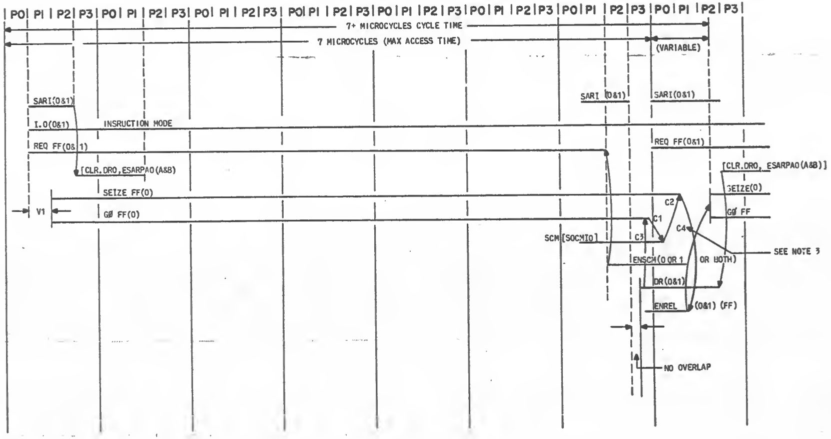
CIRCUIT OPERATION
(SEE SHEETS B4GG, B4GH AND B4GJ)

PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 5

BASIC TIMING IN THE PBC FOR A SARI MICROCONTROL COMMAND ISSUED BY THE 3A CC TO FETCH AN INSTRUCTION FROM THE ASSOCIATED (i.e. MY) MAIN STORE (SEE NOTE 1)



NOTES:

1. A SARD AND DFETCH HAVE THE IDENTICAL TIMING CHARACTERISTICS AS A SARI AND THE ONLY DIFFERENT FUNCTION THEY PERFORM IS TO CLEAR THE I.0 FF INSTEAD OF SETTING IT.

2. THE SARI CAN BE GIVEN REPEATEDLY BY THE MICROCONTROL BUT IT CAN ONLY INITIATE A MAS CYCLE WHEN THE DR=1.

3. CHANGE OF STATES C_1,C_2 AND C_3,C_4 COULD TAKE A VARIABLE LENGTH OF TIME MAINLY DEPENDENT UPON GATE DELAYS AND MAIN STORE BUS DELAYS. NOTE THAT C_1,C_2 AND C_3,C_4 MUST TAKE PLACE BEFORE THE SEIZE FF IS RESET. THEN THE ENREL FF CAN BE RESET AND THE NEW MAS CYCLE CAN BEGIN.

PART OF FS 4
COMPOSITE DIAGRAM 5

3A CENTRAL CONTROL ②

DWG SIZE 6S
ISSUE 5A

BELL LABORATORIES
SD-1C900-01
B4GE

E-7821 (12-73)
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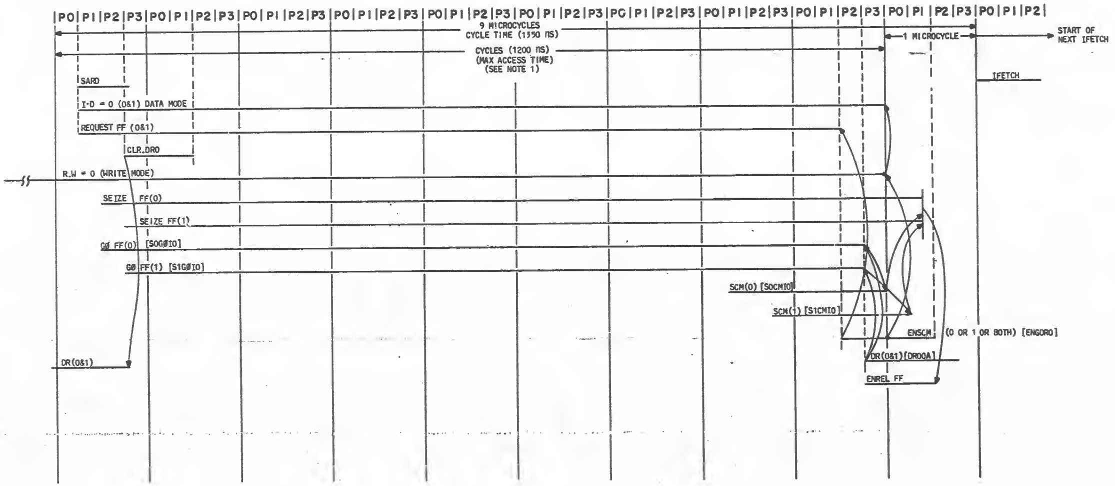
PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 6

BASIC TIMING IN THE PBC FOR A SARD MICROCONTROL COMMAND ISSUED BY THE 3A CC
TO ISSUE A WRITE COMMAND WHEN IN THE UPDATE MODE

CIRCUIT OPERATION
(SEE SHEETS B4GG, B4GH, AND B4GJ)



NOTES:

1. THIS TIME IS ONE MICROCYCLE LONGER THAN THE NORMAL CYCLE BECAUSE OF THE ADDED DELAY IN GOING THROUGH THE BUS REPEATERS TO THE OTHER STORE. IT MAY ALSO BE ONE MICROCYCLE SHORTER AS DESCRIBED IN NOTE 2 OF SHEET B4GD.

PART OF FS 4
COMPOSITE DIAGRAM 6

3A CENTRAL CONTROL ②

DWG SIZE
5S

ISSUE
5A

BELL LABORATORIES

SD-1C900-01

B4GF

PART OF FS 4

PROCESSOR BUS CONTROLLER

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2-6

CIRCUIT OPERATION

GENERAL OPERATION OF PBC

THE PBC IS A SEMIAUTONOMOUS UNIT RELATIVE TO THE 3A CC. THE STATIC MODES OF PBC OPERATION (i.e. UPDATE MODE, READ, OR WRITE) ARE DEFINED BY A CONTROL REGISTER CONTAINED WITHIN IT (THE MAIN MEMORY STATUS [MMS] REGISTER). THE MMS REGISTER IS LOADED UNDER MICROPROGRAM CONTROL AND NORMALLY REMAINS UNCHANGED FROM ONE MAS REQUEST TO ANOTHER. THE MICROPROGRAM CONTROL, HAVING LOADED A 20-BIT ADDRESS AND A DATA CONSTANT (IF A WRITE), INDICATES TO THE PBC THAT A MAS REQUEST IS REQUIRED. THE PBC THEN OPERATES IN AN AUTONOMOUS MANNER TO PERFORM THAT REQUEST. SINCE THE BUS SYSTEM ALLOWS TIME SHARING OF THE MEMORY RESOURCES, THE PBC MUST BE ABLE TO ISSUE ITS MAS REQUEST UNDER THE CONDITIONS OF A BUSY OR AN IDLE BUS AND, ONCE THE BUS HAS BEEN SEIZED, THE PBC MUST PREVENT OTHER USERS FROM INTERFERING WITH ITS MEMORY CYCLE.

THE ABILITY OF THE PBC TO OPERATE IN THIS MANNER ALLOWS THE MICROPROGRAM CONTROL TO OPERATE CONCURRENTLY WITH MAS REQUESTS. AT THE COMPLETION OF A REQUEST, THE PBC SETS THE DATA READY (DR) FLIP-FLOP. THE MICROPROGRAM CONTROL, UPON TERMINATING THE SEQUENCE OF MICROINSTRUCTIONS ON WHICH IT WAS WORKING, TESTS THE DR. IF THE DR IS SET, THE MICROPROGRAM CONTROL CAN USE THE FETCHED DATA. IF THE DR IS NOT SET, THE MICROPROGRAM CONTROL WILL LOOP WHILE WAITING FOR THE DR TO BE SET. THIS LOOPING THUS ALLOWS THE 3A CC AND THE OPERATION OF ITS MAS TO BE COMPLETELY ASYNCHRONOUS.

THE PBC HAS BEEN DESIGNED TO ACCOMMODATE THE NORMAL DUPLEX OPERATION OF THE 3A CC IN THE NO. 3 ESS AND COMMON SYSTEM APPLICATIONS (16-BIT MEMORY WIDTH PLUS 2 PARITY BITS) AND THE NO. 2B ESS (24-BIT MEMORY WIDTH PLUS 2 PARITY BITS) SYSTEMS. IN ADDITION, IT HAS BEEN DESIGNED TO WORK IN A MULTIPROCESSING MODE OR A MODE WHERE ADDITIONAL ATTACHMENTS TO THE 3A CC BUS SYSTEM MAY REQUIRE TIME-SHARING THE MAS (SUCH AS REQUIRED WITH A DMA UNIT).

IN ADDITION TO THE PBC IN THE 3A CC, THERE IS A MAIN STORE CONTROLLER (MASC) THAT IS ASSOCIATED WITH EACH 256K (K=1024) WORDS OF MAS. THE 3A CC HAS THE ABILITY TO ADDRESS 1000K WORDS OF MAIN MEMORY AND HENCE, THE 3A CC CAN HAVE AS MANY AS FOUR MASC'S ASSOCIATED WITH IT. EACH MASC IS AN AUTONOMOUS UNIT RELATIVE TO THE 3A CC. IT HAS ITS OWN CLOCK, TIMING, AND CONTROL SOURCES WHICH ARE USED INDEPENDENTLY. THEY PERIODICALLY REFRESH THE DYNAMIC IGFET MEMORY CELLS. THE MASC ALSO PROVIDES THE NECESSARY CONTROL AND SEQUENCING LOGIC TO ACCEPT ADDRESSES FROM THE 3A CC VIA THE MASB ADDRESS LEADS (SA00-SA19, SAPL, SAPH) AND TO EITHER READ OR WRITE THE CONTENTS OF THE ADDRESSED LOCATION VIA MASB DATA LEADS (SD00-SD15, SDPL, SDPH). THE READ OR WRITE CONTROL IS DETERMINED BY A 2-OUT-OF-4 CONTROL CODE ISSUED BY THE 3A CC ON THE MASB CONTROL LEADS (SC0-SC3). THE MASB SIGNALS ARE REPEATED AT EACH MASC SO THAT, IF THE WORD ADDRESSED IS NOT IN THE FIRST 256K, THE INFORMATION WILL BE RELAYED ON TO THE APPROPRIATE MASC. THERE IS ABOUT A 10 PERCENT SLOW-DOWN IN ACCESS TIME CAUSED BY EACH ADDITIONAL MASC THE BUS SIGNAL MUST PASS THROUGH. IT IS, THEREFORE, EXPEDIENT TO PUT ALL REAL-TIME DEPENDENT CODE IN THE FIRST 256K WORDS.

THE ABILITY TO PROTECT PROGRAMS STORED IN MAIN MEMORY IS PROVIDED BY A WRITE-PROTECT FEATURE. WRITE PROTECT IS PROVIDED ON THE 4K-BLOCK SIZES BY CIRCUITRY WITHIN THE MASC. THE MASC CONTAINS A REGISTER WITH A BIT FOR EACH 4K BLOCK THAT IT CAN ADDRESS. IF THE 3A CC ISSUES A WRITE TO A WORD IN A BLOCK THAT HAS BEEN WRITE PROTECTED, THE MASC WILL ISSUE A WRITE PROTECTION ERROR (STORE ERROR B) SIGNAL TO THE 3A CC AND THE APPROPRIATE ACTION WILL BE TAKEN. THE ABILITY TO ACCESS AND HENCE CHANGE THE STATE OF THE WRITE PROTECT REGISTER IS PROVIDED BY TWO OF THE STATES OF THE MASB CONTROL LEADS (SC0-SC3). THESE CONTROL STATES ARE A FUNCTION OF THE MMS REGISTER IN THE 3A CC. IT, THEREFORE, REQUIRES AN ORDERED SEQUENCE OF EVENTS TO CHANGE THE CONTENTS OF THE WRITE-PROTECT REGISTER.

THE INITIATION OF A MEMORY CYCLE BY THE 3A CC IS GIVEN VIA THE PBC WITH THE STORE GO (SGO) LEAD. THE PRESENCE OF THE SGO SIGNAL INDICATES TO THE MASC THAT THE ADDRESS, THE DATA (IF A WRITE CYCLE), AND THE CONTROL INFORMATION ON THE MASB ARE STABLE AND, THEREFORE, A MEMORY CYCLE MAY AND SHOULD BEGIN. IF A REFRESH IS IN PROCESS, THE REQUEST IS DELAYED (≃ 1us MAXIMUM). WHEN THE MASC HAS COMPLETED ITS REFRESH CYCLE, IT RESPONDS TO THE PRESENCE OF THE GO SIGNAL AND THE REQUESTED MEMORY CYCLE IS THEN PERFORMED. THE MASC INDICATES THAT IT HAS COMPLETED THE REQUESTED MEMORY CYCLE BY USING THE STORE COMPLETE SIGNAL (SCM). CONCURRENTLY WITH MEMORY CYCLE OPERATION, THE 3A CC IS EXECUTING THE PREVIOUSLY FETCHED INSTRUCTION. DEPENDING UPON THE NUMBER OF MICROCYCLES IN THIS INSTRUCTION WHEN THE MICROCONTROL TESTS THE SCM SIGNAL VIA THE DR, THE MICROCONTROL WILL EITHER:

- (A) FIND THE DR=1 AND THEREFORE CONTINUE EXECUTING ADDITIONAL MICROINSTRUCTIONS IN RESPONSE TO THE DATA FETCHED FROM THE MAS.
- (B) FIND THE DR=0 AND IT THEREFORE WILL LOOP WHILE WAITING FOR THE MEMORY TO COMPLETE.

CIRCUIT OPERATION (CONT)

THE MASC, IN COMBINATION WITH THE MAS, IS A SELF-CHECKING UNIT AND, AS SUCH, IT PERFORMS A NUMBER OF HARDWARE CHECKS INCLUDING PARITY CHECKS ON THE ADDRESS AND DATA FIELDS IT RECEIVES. BECAUSE THE ADDRESS AND DATA REGISTERS ARE BIT SLICED IN THE 3A CC, IN THE MASC, AND IN THE MAS, A PARITY CHECK CODE OVER THE ADDRESS AND DATA FIELDS REPRESENTS A VERY EFFICIENT AND COMPLETE CHECK ON ALL MULTIPLE FAULTS THAT AFFECT NO MORE THAN ONE CIRCUIT PACK. THE RESULTS OF ALL THE CHECK CIRCUITS ARE PLACED ON THE MASB ERROR LEADS (SERA,SERB,SERC) AND, ON EACH MEMORY REQUEST BY THE 3A CC THE CONTENTS OF THE ERROR LEADS ARE DIRECTLY GATED TO THE ERROR REGISTER (ER) WITHIN THE 3A CC. AS IN THE CASE OF THE OTHER ERROR CONDITIONS MONITORED IN THE ER, THE ABILITY TO IGNORE OR AT LEAST POSTPONE IMMEDIATE RESPONSE TO ERRORS COMING FROM THE MAS IS PROVIDED BY THE BLOCK HARDWARE CHECK (BHC) FLIP-FLOP FOR THE MORE SERIOUS TYPES OF ERRORS AND BY THE INTERRUPT MASK (IM) REGISTER FOR THE REMAINING LESS SERIOUS ERRORS. THE ABILITY TO EXERCISE THE CHECKERS IN THE MASC AND HENCE, PROVIDE MAINTIANABILITY IS IMPLEMENTED BY A DEDICATED I/O SUBCHANNEL PORT FROM THE 3A CC TO EACH MASC.

THE TIMING BETWEEN THE CC AND THE MASC IS ASYNCHRONOUS. THIS ASYNCHRONISM PROVIDES FLEXIBLITY IN THE PRESENT DESIGN AND POTENTIALLY ALLOWS A VARIETY OF DIFFERENT MAIN MEMORY DESIGNS TO BE IMPLEMENTED INDEPENDENTLY OF THEIR INDIVIDUAL ACCESS TIMES AND CYCLE TIMES. FOR EXAMPLE, THE PRESENT NO. 3A CC MAS USES AN IGFET REFRESHABLE CELL. SINCE THE MAS MUST PERIODICALLY GO INTO A REFRESH CYCLE. THE ACCESS TIME FOR AN MAS REQUEST FROM THE 3A CC FOR A GIVEN CYCLE MAY VARY CONSIDERABLY. BECAUSE THE TIMING IS ASYNCHRONOUS, THE VARIABILITY DOES NOT CREATE A PROBLEM. THE DESIGN ALSO ALLOWS MULTIPLE USERS OR UNITS TO BE ATTACHED TO MEMORY BUS AND TO TIME SHARE THE MEMORY RESOURCES. THE ASYNCHRONOUS NATURE OF THE MEMORY BUS ALLOWS A SIMPLE AND DIRECT METHOD OF PERFORMING THE HANDSHAKING BETWEEN VARIOUS UNITS ATTACHED TO THE BUS.

PBC CONTROL AND SEQUENCING

THE CONTROL AND SEQUENCING PART OF THE PBC PROVIDES THE CONTROL INTERFACE BETWEEN THE MICROPROGRAM CONTROL OF THE 3A CC AND THE CONTROL LOGIC IN THE MASC. ITS PRIMARY FUNCTION AS A CONTROL ENTITY IS TO RECEIVE, BUFFER, AND EXECUTE MAS REQUESTS ISSUED BY THE MICROCONTROL.

THE CONTROL PORTION OF THE PBC CAN BE SUBDIVIDED INTO TWO SEPARATE PARTS FOR THE PURPOSE OF DESCRIBING ITS FUNCTIONAL OPERATION. THE TWO PARTS ARE:

- (A) THE CONTROL PORTION THAT DETERMINES THE STATIC CONDITIONS (REMAIN FIXED DURING A MEMORY CYCLE) OF THE PBC.
- (B) THE CONTROL PORTION THAT DETERMINES THE DYNAMIC CONDITIONS OR STATES (SEQUENCE THROUGH ON A GIVEN MEMORY CYCLE) OF THE PBC.

1. PBC STATIC STATES (MMS REGISTER)

THE STATIC STATES ARE BUFFERED IN A REGISTER CONTAINED WITHIN THE PBC CALLED THE MAIN MEMORY STATE (MMS) REGISTER. AS INDICATED IN COMPOSITE DIAGRAM 2, EACH PBC HAS ITS OWN COPY OF THE MMS SO THAT EACH BIT OF THE MMS IS DUPLICATED, WITH THE EXCEPTION OF THE TWO UPPER BITS. THE UPPER TWO BITS OF THE MMS ARE USED FOR THE ERROR RECOVERY TECHNIQUES (BIT 14-CW AND BIT 15-BEC). ALTHOUGH THEY ARE THE ONLY TWO BITS NOT DUPLICATED AT THE REGISTER CELL LEVEL, THEY HAVE DUPLICATED OUTPUTS TO PRESERVE PARITY ACROSS THE MMS WHEN GATING IT TO THE GB (SEE NOTE, SHEET B4GB). THE MMS IS 16 BITS IN WIDTH, AND IT IS LOADED VIA MICROPROGRAM CONTROL USING A MISCELLANEOUS DECODER CROSSPOINT. THIS CROSSPOINT LOADS BITS 0-15 OF THE BRO REGISTER (CONTAINED IN DMLO) INTO THE MMS USING "DUAL RAIL GATING". NOTE THAT, SINCE THE CONTENTS OF THE MMS CAN DIRECTLY AND IMMEDIATELY AFFECT OTHER USERS ON THE BUS (i.e. BRINGING UP THE ISOLATE STATE), THE GATING INTO THE MMS MUST NOT CAUSE MOMENTARY CHANGES OF STATE OF THE BITS OF THE REGISTER. THUS, THE "CLEAR AND GATE" TECHNIQUE USED IN NORMAL REGISTER TO REGISTER IN THE 3A CC IS NOT PERMISSALBE. THE ABILITY TO ACCESS THE MMS IS PROVIDED BY A FROM-FIELD CROSSPOINT WHICH GATES IT DIRECTLY ONTO THE GB. AS A RESULT, THE MMS MUST MAINTAIN VALID PARITY. SINCE ALL BITS ARE EITHER DUPLICATED OR HAVE DUPLICATED APPEARANCES ON THE GB AND, EXCEPT FOR THE IDLE BITS, ARE ALWAYS ALIKE, THE PARITY CAN EASILY BE PREDICTED BY THE HARDWARE. THE PREDICTED VALUE OF PARITY IS INDICATED IN NOTE 2 OF SHEET B4GB. IF FOR MAINTENANCE OR OTHER REASONS THE MMS MUST BE ACCESSED WITH BAD PARITY, THE GB PARITY CHECKER SHOULD BE INHIBITED. DURING A 3A CC INITIALIZATION PROCEDURE, THE MMS IS LOADED BY THE MICROPROGRAM CONTROL WITH THE USE OF A MICROCONTROL DATA COMMAND. THIS COMMAND OBTAINS A CONSTANT FROM THE MICROSTORE TO DEFINE THE INITIAL STATE OF THE MASB. THE MMS, HAVING BEEN LOADED WITH THIS CONSTANT, THEN DETERMINES THE BASIC MODE OF OPERATION OF THE

CIRCUIT OPERATION (CONT)

MASB OF THE 3A CC FOR THE SUBSEQUENT MEMORY REQUESTS TO BE USED DURING THE INITIALIZATION. ONCE THE INITIALIZATION SEQUENCE HAS STARTED TO ACCESS MAIN MEMORY INSTRUCTIONS, THE MMS CAN BE ALTERED AGAIN. THAT IS, THERE ARE MAINTENANCE TYPE INSTRUCTIONS (MSFN,MSFNX,MI,MIS) THAT PROVIDE THE ABILITY TO RELOAD THE MMS. THE MMS CONTROLS SUCH FUNCTIONS AS:

- (A) WHETHER A READ OR WRITE IS TO BE PERFORMED.
- (B) WHETHER WRITES ARE ISSUED TO BOTH MAS'S.
- (C) WHICH MASB IS ACTIVE IN THE CASE OF A READ.
- (D) WHETHER THE BUS REPEATER SHOULD ISOLATE ITSELF FROM USERS OF LOWER PRIORITY ATTACHED TO THE BUS, ETC.

THE FOLLOWING DESCRIBES THE BITS IN THE MMS AND THEIR FUNCTIONS.

MM1,MM2, AND R.W BITS (SEE TABLE A)

MM1 AND MM2 ARE TWO BITS WHICH ARE ENCODED INTO FOUR BINARY STATES. THE FOUR STATES LISTED BELOW. TOGETHER WITH THE READ-WRITE (R.W) BIT, DETERMINE THE 2-OUT-OF-4 CODE THAT IS SENT TO THE MASC TO DEFINE THE TYPE OF REQUEST THAT HAS BEEN ISSUED TO IT BY THE 3A CC. THIS 2-OUT-OF-4 CONTROL CODE IS SENT ON THE SC0-SC3 CONTROL LEADS IN THE MASB.

TABLE A

MM2	MM1	R.W	SC3-SC0	FUNCTIONS TO BE PERFORMED IN THE MAS
0	0	0	0011*	NORMAL WRITE
0	0	1	1100	NORMAL READ
0	1	0	0110	WRITE THE WRITE PROTECT REGISTER
0	1	1	1001	READ THE WRITE PROTECT REGISTER
1	0	0	0101†	SPARE (BLIND WRITE)
1	0	1	1010	SPARE
1	1	0	0011 **	PUTS PBC IN THE LOCK STATE AND PERMITS A NORMAL READ OR WRITE
1	1	1	1100 **	

* THE SC3 SIGNAL IS ALWAYS EQUAL TO THE R.W BIT FOR DATA REQUESTS (I.D=0). FOR INSTRUCTION FETCHES OR INSTRUCTION OPERAND FETCHES (I.D=1), THE PBC IS ASSUMED TO BE IN THE READ MODE. THAT IS I.D=1 FORCES SC3=1 INDEPENDENT OF THE R.W BIT.

† THIS 2-OUT-OF-4 STATE CAN BE USED FOR ISSUING BLIND WRITES IF A SINGLE BACKPLANE STRAP OPTION IS IMPLEMENTED IN THE MASC. BLIND WRITES ARE WRITE REQUESTS THAT ARE PERFORMED INDEPENDENTLY OF THE WRITE PROTECT FUNCTION IN THE MAIN STORE CONTROLLER. NO. 2B ESS OR NO. 3 ESS SYSTEMS DO NOT PROVIDE THIS BLIND WRITE FEATURE.

** THE LOCK STATE IS USED TO REQUEST THE EXCLUSIVE USE OF THE MEMORY BUS FOR AN EXTENDED NUMBER OF MEMORY CYCLES.

IDL BIT

THE IDL BIT IS USED TO IDLE OR DISABLE A PARTICULAR PBC. AS SHOWN IN COMPOSITE DIAGRAM 2, THERE IS PBC FOR 0 AND A PBC FOR STORE BUS 1. THEREFORE, IF THE IDL BIT IS NOT SET THE RESPECTIVE PBC WILL RESPOND TO MEMORY REQUESTS ISSUED BY THE MICROPROGRAM CONTROL. ONE IDL BIT MUST BE SET AT ALL TIMES.

UPD BIT

THE UPD BIT IS USED TO INDICATE THAT THE SYSTEM IS IN THE UPDATE MODE AND, AS SUCH, WRITE COMMANDS ARE TO BE ISSUED TO BOTH STORES. THUS, WHEN THE UPD BIT IS SET, BOTH PBC0 AND PBC1 ARE ACTIVATED FOR WRITE REQUESTS AND THE EFFECT OF THE IDL BIT IS NULLIFIED FOR THOSE RESPECTIVE WRITE CYCLES.

ISO BIT

THE ISO BIT IS USED TO ISOLATE OR INHIBIT FOR MAINTENANCE PURPOSES, ANY PROCESSOR OR OTHER FUNCTIONAL UNIT ATTACHED TO THE MEMORY BUS THAT IS OF LOWER PRIORITY, FROM GAINING ACCESS TO THE MEMORY. PRIORITY IS POSITIONALLY ASSIGNED AND THE CLOSER THE PROCESSOR OR FUNCTIONAL UNIT IS TO THE MEMORY, THE HIGHER ITS PRIORITY.

CIRCUIT OPERATION (CONT)

BDSR BIT

THE BLOCK DOUBLE STORE READ (BDSR) BIT IS USED TO DETERMINE THE TYPE OF ERROR RECOVERY PROCEDURE TO BE INVOKED WHEN A PARITY ERROR IS DETECTED IN A WORD BEING READ OUT OF THE MAS. IF THE BDSR BIT IS ZERO, THE DSR TECHNIQUE WILL BE USED. IF THE BDSR BIT IS A ONE, THE COMPLEMENT CORRECTION TECHNIQUE WILL BE USED.

CW BIT

THE COMPLIMENT WRITE BIT IS USED TO INDICATE TO THE MASC A SPECIAL MAINTENANCE CONDITION. IF THIS BIT IS ACTIVE UPON RECEIVING A WRITE COMMAND FROM THE 3A CC, THE MASC WILL WRITE INTO THE ADDRESS INDICATED BY THE MASB THE COMPLEMENT OF THE LAST WORD THAT HAS BEEN READ OUT OF THE MAS (SEE SHEET D12).

BEC BIT

THE BLOCK ERROR CORRECTION BIT IS USED TO INHIBIT ALL ERROR RECOVERY PROCEDURES WITHIN THE 3A CC ASSOCIATED WITH INCORRECT STORE READ DATA.

IN CONTRAST TO THE ISOLATE STATE, THE LOCK STATE (MM1=1, MM2=1) IS USED TO "REQUEST" THE EXCLUSIVE USE OF THE MEMORY BUS OF BOTH LOWER AND HIGHER PRIORITY UNITS ATTACHED TO THE BUS. IF THE BUS IS BUSY (A UNIT OF LOWER PRIORITY USING THE BUS) AT THE TIME THE LOCK IS ISSUED, THE LOCK CONDITION ON THE MEMORY BUS IS DELAYED UNTIL THE BUS HAS BECOME FREE. ON THE OTHER HAND, WHEN THE ISOLATE STATE IS LOADED ONTO THE MMS, NO CHECK IS MADE OF THE PRESENT STATUS OF THE BUS. THEREFORE, IF THE BUS IS PRESENTLY IN USE BY ANOTHER USER OF LOWER PRIORITY, THE ACTIVATION OF THE ISOLATE STATE, BY SETTING THE ISO BITS, WILL ABNORMALLY TERMINATE THE MEMORY CYCLE OF THE LOWER PRIORITY UNIT. THUS, THE ISOLATE STATE SHOULD ONLY BE USED AS FOLLOWS:

- (A) TO ALLOW THE MAINTENANCE PROGRAMMER TO "ISOLATE" FAULTS ON THE MEMORY BUS REPEATERS SO AS TO OBTAIN DIAGNOSTIC INFORMATION.
- (B) TO ALLOW SYSTEM PARTITIONING SO THAT A WORKING HALF SYSTEM IS ISOLATED FROM THE OTHER HALF SYSTEM IF THE STATE OF THAT SYSTEM IS EITHER IN ERROR OR IN DOUBT. INITIALIZATION OF A 3A CC RESULTS IN THE MICROPROGRAM CONTROL LOADING THE MMS WITH ISO BITS SET, SINCE THE STATE OF THE OTHER 3A CC IS UNKNOWN AT THIS TIME. A SYSTEM PROGRAM WILL SUBSEQUENTLY DETERMINE THE INTEGRITY OF THE OTHER HALF SYSTEM AND WILL DECIDE IF THE ISOLATE STATE IS TO BE REMOVED.

IF THE BUS IS NOT BUSY OR IT BECOMES NOT BUSY AND THE LOCK STATE IS ACTIVE, THE CONTROL IN THE PBC THAT IS ISSUING A MEMORY REQUEST WILL:

- (A) ACTIVATE THE STORE REQUEST (SREQ) LEAD ON THE MASB. THIS LEAD IS USED TO INDICATE TO USERS OF HIGHER PRIORITY THAT EXCLUSIVE USE OF THE BUS IS REQUESTED BY A UNIT OF LOWER PRIORITY. IF THE UNIT OF HIGHER PRIORITY IS PRESENTLY USING THE BUS, THE REQUEST IS DELAYED UNTIL THAT MEMORY CYCLE IS COMPLETE. THEN THE SREQ SIGNAL IS REPEATED ON UP THE LINE (TOWARDS THE STORE). IN THIS WAY, A UNIT THAT HAS ITS INCOMING SREQ SIGNAL ACTIVE AND IS NOT PRESENTLY IN THE PROCESS OF PERFORMING A MEMORY CYCLE CANNOT ISSUE ANOTHER MEMORY REQUEST UNTIL THE INCOMING SREQ SIGNAL IS REMOVED.
- (B) ACTIVATE THE ISOLATION OF ITS OWN BUS REPEATER SO THAT UNITS OF LOWER PRIORITY CANNOT USE THE MEMORY EITHER. THE LOCK CONDITION ON THE BUS WILL REMAIN ACTIVE UNTIL THE MICROPROGRAM CONTROL CHANGES THE STATE OF MM1 AND MM2 IN THE MMS REGISTER.

THEREFORE, IF THE LOCK STATE IS SET, THE ISSUING PROCESSOR CAN MAKE MULTIPLE MEMORY REQUESTS WITHOUT THE UNCERTAINTY OF DATA IN MEMORY CHANGING OUT FROM UNDER IT (FOR EXAMPLE, IN THE READ-MODIFY-WRITE SITUATION). THE LOCK STATE ALLOWS THE ABILITY TO IMPLEMENT TIME SHARING OF THE CONTENTS OF MEMORY FOR SUCH FUNCTIONS AS MULTIPROCESSING. NOTE THAT IF A FAULT OCCURS SO THAT THE LOCK STATE IS STUCK ACTIVE, THE PROCESSOR OF HIGHER PRIORITY CAN PUT ITSELF INTO THE ISOLATE STATE AND REMOVE THE EFFECT OF THE SREQ SIGNAL ON IT. IN THIS WAY, A CORRECTLY OPERATING MACHINE CAN ISOLATE ITSELF WHEN "ON-LINE" FROM A FAULTY UNIT ATTACHED TO THE BUS WHICH IS OF LOWER PRIORITY.

(CONT ON SHT B4GH)

PART OF FS 4

3A CENTRAL CONTROL ②

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4GG

PART OF FS 4

PROCESSOR BUS CONTROLLER

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2-6 (CONT)

CIRCUIT OPERATION (CONT FROM SHT B4GG)

AS INDICATED, THERE ARE THREE METHODS TO OBTAIN CONTROL OF THE BUS REPEATER ITSELF. THE FIRST IS THE SETTING OF THE IS0 BIT IN THE MMS. AS SHOWN, THIS BIT DOES NOT CHECK THE PRESENT STATE OF THE BUS BEFORE PERFORMING THE FUNCTION. THE SECOND METHOD IS TO PUT THE PBC IN THE LOCK STATE. IN THIS CASE THE CONTROL CHECKS FOR THE MASB TO BE NONBUSY BEFORE ACTIVATING LOCK CONDITION. THE THIRD IS WITH THE USE OF THE SEIZE FLIP-FLOP THAT ALSO CHECKS FOR A NONBUSY CONDITION BEFORE SEIZING THE BUS. THE SEIZE FUNCTION IS ACTIVATED ON EACH MEMORY CYCLE AND IT GUARANTEES THAT WHILE A SINGLE MEMORY CYCLE IS IN PROGRESS, IT WILL NOT BE INTERRUPTED BY OTHER USERS ON THE BUS. THEREFORE, THE ISOLATE STATE, THE LOCK STATE, AND THE SEIZE STATE ALL ACCOMPLISH THE SAME GOAL AT THE BUS REPEATER. THE DIFFERENCE IS THE METHOD OF TESTING THE BUS BEFORE EXECUTING THE FUNCTION PERFORMED BY THE THREE STATES AND THE DURATION FOR WHICH THEY ARE ACTIVE. THUS, THE ISOLATE STATE, IF ACTIVE, WOULD TEND TO REMAIN ACTIVE FOR AN INDEFINITE PERIOD (i.e. UNTIL THE FAULT BEING ISOLATED IS REMOVED OR DETERMINED NOT TO BE A PROBLEM). THE LOCK STATE WOULD TEND TO BE ACTIVE FOR ONLY A FEW MEMORY CYCLES. THE SEIZE STATE IS ACTIVE FOR ONLY THE DURATION OF ONE CYCLE. THE FACT THAT THE SEIZE STATE IS ACTIVE FOR ONLY ONE MEMORY CYCLE GUARANTEES THAT, IF A UNIT OF LOWER PRIORITY IS WAITING AT THE INPUT OF A REPEATER THAT IS PRESENTLY ISSUING A MEMORY REQUEST (AND THAT UNIT IS NOT IN THE LOCK OR ISOLATE STATE) THE LOWER PRIORITY UNIT WILL BE SERVICED NEXT (i.e. ITS MEMORY REQUEST PERFORMED). IN THIS WAY, MULTIPLE USERS ATTACHED TO THE BUS WILL TEND TO INTERLEAVE THEIR MEMORY REQUESTS UNLESS ONE OF THE USERS INVOKES A LOCK OR ISOLATE STATE.

IN ORDER TO PROVIDE AN ERROR DETECTION SCHEME FOR EITHER HARDWARE OR SOFTWARE FAULTS THAT RESULT IN A MEMORY BUS BEING OCCUPIED OR BUSY FOR AN INORDINATE AMOUNT OF TIME, A HARDWARE "FAST TIME-OUT" MECHANISM IS IMPLEMENTED (SEE COMPOSITE DIAGRAM 4). THE "FAST TIME-OUT" NOMENCLATURE IS USED TO DISTINGUISH THIS TIME-OUT FUNCTION FROM THE PROGRAM TIMER TIME-OUT FUNCTION USED AS THE BASIC SYSTEM SANITY CHECK. THE PROGRAM TIMER TIME-OUT IS SOFTWARE CONTROLLED AND RANGES FROM 500ms IN THE ON-LINE 3A CC TO 1.6 SECONDS IN THE OFF-LINE 3A CC. THE "FAST TIME-OUT" WILL FIRE APPROXIMATELY 50us(38.2 TO 57.6us) AFTER INITIATION OF A MEMORY CYCLE BY THE MICROPROGRAM CONTROL IF THE CYCLE HAS NOT BEEN COMPLETED. THUS, USERS OF THE LOCK CAPABILITY MUST LIMIT THE NUMBER OF MEMORY CYCLES FOR WHICH THE EXCLUSIVE USE OF THE BUS IS REQUIRED.

2. PBC DYNAMIC STATES

THE DYNAMIC STATES OF THE PBC ARE THOSE STATES THROUGH WHICH THE CONTROL LOGIC MUST SEQUENCE IN THE PROCESS OF:

(A) ISSUING A MAS REQUEST TO THE MASC.
(B) RECEIVING THE APPROPRIATE RESPONSE.
(C) COMPLETING THAT MEMORY CYCLE.

TO PERFORM THIS SEQUENCING, THERE ARE SIX MAIN FLIP-FLOPS THAT REFLECT THE CONTROL STATES THAT ARE SEQUENCED THROUGH. THESE CONTROL STATES ARE SHOWN ON COMPOSITE DIAGRAM 3. THE FOLLOWING IS A LIST OF THE CONTROL STATE FLIP-FLOPS AND THE FUNCTIONS THAT THEY PERFORM ON A GIVEN MEMORY CYCLE OPERATION.

REQUEST FLIP-FLOP

THE REQUEST FLIP-FLOP IS USED TO INDICATE THAT A REQUEST FOR A MEMORY CYCLE HAS BEEN ISSUED BY THE MICROCONTROL. (THE FUNCTION OF THE REQUEST FLIP-FLOP IS NOT RELATED TO THE STORE REQUEST [SREQ] SIGNAL THAT IS USED ON THE MASB.) THE SETTING OF THE DR INDICATES TO THE MICROCONTROL THAT A PREVIOUSLY ISSUED MAS REQUEST HAS TERMINATED. ONCE THE DR HAS BEEN SET, THE MICROCONTROL CAN IMMEDIATELY SET THE REQUEST FLIP-FLOP TO INITIATE THE NEXT MAS REQUEST. THE SETTING OF THE REQUEST FLIP-FLOP BY THE MICROCONTROL ALLOWS THE MICROCONTROL TO CONTINUE EXECUTING MICROINSTRUCTIONS WITHOUT CHECKING TO DETERMINE WHETHER THE MASB IS BUSY OR IDLE.

SEIZE FLIP-FLOP

THE SEIZE FLIP-FLOP IS USED TO INDICATE THAT THE PBC IS IN THE PROCESS OF ISSUING A MEMORY REQUEST TO THE MAIN STORE. THE SEIZE FLIP-FLOP IS NOT SET UNTIL THE BUS BECOMES NONBUSY. IN THIS INSTANCE, NONBUSY IS DEFINED AS:

(A) NO INCOMING REQUESTS TO THE BUS REPEATER.

(B) THE STORE COMPLETE AND STORE ERROR SIGNALS FROM THE MASC INDICATE AN IDLE CONDITION AT THE MASC.

NOTE THAT, ONCE THE MEMORY REQUEST IS ISSUED ONTO THE BUS, IT MAY BE DELAYED BY UNITS OF HIGHER PRIORITY CLOSER TO THE MASC. THE FUNCTION OF THE SEIZE FLIP-FLOP IS TO ISOLATE THE BUS FROM UNITS OF LOWER PRIORITY SO THEY DO NOT INTERFERE WITH THE MEMORY CYCLE PRESENTLY IN PROGRESS. AT THE COMPLETION OF THE MEMORY CYCLE, THE SEIZE FLIP-FLOP WILL BE RESET WHICH ALLOWS OTHER USERS ON THE BUS TO ISSUE THEIR REQUEST TO THE MAS.

CIRCUIT OPERATION (CONT)

GO FLIP-FLOP

THE GO FLIP-FLOP IS USED TO ACTIVATE THE SG0 SIGNAL TO THE MASC. THE SG0 INDICATES THAT THE ADDRESS AND DATA (IF A WRITE CYCLE) AND THE OTHER CONTROL SIGNALS ON THE MASB ARE STABLE AND THAT THE CYCLE SHOULD BEGIN. THE GO FLIP-FLOP BECOMES ACTIVE AT APPROXIMATELY THE SAME TIME AS THE SEIZE FLIP-FLOP BECOMES ACTIVE. ON THE OTHER HAND, THE GO FLIP-FLOP BECOMES INACTIVE WHEN THE STORE COMPLETE (SCM) SIGNAL RETURNS FROM THE STORE INDICATING THAT THE STORE HAS COMPLETED THE REQUESTED CYCLE. THE ACTUAL RESETTING OF THE GO FLIP-FLOP IS PERFORMED BY SETTING THE DR.

DR FLIP-FLOP

THE DATA READY(DR) FLIP-FLOP IS USED TO INDICATE TO THE MICROPROGRAM CONTROL THAT THE STORE HAS COMPLETED THE REQUESTED MEMORY CYCLE. IT IS SET IN RESPONSE TO AN ACTIVE SCM SIGNAL RETURNING FROM THE MASC. EACH MICROCYCLE, THE STATE OF THE SCM SIGNAL IS GATED TO THE DR FLIP-FLOP. THIS PERMITS THE DR FLIP-FLOP TO BE TESTED BY THE MICROCONTROL WITHOUT THE UNCERTAINTY OF ITS OUTPUT CHANGING STATES DURING THE TEST.

ENREL FLIP-FLOP

THE ENABLE RELEASE (ENREL) FLIP-FLOP IS USED TO INDICATE THAT AN SCM SIGNAL HAS BEEN ACTIVATED AND HENCE A PBC CYCLE IS TO BE TERMINATED. IT IS SET WHEN THE DR IS SET, BUT UNLIKE THE DR, IT IS CLEARED WHEN THE PBC CYCLE ENDS (i.e. SEIZE-0 CLEARS THE ENREL FLIP-FLOP).

I.D. FLIP-FLOP

THE INSTRUCTION OR DATA (I.D.) FLIP-FLOP IS USED TO INDICATE WHETHER THE MEMORY CYCLE THAT IS BEING ISSUED IS AN INSTRUCT TYPE OR A DATA TYPE. THAT IS, IF THE I.D. FLIP-FLOP EQUALS ONE, THAT DATA RETURNED IS PUT INTO THE SIR REGISTER. IF THE I.D FLIP-FLOP EQUALS ZERO, THE DATA RETURNED IS PUT INTO THE SDR REGISTER. THE I.D FLIP-FLOP IS ALSO USED TO DETERMINE THE STATE OF SC3 LEAD ON THE MAIN STORE BUS. THIS LEAD DETERMINES WHETHER THE CYCLE BEING ISSUED IS A READ OR A WRITE CYCLE. THE ASSUMPTION IS THAT, IF THE I.D FLIP-FLOP IS EQUAL TO A ONE, A READ IS REQUESTED, INDEPENDENT OF THE READ-WRITE FLIP-FLOP. AS EXPLAINED ABOVE, THIS ALLOWS THE R.W FLIP-FLOP TO BE SET INDEPENDENTLY OF THE PRESENT STATE OF THE PBC. ALSO, THE I.C FLIP-FLOP EQUALLING TO ONE DETERMINES WHETHER THE SAR IS GATED AROUND INTO THE PA AT THE START OF THE MEMORY CYCLE SO THAT THE PA+1 LOGIC CAN COMPUTE THE NEXT SEQUENTIAL ADDRESS FOR THE FOLLOWING INSTRUCTION.

3. MICROPROGRAM CONTROL INTERFACE TO PBC

THE BASIC FUNCTIONS THE MICROCONTROL MUST PERFORM IN THE PROCESS OF EXECUTING A MAS REQUEST ARE:

(A) LOAD THE MMS REGISTER
(B) ISSUE A MAS REQUEST
(C) TEST FOR A MAS COMPLETION AND
(D) GATE THE ACCESSED DATA TO THE APPROPRIATE DESTINATION WITHIN THE 3A CC.

THESE TWO FUNCTIONS ARE NORMALLY COMBINED INTO A SINGLE OPERATION.

METHODS OF LOADING THE MMS

THE BASIC MODE OF OPERATION OF THE PBC IS DEDICATED BY THE MICROPROGRAM CONTROL THROUGH THE USE OF THE MMS REGISTER. ONCE THE MMS HAS BEEN LOADED, THE MICROPROGRAM CONTROL CAN ISSUE A SEQUENCE OF MEMORY REQUESTS TO THE PBC WITH THE MODE OF OPERATION FOR ALL SUBSEQUENT REQUESTS DEFINED BY THE INITIAL STATE OF THE MMS. THE R.W BIT IS THE ONLY EXCEPTION TO THIS. WHEN THE SDR IS GATED INTO VIA MICROPROGRAM CONTROL, THE READ-WRITE (R.W) BIT IN THE MMS IS PUT INTO THE WRITE MODE. THE ASSUMPTION MADE IS THAT A WRITE REQUEST IS DESIRED UPON THAT DATA. THE R.W BIT IS THEN RESET TO THE READ MODE AT THE COMPLETION OF THE NEXT "DATA CYCLE" (I.D=0) REQUEST TO THE MAS BY THE PBC. NOTE THAT, BECAUSE OF THE CONCURRENT OPERATION OF THE PBC AND THE MICROPROGRAM CONTROL AT THE TIME THE SDR IS LOADED, THE PBC MAY BE IN THE PROCESS OF AN INSTRUCTION REQUEST TO THE MAS. THEREFORE, WHEN THE I.D FLIP-FLOP INDICATES THE INSTRUCTION MODE, THE EFFECT OF THE READ-WRITE FLIP-FLOP IS NULLIFIED. THAT IS, WHEN THE I.D FLIP-FLOP IS SET, THE HARDWARE AUTOMATICALLY ASSUMES THAT THE PBC IS IN THE READ MODE AND THUS ALLOWS THE LOADING OF THE SDR INDEPENDENTLY OF THE STATE OF THE CURRENT INSTRUCTION FETCH CYCLE.

CIRCUIT OPERATION (CONT)

MICROCONTROL INSTRUCTIONS TO ISSUE A MEMORY REQUEST

ONCE THE MICROCONTROL HAS LOADED THE MMS, IT MAY THEN ISSUE A MAS REQUEST TO THE PBC. NORMALLY, THE MMS HAS BEEN LOADED BY A PREVIOUS OPERATION AND, THEREFORE, AT THE START OF AN INSTRUCTION THE MICROCONTROL DOES NOT HAVE TO LOAD THE MMS. THERE ARE FIVE WAYS IN WHICH THE MICROPROGRAM CONTROL CAN INITIATE AN MAS REQUEST CYCLE.

CA, CB DECODER (IFETCH)

THE NORMAL AND THE MOST FREQUENT WAY OF ISSUING AN MAS REQUEST IS WITH THE USE OF THE CA, CB DECODER. THE CA, CB DECODER ALLOWS A MAXIMUM OVERLAP OF MICROINSTRUCTION EXECUTION WITH MAS OPERATIONS. AS DETAILED THE CA AND CB BITS ARE OBTAINED ON EACH WORD THAT IS ACCESSED FROM THE MICROSTORE. TYPICALLY, THE FIRST WORD OF EVERY INSTRUCTION EXECUTED CONTAINS THE CA, CB BITS SET TO THE IFETCH STATE WHICH INITIATES THE PBC TO FETCH THE NEXT SEQUENTIAL INSTRUCTION. IN THIS WAY, AS EACH NEW INSTRUCTION IS STARTED, THE PBC IS ACTIVATED TO FETCH THE FOLLOWING INSTRUCTION. IF, AS IN THE CASE OF A TRANSFER INSTRUCTION, THE NEXT SEQUENTIAL WORD IS NOT TO BE FETCHED, THE CA, CB BITS ARE NOT ACTIVATED TO THE IFETCH STATE. THE MICROCONTROL WOULD INSTEAD USUALLY CALCULATE (USING THE DATA MANIPULATION LOGIC [DML]) THE TARGET ADDRESS FOR THE TRANSFER AND LOAD IT INTO THE SAR. THEN IT WOULD INITIATE THE MEMORY REQUEST WITH THE SARI MICROINSTRUCTION. IT SHOULD BE NOTED THAT WITH THE USE OF THE CA, CB DECODER, IT IS ASSUMED THAT THE PA+1 LOGIC IS BEING USED. THEREFORE, WHEN THE CA, CB IFETCH CROSSPOINT FIRES, NOT ONLY THE REQUEST FLIP-FLOP AND THE I.D FLIP-FLOP ARE SET, BUT ALSO THE PA+1 ADDRESS IS LOADED INTO THE SAR.

SARI AND SARD

IN THE CASE OF THE CA, CB IFETCH, IT IS ASSUMED THAT THE PREVIOUS MEMORY REQUEST HAS BEEN COMPLETED AND THEREFORE, THE DR HAS BEEN SET WHEN THE NEXT MEMORY MAS REQUEST IS ISSUED. THERE ARE SOME CASES WHERE IT IS UNCERTAIN THAT THE PREVIOUS REQUEST HAS BEEN COMPLETED AND YET THE MICROCONTROL IS READY TO ISSUE ANOTHER MAS REQUEST. TO ALLOW THE MICROCONTROL TO EFFICIENTLY HANDLE THOSE CASES, TWO SPECIAL MICROINSTRUCTIONS ARE PROVIDED. THESE MICROINSTRUCTIONS ARE THE SARI AND SARD. THE SARI INSTRUCTION IS PERFORMED BY A TO-FIELD DECODER CROSSPOINT. THIS INSTRUCTION IS SIMILAR TO A CONDITIONAL BRANCH SINCE IT LOOPS UPON ITSELF WHILE THE DR FLIP-FLOP IS EQUAL TO ZERO. WHEN THE DR FLIP-FLOP IS SET, IT EXITS FROM THAT LOOP. AS THE SARI INSTRUCTION EXITS FROM THE LOOP, IT ALSO PERFORMS A GATING FUNCTION INTO THE SAR FROM THE GATING BUS (GB) (SEE COMPOSITE DIAGRAM 12). THE SOURCE OF THE DATA THAT IS GATED TO THE SAR IS DEFINED BY AN ARBITRARY FROM FIELD IN THIS PARTICULAR MICROINSTRUCTION. EACH MICROCYCLE, DURING AN SARI LOOP, THE CONTENTS OF THE SELECTED SOURCE REGISTER ARE GATED ON TO THE GB. HOWEVER, IT DOES NOT FLOW INTO THE SAR UNTIL THE DR FLIP-FLOP EQUALS 1. USUALLY, THE INFORMATION THAT IS LOADED INTO THE SAR IS THE ADDRESS (USUALLY COMPUTED WITHIN THE DML) OF THE NEXT WORD TO BE ACCESSED FROM MAIN MEMORY. IN ADDITION, THE SARI MICROINSTRUCTION SETS THE REQUEST FLIP-FLOP AND THE I.D FLIP-FLOP IN THE PBC WHEN THE DR FLIP-FLOP HAS BEEN SET TO 1. WHEN THE DR IS SET TO 1, THE SARI MICROINSTRUCTION PERFORMS THE THREE OPERATIONS; LOADING THE SAR, EXITING OUT OF THE CONDITIONAL LOOP (ADDS ONE TO MAR), AND ISSUING AN INSTRUCTION FETCH TO THE PBC. THE INSTRUCTION FETCH MEANS THAT THE I.D FLIP-FLOP IS SET TO 1 AND THUS, THE ACCESSED WORD RETURNED FROM THE MAS REQUEST WILL BE BUFFERED IN THE SIR. THE OPERATION OF THE SARD MICROINSTRUCTION IS EXACTLY THE SAME TO THE SARI MICROINSTRUCTION, EXCEPT IN THIS CASE THE I.D FLIP-FLOP IS SET TO ZERO. THUS, THE WORD RETURNED FROM THE MAS REQUEST IS BUFFERED IN THE SDR INSTEAD OF IN THE SIR. ALSO, IF THE MMS IS THE WRITE STATE (R.W=0) AND AN SARD IS GIVEN, A WRITE COMMAND IS PERFORMED ON THE DATA CONTAINED IN THE SDR. NOTE THAT THE SARI CANNOT BE USED FOR A WRITE OPERATION.

DATA FETCH (DFETCH)

THE DFETCH MISCELLANEOUS DECODER CROSSPOINT IS USED TO ACTIVATE THE PBC FOR A DATA OPERATION WITH THE MAS. THUS, WHEN A DFETCH IS GIVEN, THE I.D FLIP-FLOP IS ZEROED AND THE RETURNING DATA (IF A READ COMMAND) IS BUFFERED IN THE SDR. IF A WRITE COMMAND, THE DATA WRITTEN IS OBTAINED FROM THE SDR. AGAIN, SIMILAR TO THE CA, CB DECODER AND UNLIKE THE SARI AND THE SARD MICROINSTRUCTIONS, THE DFETCH MISCELLANEOUS DECODER CROSSPOINT METHOD OF ISSUING A MAS REQUEST ASSUMES THAT THE DR FLIP-FLOP IS EQUAL TO 1 AND THE SAR HAS BEEN LOADED BEFORE THE REQUEST IS ISSUED.

CIRCUIT OPERATION (CONT)

START PBC

THE START PBC MISCELLANEOUS DECODER CROSSPOINT IS USED TO ACTIVATE THE PBC FOR AN MAS REQUEST. IT OPERATES IN EXACTLY THE SAME MANNER AS THE DFETCH MISCELLANEOUS CROSSPOINT EXCEPT THAT IT DOES NOT AFFECT THE STATE OF THE I.D FLIP-FLOP. THAT IS, IF THE PREVIOUS STATE OF THE I.D=1, THEN AN INSTRUCTION FETCH IS PERFORMED AND, IF THE PREVIOUS STATE OF THE I.D=0, A DATA FETCH IS PERFORMED. THIS MICROINSTRUCTION WAS IMPLEMENTED TO AID IN THE DESIGN OF THE COMPLEMENT CORRECTION MICROCODE ROUTINE.

TESTING FOR MEMORY COMPLETION

THE MICROCONTROL TESTS FOR THE COMPLETION OF A MAS REQUEST WITH THE USE OF A CONDITIONAL TRANSFER ON THE STATE OF THE DR FLIP-FLOP. THE DR FLIP-FLOP IS SET BY THE PBC AT THE COMPLETION OF EACH MEMORY REQUEST. IT IS SET WHEN THE PBC RECEIVES THE SCM SIGNAL FROM THE MAS AND, TO AVOID AN INDETERMINATE CONDITION WITHIN THE 3A CC, THE ASYNCHRONOUS SCM SIGNAL IS CLOCKED OR STROBED INTO THE DR FLIP-FLOP.

THE MICROCONTROL CAN USE ONE OF SIX DIFFERENT METHODS TO TEST FOR THE SETTING OF THE DR. IN ADDITION, SOME OF THESE METHODS COMBINE THE GATING OF EITHER THE ACCESSED DATA OR THE NEXT ADDRESS TO BE CONTROLLED WITH THE TESTING OF THE DR.

ALL-ZEROS DETECTOR (NA FIELD)

THE MOST FREQUENT WAY OF TESTING THE DR FLIP-FLOP IS BY USE OF AN ALL-ZEROS DETECTOR ATTACHED TO THE OUTPUT OF THE NEXT ADDRESS (NA) FIELD OF THE MICROSTORE OUTPUT. AS EXPLAINED IN FS 1 0P CODES ARE LOADED FROM THE STORE INSTRUCTION REGISTER (SIR) INTO THE MICROSTORE ADDRESS REGISTER (MAR). THEY POINT TO A STARTING ADDRESS OF A SEQUENCE OF MICROINSTRUCTIONS THAT WILL INTERPRET THAT 0P CODE.

THE LAST ADDRESS OF AN 0P CODE SEQUENCE IS INDICATED BY PLACING ALL ZEROS IN THE NA FIELD. THE PRESENCE OF THE ALL-ZEROS ADDRESS IS DETECTED BY THE ALL-ZEROS HARDWARE AND IS USED TO INDICATE THAT AN 0P CODE SEQUENCE HAS TERMINATED. WHEN THE ALL-ZEROS DETECTOR FIRES, THE STATE OF THE DR FLIP-FLOP IS SAMPLED. IF THE DR IS EQUAL TO 1, THE NEXT 0P CODE THAT HAS BEEN FETCHED IS GATED FROM THE SIR INTO THE MAR TO INITIATE THE NEXT SEQUENCE OF MICROINSTRUCTIONS THAT WILL PERFORM THE 0P CODE. IF THE DR IS NOT SET, THE ALL-ZEROS CONSTANT THAT IS READ FROM THE MICROSTORE WILL FLOW THROUGH THE MIR AND AROUND INTO THE MAR IN THE NORMAL MANNER. THIS WILL CAUSE THE MICROCONTROL TO ACCESS WORD ZERO OF THE MICROSTORE. WORD ZERO OF THE MICROSTORE ALSO CONTAINS ALL ZEROS IN THE NA FIELD. THEREFORE, IF A PREVIOUS MEMORY REQUEST IS READY (DR=1), THE NEXT 0P CODE IS LOADED INTO THE MAR AND ACCESSED IMMEDIATELY. IF AN 0P CODE SEQUENCE COMPLETES AND THE MAS HAS NOT YET RESPONDED, THE MICROCONTROL WILL LOOP AT THE ALL ZEROS LOCATION, UNTIL THE DR IS SET.

SARI AND SARD

THE SARI INSTRUCTION ALSO TESTS FOR THE DR BEING SET BUT UNLIKE THE ALL-ZEROS TEST ANY EVEN NUMBERED WORD ADDRESS MAY BE CONTAINED IN THE NA FIELD. IT IS THE TO-FIELD PORTION OF THE MICROSTORE OUTPUT THAT IS DECODED AND USED TO GATE THE CONTENTS OF THE DR FLIP-FLOP INTO THE LOW-ORDER BIT OF THE MAR. THAT IS, IF THE DR IS EQUAL TO ZERO, THE NEXT ADDRESS THAT THE MICROCONTROL WILL ACCESS IS THE SAME AS THE ONE BEING READ AT THE MICROSTORE. IF THE DR IS EQUAL TO 1, THE NEXT ADDRESS ACCESS BY THE MICROCONTROL WILL BE THE ADDRESS BEING READ OUT OF THE MICROSTORE PLUS ONE. AS INDICATED PREVIOUSLY, THE SARI ALSO INITIATES THE NEXT MAS REQUEST AS WELL. THE SARD WORKS IN EXACTLY THE SAME MANNER EXCEPT THAT IT PUTS THE I.D FLIP-FLOP IN THE DATA MODE (I.D=0).

SIRC AND SDRC

THE SIRC AND SDRC MICROINSTRUCTIONS ARE USED TO TEST FOR AN MAS RESPONSE WHEN DATA IS BEING RETURNED TO THE SIR OR SDR REGISTERS. THE SIRC OPERATES IN THE SAME MANNER TO THE SARI MICROINSTRUCTION IN THAT IT COMBINES THE TESTING OF THE DR WITH A GATING OPERATION. THAT IS, IT IS A CONDITIONAL LOOPING INSTRUCTION THAT LOOPS ON AN EVEN BOUNDARY ADDRESS DEFINED BY ITS NA FIELD. WHEN THE DR IS SET, IT TRANSFERS TO THAT ADDRESS PLUS ONE. AS THE NAME IMPLIES, THE CONDITIONAL GATING FROM THE SIR TO THE GB ON EACH MICROCYCLE IN THE LOOP. DURING THE MICROCYCLE IN WHICH THE DR IS SET, THE CONTENTS OF THE SIR ARE GATED TO A DESTINATION REGISTER VIA THE GB AS DEFINED BY THE CONTENTS OF THE TO FIELD. THE FROM FIELD IS USED TO DEFINE THIS AS AN SIRC INSTRUCTION. THE FROM-FIELD GATING IS ACTUALLY DISABLED WHILE THE DR=0. THEREFORE, THE GB PARITY CHECKER MUST BE INHIBITED WHILE IN THE SIRC LOOP SINCE ZEROS ARE BEING PUT ONTO THE GB (i.e. GOOD PARITY IS DEFINED AS ODD). THE SDRC OPERATES EXACTLY THE SAME AS THE SIRC EXCEPT THAT THE SDR REGISTER IS USED AS THE SOURCE REGISTER OF THE CONDITIONAL GATING OPERATION. (CONT ON SHT B4GJ)

PART OF FS 4

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B4GH

PART OF FS 4

PROCESSOR BUS CONTROLLER

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2-6 (CONT)

CIRCUIT OPERATION (CONT FROM SHT B4GH)

TEST DR

THERE IS A MISCELLANEOUS DECODER CROSSPOINT THAT PERFORMS NO ACTION OTHER THAN TO TEST THE OR FLIP-FLOP. LIKE OTHER CONDITIONAL TRANSFERS IN THE 3A CC MICROINSTRUCTION SET, THIS INSTRUCTION MUST CONTAIN AN EVEN WORD ADDRESS IN ITS NA FIELD. IF THE OR EQUALS 0, THE INSTRUCTION AT THIS ADDRESS WILL BE EXECUTED; IF THE OR EQUALS 1, THE MICROCONTROL WILL TRANSFER TO THIS ADDRESS PLUS ONE.

4. MICROPROGRAM CONTROL RESTRICTIONS

ONE OF THE RESTRICTIONS THAT IS PUT ON THE MICROPROGRAMMER IS THE WAY IN WHICH AN MAS REQUEST IS ISSUED AND HOW THE SUBSEQUENT TEST FOR THE COMPLETION OF THAT REQUEST, IS PERFORMED. THE HARDWARE IS DESIGNED SUCH THAT THE MICROPROGRAMMER MUST WAIT ONE COMPLETE MICROCYCLE BETWEEN ISSUING AN MAS REQUEST AND BEFORE TESTING THE DR. THE REASON FOR THIS IS THAT THE DR IS NOT CLEARED UNTIL THE END OF THE CYCLE IN WHICH THE REQUEST IS ISSUED. THEREFORE, IF THE MICROCONTROL TESTED THE OR IN THE MICROCYCLE IMMEDIATELY FOLLOWING A MICROCYCLE THAT ISSUED AN MAS REQUEST, A RACE CONDITION WOULD RESULT. THIS CONDITION MIGHT, IN TURN, INDICATE AN ERRONEOUS COMPLETION OF A MEMORY CYCLE. THIS RESTRICTION DOES NOT CAUSE A REAL TIME PROBLEM SINCE THE MICROCONTROL MUST IN GENERAL WAIT SIX ADDITIONAL MICROCYCLES FOR THE MAS REQUEST TO COMPLETE ANYWAY.

AN ADDITIONAL RESTRICTION THAT THE MICROPROGRAMMER MUST BE AWARE OF IS THE OPERATION OF THE PA+1 LOGIC. UPON LOADING THE PA, IT TAKES APPROXIMATELY 400ns MAXIMUM OR THREE COMPLETE MICROCYCLES BEFORE THE OUTPUT OF THE PA+1 LOGIC HAS STABILIZED. THIS AGAIN SHOULD NOT CAUSE A PROBLEM UNLESS A MAIN MEMORY IS USED THAT HAS A CYCLE TIME OF LESS THAN 500 ns.

5. AUTONOMOUS OPERATION

ONCE THE MICROCONTROL HAS LOADED THE MMS AND GIVEN A SPECIFIC MAS REQUEST, IT IS THE FUNCTION OF THE PBC TO CARRY OUT THAT REQUEST. APART FROM USING THE FOUR-PHASE CLOCK OF THE 3A CC, THE OPERATION OF THE PBC IN EXECUTING THAT REQUEST IS COMPLETELY AUTONOMOUS TO THE REST OF THE 3A CC. THE MAIN FUNCTION OF THE CLOCK IN THE PBC IS TO SYNCHRONIZE THE ASYNCHRONOUS ARRIVAL OF A MEMORY COMPLETION SIGNAL (SCM) WITH THE TESTING OF THAT COMPLETION BY THE MICROCONTROL. THE BASIC AUTONOMOUS OPERATION OF THE PBC IS DEPICTED IN COMPOSITE DIAGRAM 3.

AN MAS REQUEST IS INITIATED BY THE MICROCONTROL IN EXECUTING A NUMBER OF DIFFERENT MICROINSTRUCTIONS AS DESCRIBED. EACH OF THESE MICROINSTRUCTIONS RESULTS IN SETTING THE REQUEST FLIP-FLOP. IN ADDITION, THE TYPE OF MICROINSTRUCTION ISSUED DETERMINES WHETHER THE DATA FETCHED IS PLACED IN THE SIR OR THE SDR. THAT IS, THE ACCESSED DATA IS PLACED IN THE SIR IF AN IFETCH OR AN SARI INSTRUCTION IS GIVEN. THE DFETCH AND THE SARD CAUSE THE DATA TO BE PLACED IN THE SDR. THE MAJOR DIFFERENCE IN THESE TWO PAIRS OF MICROINSTRUCTIONS IS THAT THE FIRST PAIR SET THE I.D FLIP-FLOP AND THE LAST PAIR CLEARS IT.

WHEN THE MICROINSTRUCTION HAS SET THE REQUEST FLIP-FLOP AND HAS DETERMINED THE STATE OF THE I.D FLIP-FLOP, THE CIRCUITRY WITHIN THE PBC MUST THEN

(A) CLEAR THE DR

(B) GATE THE SAR TO THE PA IF THE I.D=1 (INSTRUCTION MODE) TO ALLOW THE PA+1 LOGIC TO OPERATE.

TO AVOID A RACE CONDITION, BOTH OF THESE ACTIONS ARE INITIATED ON THE TRAILING EDGE OF THE MICROINSTRUCTION CONTROL SIGNAL THAT SETS THE REQUEST FLIP-FLOP. THIS TRAILING EDGE SETS A CONTROL FLIP-FLOP (PULREQ) THAT IS SUBSEQUENTLY CLEARED BY THE NEXT P2 CLOCK PHASE (SEE COMPOSITE DIAGRAM 5). IT IS THE OUTPUT OF THIS FLIP-FLOP THAT CLEARS THE OR AND, IF THE I.D EQUALS 1, ALSO GATES THE SAR TO THE PA.

AT THIS POINT, ASSUME AN IFETCH IS USED TO INITIATE A MEMORY REQUEST SINCE THE OPERATION OF THE PBC IS ALMOST IDENTICAL (APART FROM THE SETTING OR CLEARING OF THE I.D FLIP-FLOP) FOR EACH OF THE MICROINSTRUCTIONS THAT ISSUE STORE REQUESTS. THE MICROCONTROL, HAVING SET THE REQUEST FLIP-FLOP WITH IFETCH, IS THEN FREE TO CONTINUE EXECUTING MICROINSTRUCTIONS. WITH THE REQUEST FLIP-FLOP SET, THE OR CLEARED, AND THE SAR GATED TO THE PA, THE NEXT FUNCTION OF THE PBC IS TO SET THE SIEZE AND GO FLIP-FLOPS. BEFORE THIS FUNCTION CAN BE PERFORMED, THE PBC LOGIC MUST CHECK THE PRESENT STATE OF THE MASB. IF THE MASB IS IN USE BY EITHER A UNIT OF LOWER PRIORITY OR A PREVIOUS REQUEST, THE PBC MUST WAIT. IN ADDITION, ONLY THE ACTIVE PBC SETS ITS SEIZE AND GO FLIP-FLOPS. THE ACTIVE PBC IS DEFINED BY THE IDL BIT FROM THE MMS FOR READ COMMANDS OR IF A WRITE COMMAND IS BEING ISSUED AND THE UPDATE MODE IS SET BOTH PBC'S WILL BE ACTIVATED. NOTE THAT ALL OTHER FUNCTIONS PERFORMED TO THIS POINT IN TIME ARE DUPLICATED IN BOTH PBC'S INDPENDENTLY OF WHICH ONE IS ACTIVE. THERE ARE THREE BUS SIGNALS THAT MUST BE MONITORED TO ENSURE THE MASB IS IDLE.

CIRCUIT OPERATION (CONT)

(A) THE FIRST IS THE SCM SIGNAL. THIS SIGNAL WILL BE BUSY IF THE PREVIOUS MEMORY REQUEST ISSUED BY THE SAME 3A CC HAS NOT COMPLETED. NOTE THAT WHEN THE DR IS SET AT THE END OF A MEMORY CYCLE, IT IS STILL NECESSARY FOR THE 3A CC TO INDICATE TO THE MASC THAT THE SCM HAS BEEN RECEIVED (i.e., GO BECOMES INACTIVE). IN TURN, THE MASC MUST INDICATE TO THE 3A CC THAT IT HAS IDLED ITSELF AND IS READY FOR THE NEXT MAS REQUEST (SCM BECOMES INACTIVE). SERC MUST ALSO BE CHECKED, AS IT HAS THE SAME TIMING AS SCM.

(B) THE SECOND BUS SIGNAL THAT MUST BE CHECKED BEFORE ISSUING A MEMORY REQUEST IS THE INCOMING SG0 SIGNAL FROM UNITS OF LOWER PRIORITY. IF A UNIT OF LOWER PRIORITY HAS SG0 ACTIVE, THE PBC MUST WAIT UNTIL BOTH THE INCOMING SG0 AND THE INCOMING SCM ARE IDLE (i.e., THE LOWER PRIORITY UNIT HAS FINISHED ITS MEMORY REQUEST). NOTE THAT, AS SEEN ON THE MASB, THE START OF A MEMORY CYCLE IS INDICATED BY THE ARRIVAL OF AN ACTIVE SG0 LEAD AND THE COMPLETION OF THAT SAME MEMORY CYCLE IS INDICATED BY THE ARRIVAL OF AN INACTIVE SCM LEAD. AS SOON AS THE SCM SIGNAL BECOMES IDLE, THE PBC WILL ISSUE ITS OWN MAS REQUEST. THE FACT THAT THE PBC MUST ALWAYS LOOK AT THE INCOMING SG0 SIGNAL ON THE MASB BEFORE ISSUING AN MAS REQUEST ENSURES THAT IF MORE THAN ONE UNIT IS ACCESSING THE SAME MAS, THEY WILL INTERLEAVE THEIR REQUESTS.

(C) THE THIRD LEAD THAT THE PBC MUST CHECK BEFORE ISSUING AN MAS REQUEST OUT ONTO THE MASB IS THE STORE REQUEST (SREQ) LEAD (DO NOT CONFUSE THIS LEAD WITH THE REQUEST FLIP-FLOP). THE SREQ LEAD ALLOWS THE LOWER PRIORITY UNITS ATTACHED TO THE MASB (FURTHER AWAY FROM THE STORE) TO OBTAIN EXCLUSIVE USE OF THE MASB. IN THIS WAY, A LOWER PRIORITY UNIT CAN PERFORM A NUMBER OF CONSECUTIVE MEMORY REQUESTS WITHOUT BEING INTERRUPTED.

ONCE A BUS BECOMES IDLE, THE SEIZE AND GO FLIP-FLOPS ARE SET AND A MEMORY REQUEST IS INITIATED OUT ONTO THE BUS TO THE MASB. NOTE THAT THE CLEARING OF THE DR AND THE GATING FROM THE SAR TO PA IS A SYNCHRONOUS FUNCTION RELATIVE TO THE 3A CC CLOCK, HOWEVER, THE SETTING OF THE GO AND SEIZE FLIP-FLOPS, ONCE THE REQUEST FLIP-FLOP IS SET, IS NOT. THEREFORE, THE CLEARING OF THE DR COULD TAKE PLACE BEFORE OR AFTER THE GO FLIP-FLOP IS SET. THE FACT THAT THE DR IS NOT CLEARED UNTIL LATE IN A MICROCYCLE IS THE REASON WHY THE MICROCODE CANNOT ISSUE A STORE REQUEST ON ONE MICROCYCLE BEFORE TESTING THE OR. THE SETTING OF THE SEIZE FLIP-FLOP GUARANTEES THAT, DURING A MEMORY CYCLE, LOWER PRIORITY UNITS WILL NOT AND CANNOT INTERFERE.

THE SETTING OF THE GO FLIP-FLOP, WHICH IN TURN DRIVES THE SG0 LEAD ON THE MASB, IS USED TO SIGNAL TO THE MASC THAT THE ADDRESS AND 2-OUT-OF-4 CONTROL LEADS ON THE MASB ARE STABLE. IT IS THE ARRIVAL OF THE SG0 SIGNAL AT THE MASC THAT INITIATES AN MAS CYCLE WITHIN THE MASC AND MAS. IN THE CASE OF THE IFETCH, THE ADDRESS IS LOADED BY GATING THE OUTPUT OF THE PA+1 LOGIC INTO THE SAR SIMULTANEOUSLY WITH THE SETTING OF THE REQUEST FLIP-FLOP. THE LOGIC DELAYS ARE SUCH THAT THE ARRIVAL OF THE STORE ADDRESS SIGNALS WILL NOT LAG THE SG0 SIGNAL BY MORE THAN 40 ns (MAXIMUM). THIS POSSIBLE TIME LAG IS ACCOUNTED FOR WITHIN THE MASC AND REPRESENTS THE MAXIMUM LAG OF DATA (IF A WRITE), CONTROL, AND ADDRESS WITH RESPECT TO THE SG0 SIGNAL.

THE NEXT SEQUENCIAL FUNCTION OF THE PBC IS TO CONTINUALLY MONITOR THE MASB FOR THE STORE COMPLETION (SCM) SIGNAL. THIS MONITORING IS PERFORMED ON A "SAMPLING" BASIS, ONCE PER MICROCYCLE AS INDICATED IN COMPOSITE DIAGRAM 3. AT THE START OF EACH CLOCK PHASE P2, THE STATE OF THE SCM LEAD IS STROBED INTO THE ENSCM (ENABLE SCM) FLIP-FLOP. THEN, ON CLOCK PHASE P3, THE STATE OF THE ENSCM FLIP-FLOP IS GATED INTO THE OR FLIP-FLOP AND THE ENREL FLIP-FLOP. THE REASONS FOR THE TWO LEVELS OF SAMPLING ARE:

(A) TO ALLOW THE RECOVERY OF THE ENSCM FLIP-FLOP TO A STABLE STATE IF THE SCM LEAD HAS BEEN SAMPLED ON OR NEAR A TRANSITION

(B) TO PROVIDE THE ABILITY TO SYNCHRONIZE THE TWO PBC'S WHICH BOTH RESPOND TO THE SCM. THAT IS, BOTH OR0 AND OR1 AND ENREL0 AND ENREL1 ARE SET TO RESPONSE TO A SCM SIGNAL FROM ONE MAS OR THE OTHER OR BOTH.

WITH THE OR'S SET, THE MICROCODE IS FREE TO USE THE DATA ACCESSED. IN THIS CASE, AN IFETCH MICROINSTRUCTION WAS ISSUED AND, THEREFORE, THE DATA FETCH IS TYPICALLY THE NEXT 0P CODE TO BE EXECUTED. IF THE MICROCONTROL HAS FINISHED EXECUTING THE PREVIOUS 0P CODE AND HENCE HAS REACHED THE ALL-ZEROS LOOP, THE SETTING OF THE OR'S CAUSES THE CONTENTS OF THE SIR TO BE GATED INTO THE IB AND THE MAR (ALSO THE RAR FOR CHECKING PURPOSES). IF THE MICROCONTROL HAS NOT REACHED THE ALL-ZEROS LOOP, THE UNLOADING OF THE SIR IS DELAYED WITH

CIRCUIT OPERATION (CONT)

EXACTLY THE SAME OPERATION BEING PERFORMED AT SOME MICROCYCLE LATER.

CONCURRENT WITH THE MICROCONTROL OPERATION, THE SETTING OF THE ENREL FLIP-FLOPS ALSO CLEARS THE RESPECTIVE GO FLIP-FLOP. THE CLEARING OF THE GO FLIP-FLOP IN TURN DEACTIVATES THE SG0 SIGNAL ON THE MASB BEING USED. THIS INDICATES TO THE MASC THAT THE 3A CC HAS BUFFERED THE DATA (IF A READ CYCLE) AND IS PREPARING TO SEND ANOTHER REQUEST. THE MASC IN TURN RESPONDS BY DEACTIVATING SCM. WHEN THE PBC RECEIVES THE LATTER MASB SIGNAL, IT RESETS ITSELF AND PREPARES TO ISSUE THE NEXT STORE REQUEST.

THE ENREL FLIP-FLOP CANNOT BE CLEARED UNTIL THE SEIZE FLIP-FLOP IS CLEARED. IN THIS WAY, NO NEW MAS REQUESTS CAN BE ISSUED BY THE 3A CC UNTIL THE ENREL IS CLEARED. THE CLEARING OF THE SEIZE FLIP-FLOP IS CONTROLLED BY THE MASC REMOVING THE SCM SIGNAL. THIS INDICATES THAT THE MASC IS IDLE AND IS READY FOR THE NEXT STORE REQUEST.

IF A WRITE TO BOTH MAS'S IS BEING PERFORMED (UPDATE) BOTH COPIES OF THE SEIZE AND THE GO FLIP-FLOP WILL BE SET. HOWEVER, SINCE THE SETTING OF A PBC'S SEIZE FLIP-FLOPS IS DEPENDENT ON THE STATE OF ITS RESPECTIVE MASB, THE TWO PBC'S WILL NOT NECESSARILY ISSUE MAS REQUESTS SIMULTANEOUSLY TO THEIR MAS'S. AT THE COMPLETION OF THE CYCLE, BOTH MAS'S MUST RESPOND WITH THEIR SCM SIGNALS BEFORE THE DR FLIP-FLOPS GET SET. ALSO, BOTH MAS'S MUST RETURN TO THEIR IDLE CONDITION (i.e. SCM = 0) BEFORE THE WRITE CYCLE TO BOTH MAS'S WILL TERMINATE (i.e. BOTH SEIZE FLIP-FLOPS RESET). THE PURPOSE OF THE OW (DOUBLE STORE WRITE) FLIP-FLOP IS TO INSURE THAT THE SEIZE FLIP-FLOPS IN THE RESPECTIVE PBC'S ARE NOT RESET UNTIL BOTH MAS'S HAVE RETURNED TO THEIR IDLE CONDITION.

ANOTHER CHARACTERISTIC OF THE PBC IS THE MANNER IN WHICH IT RELEASES CONTROL OF THE MASB WITH RESPECT TO AN INCOMING BUS REQUEST ON THE BUS REPEATER INPUT. THAT IS, THE PBC MUST RELEASE THE MASB SO THAT THE INCOMING ADDRESS, DATA, AND CONTROL INFORMATION FROM A UNIT OF LOWER PRIORITY MAINTAIN THEIR PHASE RELATIONSHIP WITH THEIR RESPECTIVE SG0 SIGNAL. THIS IS DONE BY USING THE OUTPUT OF THE GO FLIP-FLOP, WHEN CLEARED, TO ALLOW THE BUS REPEATED TO SEND ON THE ADDRESS, DATA, AND CONTROL. WHEN THE SEIZE FLIP-FLOP IS CLEARED AT THE VERY END OF THE CYCLE, IT IS USED TO ENABLE THE SG0 SIGNAL IN THE BUS REPEATER.

ONE OTHER AUTONOMOUS OPERATION THAT IS PERFORMED BY THE PBC IS THE CLEARING OF THE R.W FLIP-FLOP AT THE END OF ALL-DATA CYCLES (I.D EQUALS 0). THAT IS, THE PBC IS FORCED BACK INTO THE READ MODE AT THE END OF ANY MEMORY CYCLE THAT ISSUES A DATA WRITE. THE RETURN TO THE READ MODE (i.e., CLEARING THE R.W FLIP-FLOP) IS PERFORMED WHEN THE DR IS SET IN THE RESPECTIVE MEMORY CYCLE.

TABLE 8

TO- AND FROM-FIELD DECODER

FUNCTION	TO FIELD		FROM FIELD	
	NETNAME(PIN NO.)		NETNAME (PIN NO.)	
SARI	T204LCDB(015)	T204R50C(117)	——	——
SARD	T204LC0B(015)	T204R30C(215)	——	——
OFETCH (STSEQ)	T204L30B(016)	T204RC0C(116)	F204LC0B(216)	F204RA0B(115)
BR=>MMS	T204LC0B(015)	T204RA0B(315)	F204LC0B(216)	F204RA0B(115)
MMS=>GB	——	——	F204L90B(217)	F204RA0B(115)
START PBC (COMPLEMENT CORRECTION)	T104L10B(314)	T304RB0B(10?)	F204LC0B(216)	F204RA0B(115)
SET SEIZE & GO (SSEIZE)	T204LC0B(015)	T204RC0C(116)	F204LC0B(216)	F204RA0B(115)

PART OF FS 4

3A CENTRAL CONTROL

②

DWG SIZE 65

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4GJ

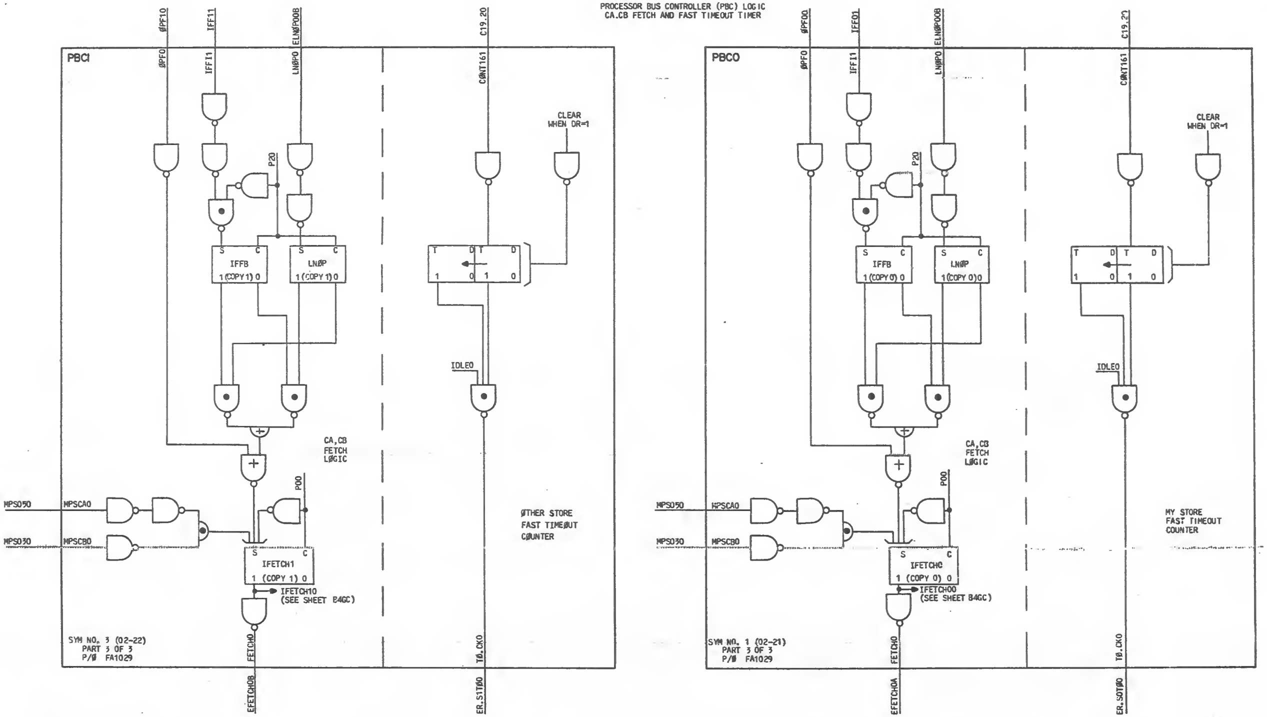
PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 7

PROCESSOR BUS CONTROLLER (PBC) LOGIC
CA.CB FETCH AND FAST TIMEOUT TIMER

CIRCUIT OPERATION
(SEE SHEET B4GL)



PART OF FS 4
COMPOSITE DIAGRAM 7

3A CENTRAL CONTROL
②

DWG SIZE
6S

ISSUE
5A

BELL LABORATORIES
SD-1C900-01
B4GK

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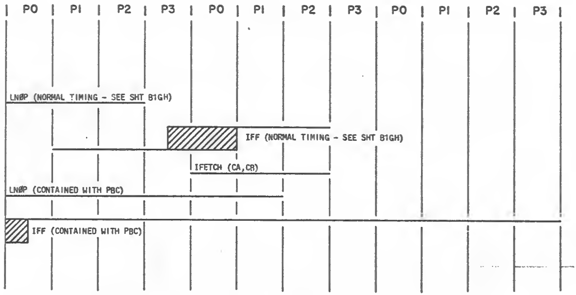
PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 8

SPECIAL TIMING OF THE IFF
TO BLOCK THE IFETCH ON THE SECOND HALF WORD OF A NO.2B INSTRUCTION



P0
P1
P2
P3
P0
P1
P2
P3
P0
P1
P2
P3
LNØP (NORMAL TIMING - SEE SHT B1GH)
IFF (NORMAL TIMING - SEE SHT B1GH)
IFETCH (CA,CB)
LNØP (CONTAINED WITH PBC)
IFF (CONTAINED WITH PBC)

CIRCUIT OPERATION

THE CA, CB FETCH LOGIC SHOWN IN COMPOSITE DIAGRAM 7 IS IMPLEMENTED TO DECODE THE CA, CB CONTROL BITS FOR THE ONE BINARY COMBINATION THAT IS USED TO ISSUE A MAS REQUEST. NOTE THAT DECODING IS ALSO PERFORMED IN FS 1 (SEE SHEET B1C5) BUT IT IS PERFORMED IN THE PBC AS WELL, TO MINIMIZE THE TIME REQUIRED TO ISSUE AN IFETCH ORDER TO THE MAS.

IN ADDITION, THERE IS A REDUNDANT COPY OF THE IFF SO AS TO PROVIDE THE ABILITY TO CORRECTLY ISSUE THE IFETCH ORDER WHEN THE 3A CC IS USED FOR THE NO.2B ESS APPLICATION (OP CODE FIL BIT IS SET [ØPF=1]). AS DETAILED IN FS 11 EACH TIME A NO.2 HALF WORD COMMAND IS LOADED FROM THE SIR, SIR0 OR SIR1, THE IFF IS TOGGLED. ALSO EACH TIME AN ØP CODE IS EXECUTED, AN IFETCH IS GIVEN. SINCE ONLY ONE IFETCH ORDER CAN BE GIVEN PER TWO HALF WORD COMMANDS EXECUTED, THE IFETCH MUST BE INHIBITED FOR HALF OF THE IFETCH ORDERS. THE IFETCH ORDER IS INHIBITED WHEN THE HALF WORD INSTRUCTION ORIGINATES FROM SIR1. THE INHIBIT FUNCTION REQUIRES SOME SPECIAL TIMING AS SHOWN IN COMPOSITE DIAGRAM 8 SINCE THE IFF CHANGES STATE AT ABOUT THE SAME TIME THE IFETCH IS ISSUED. THE PURPOSE OF THE CIRCUITRY SHOWN IN COMPOSITE DIAGRAM 7 IS TO ESSENTIALLY FORCE THE IFF FLIP-FLOP COPY CONTAINED IN THE PBC (IFFB) TO CHANGE STATE BEFORE THE IFETCH IS ISSUED.

PART OF FS 4
COMPOSITE DIAGRAM 8

3A CENTRAL CONTROL ②

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B4GL

PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 9

DOUBLE STORE READ LOGIC AND PART OF COMPLEMENT CORRECTION LOGIC

CIRCUIT OPERATION
(SEE SHEET B4GN)

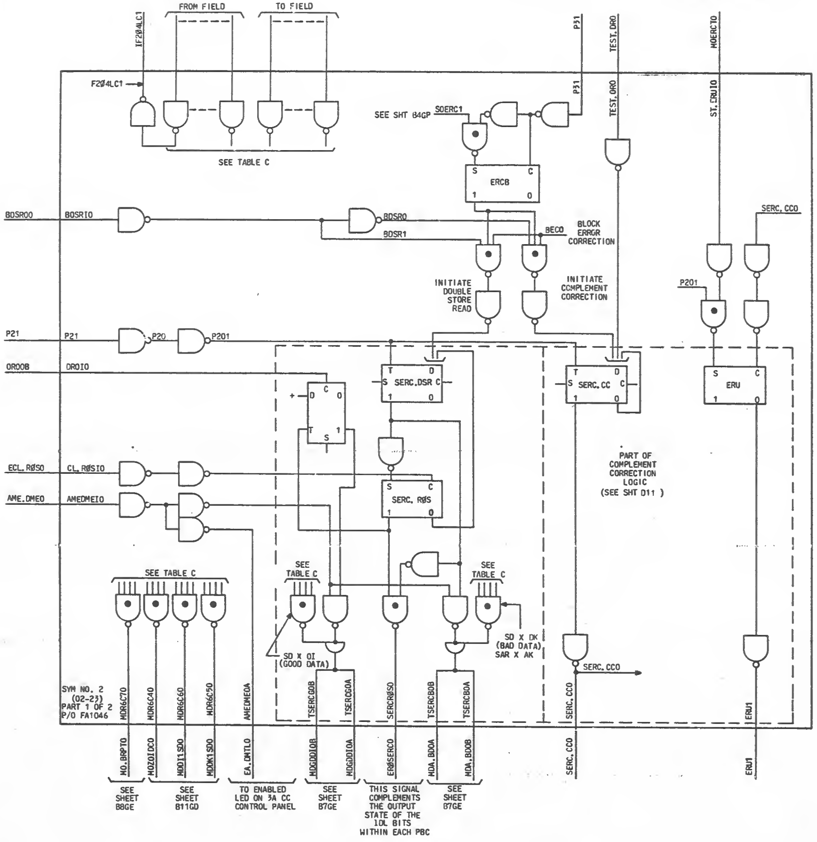


TABLE C

TO- AND FROM-FIELD OECODER ASSIGNMENT				
FUNCTION	TO FIELD		FROM FIELD	
	NETNAME(PIN NO.)		NETNAME(PIN NO.)	
BR X PT	T304LEO(101)	T104R80(301)	F204LCOB(110)	F204R90B(310)
ZDI.DK	T304LOO(201)	T104R80(301)	F204LCOB(110)	F204R90B(310)
OK1 X SDR1	T304LBOB(001)	T104R80(301)	F204LCOB(110)	F204R90B(310)
OI1 X SDRI	T304L70(305)	T104R80(301)	F204LCOB(110)	.204R90B(310)

PART OF FS 4
COMPOSITE DIAGRAM 9

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	8A

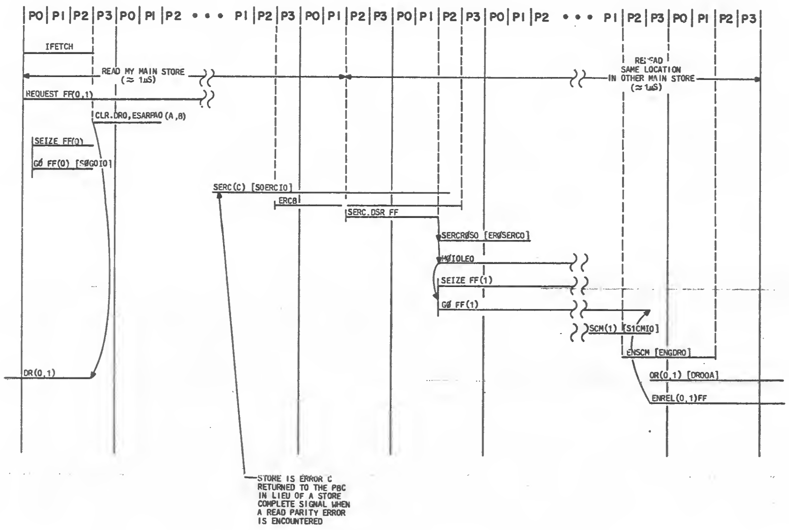
BELL LABORATORIES
SD-IC900-01
B4GM

PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 10

DOUBLE STORE READ TIMING WHEN A READ PARITY ERROR
IS DETECTED IN A 3A CC ASSOCIATED MAIN STORE (i.e. MAIN STORE)


P0 | P1 | P2 | P3 | P0 | P1 | P2 • • • P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 • • • P1 | P2 | P3 | P0 | P1 | P2 | P3
IFETCH
READ MY MAIN STORE (≈ 1µS)
REQUEST FF(0,1)
CLR.DR0,ESARPA0 (A,B)
SEIZE FF(0)
GØ FF(0) [SØGOI0]
SERC(C) [S0ERCI0]
ERCB
SERC.DSR FF
SERCRØS0 [ERØSERC0]
MØIOLE0
SEIZE FF(1)
GØ FF(1)
SCM(1) [S1CMI0]
ENSCM [ENGDR0]
REREAD SAME LOCATION IN OTHER MAIN STORE (≈ 1µS)
OR(0,1)
OR(0,1) [DR00A]
ENREL(0,1)FF

STORE IS ERROR C RETURNED TO THE PBC IN LIEU OF A STORE COMPLETE SIGNAL WHEN A READ PARITY ERROR IS ENCOUNTERED

CIRCUIT OPERATION

A NORMAL READ IS ISSUED BY THE ON-LINE 3A CC TO ITS ASSOCIATED STORE VIA PBC. THEREFORE, AS SHOWN IN COMPOSITE DIAGRAM 16, IF CC0 IS ON-LINE, THE READ IS ISSUED VIA PBC0 TO MAS0. THE PBC ASSOCIATED WITH THE OFF-LINE STORE (PBC1) DOES NOT ISSUE A READ COMMAND OUT ONTO ITS ASSOCIATED STORE BUS. IT DOES, HOWEVER, DUPLICATE MANY OF THE FUNCTIONS FOR THIS READ CYCLE THAT ARE PERFORMED IN PBC0. IN FACT, THE ONLY FUNCTION THAT IS NOT PERFORMED IN THIS PBC IS THE SETTING OF THE "GO" AND THE "SEIZE" FLIP-FLOPS (SEE SHEET B4GD, B4GE, AND B4GF). THE IDL FLIP-FLOP DETERMINES WHICH PBC IS INACTIVE.

THE IMPLEMENTATION OF THE DSR TECHNIQUE USES THE RECEPTION OF THE STORE ERROR C (SERC) SIGNAL TO REVERSE THE "OUTPUT" STATE OF IDL FLIP-FLOP TO REDIRECT THE READ THAT IS FIRST GIVEN TO THE ON-LINE STORE OVER TO THE OFF-LINE STORE. THE SERC SIGNAL INDICATES THAT A PARITY ERROR WAS DETECTED ON A READ COMMAND AND THE MASC SENDS THIS SIGNAL TO THE 3A CC IN LIEU OF A SCM SIGNAL. WHEN THE READ IS REDIRECTED AT THE OFF-LINE STORE, THE PBC GATES THE ACCESSED DATA FROM THE "OTHER" MAIN STORE BUS INTO THE SIR OR THE SDR (AS DEFINED BY ORIGINAL READ WHEN IT SETS OR CLEARS THE ID FLIP-FLOP). THE CYCLE IS COMPLETED BY THE SCM SIGNAL FROM THE OFF-LINE STORE. THERE IS NO INDICATION TO THE 3A CC THAT THE DATA IS ACCESSED CAME FROM THE OFF-LINE STORE (EXCEPT THAT ER BIT 10 IS SET AND THE EFFECTIVE READ TIME IS 2µs INSTEAD OF 1µs. THE NEXT SUCCESSIVE 3A CC READ IS AGAIN TO THE ON-LINE STORE. THIS WILL CONTINUE UNTIL ANOTHER STORE ERROR IS ENCOUNTERED.

SINCE THE STORE ERROR C SIGNAL IS ASYNCHRONOUS TO THE 3A CC IT IS FIRST STROBED INTO THE ERCB BUFFER. THE OUTPUT OF THIS BUFFER IS THEN ROUTED TO EITHER THE DSR LOGIC OR THE COMPLEMENT CORRECTION LOGIC DEPENDING UPON THE STATE OF THE BDSR (BLOCK DSR) BIT. THE BDSR BIT IS CONTROLLED BY SYSTEM SOFTWARE AND IT IS TYPICALLY CLEARED TO ENABLE DSR WHEN THE SYSTEM IS IN THE UPDATE MODE. WHEN THE SYSTEM IS NOT IN UPDATE MODE THE BDSR BIT IS SET AND COMPLEMENT CORRECTION IS USED (SEE SHEET D11 AND D12 FOR DETAILED DESCRIPTION OF COMPLEMENT CORRECTION).

IF DSR IS INVOKED THE SERC.DSR FLIP-FLOP IS SET AT CLOCK PHASE P2 (SEE COMPOSITE DIAGRAM 10). THEN THE OUTPUT OF SERC.DSR IS USED TO SET THE SERC.RØS FLIP-FLOP. NOTE THAT SERC.DSR IS CLEARED ON THE NEXT P2 CLOCK PHASE. THE INTERVAL DURING WHICH THE SERC.DSR IS SET IS USED TO GATE THE BAD DATA AND THE ADDRESS OF THAT BAD DATA INTO THE DK AND AK REGISTERS (SEE SHEETS B7GE AND B11GD), RESPECTIVELY VIA THE OUTPUT TERMINALS TSERCB0 (A,B). THE OUTPUT OF THE FLIP-FLOP SERC.RØS, VIA THE NET ERØSERC0, IS USED TO COMPLEMENT THE OUTPUT OF THE IDL BITS (SEE COMPOSITE DIAGRAM 2, B1 AN B2). IN SO DOING, IT REDIRECTS THE READ REQUEST TO THE OFF-LINE MAS (i.e. ACTIVATES PBC1); THE ERØSERC0 SIGNAL ALSO INITIALIZES PBC0 BY CLEARING THE GØ AND SEIZE FLIP-FLOPS (SEE COMPOSITE DIAGRAM 3, D9). WHEN THIS READ IS COMPLETED, THE SEIZE FLIP-FLOP AND THE ENREL FLIP-FLOP FROM PBC1 RESULT IN ENABLING THE NET ECL.RØS0. NOTE THAT THE COMPLETION OF THE REREAD TO THE OFF-LINE IS PERFORMED IN EXACTLY THE MANNER DESCRIBED FOR A NORMAL READ COMMAND. THIS SIGNAL WILL CLEAR THE SERC.RØS FLIP-FLOP AND, AS A RESULT, END THE DSR READ CYCLE. THE GOOD DATA THAT IS RETURNED ON THE DSR IS GATED, IN ADDITION TO ITS NORMAL DESTINATION OF THE SIR OR SDR, TO THE DI REGISTER FOR ERROR ANALYSIS DATA COLLECTION VIA OUTPUT TSERCG0(A,B). NOTE THAT THE SAVING OF THE GOOD AND BAD DATA AND THE ADDRESS DURING A DOUBLE STORE READ IS INHIBITED IF THE AME AND/OR DME BITS IN THE SYSTEM STATUS REGISTER ARE SET (INPUT AMEDMEI0). THIS ALLOWS THE SYSTEM SOFTWARE TO USE THE ADDRESS AND/OR DATA MATCHERS FOR UTILITY OPERATIONS WHILE IN THE DOUBLE STORE READ MODE.

ALSO CONTAINED IN COMPOSITE DIAGRAM 9 IS TO-FIELD AND FROM-FIELD DECODING THAT IS USED TO GENERATE SOME MISCELLANEOUS DECODER CONTROL POINTS TO PERMIT MAINTENANCE ACCESS OF THE DSR DATA COLLECTION LOGIC SHOWN ON SHEET B7GE.

PART OF FS 4
COMPOSITE DIAGRAM 10

3A CENTRAL CONTROL ②

DWG SIZE
ES

ISSUE
5A

BELL LABORATORIES
SD-1C900-01
B4GN

PART OF FS 4

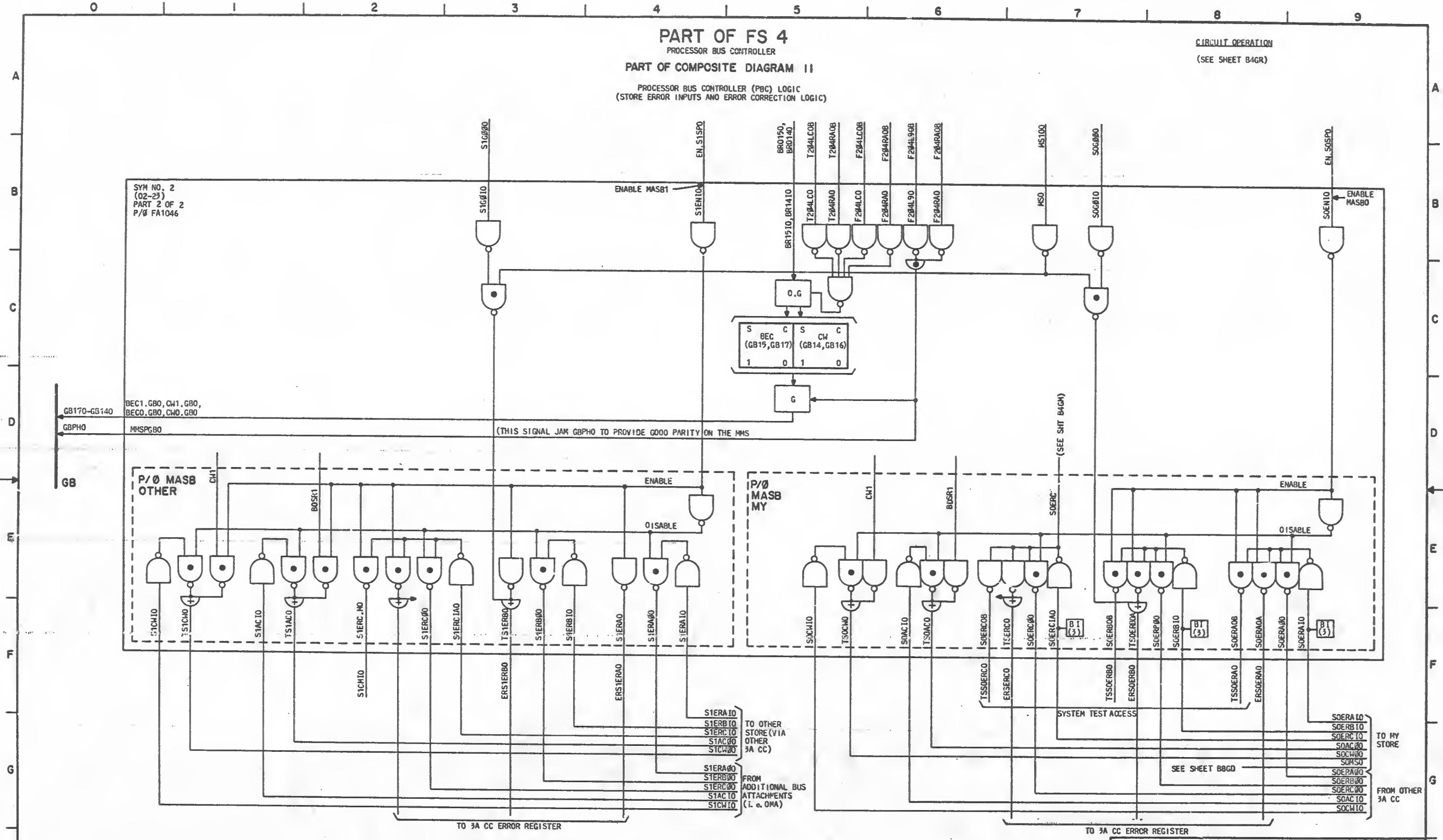
PROCESSOR BUS CONTROLLER

PART OF COMPOSITE DIAGRAM 11

PROCESSOR BUS CONTROLLER (PBC) LOGIC
(STORE ERROR INPUTS AND ERROR CORRECTION LOGIC)

CIRCUIT OPERATION

(SEE SHEET B4GR)



PART OF FS 4
PART OF COMPOSITE DIAGRAM 11

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 8A
BELL LABORATORIES	SD-1C900-01	B4GP

E-7521 (12-73)

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PART OF FS 4

PROCESSOR BUS CONTROLLER

PART OF COMPOSITE DIAGRAM 11

PROCESSORS BUS CONTROLLER (PBC) LOGIC
(STORE ERROR INPUTS AND ERROR CORRECTION LOGIC)

CIRCUIT OPERATION

COMPLEMENT CORRECTION

WHEN NOT IN THE DSR MODE (i.e., NOT IN THE UPDATE MODE) AND A SINGLE PARITY ERROR IS DETECTED, THE MASC WILL ISSUE A SERC SIGNAL IN LIEU OF AN SCM SIGNAL. THE SERC SIGNAL TOGETHER WITH THE BLOCKED DSR MODE (BDSR=1) WILL CAUSE THE 3A CC TO INVOKE A MICROSUBROUTINE TO PERFORM COMPLEMENT CORRECTION, (SEE SHEET D11 & D12). THE COMPLEMENT CORRECTION MICROCODE WILL PERFORM THE FOLLOWING FUNCTIONS:

- (A) SAVE PRESENT STATE OF MAR IN ERAR AND START COMPLEMENT CORRECTION
- (B) SAVE THE PRESENT STATE OF THE MMS
- (C) SAVE THE PRESENT STATE OF THE BR
- (D) LOAD THE MMS (WHICH ALSO INITIALIZES THE PBC) WITH THE FOLLOWING FUNCTIONS ACTIVE:
  - (1) NORMAL WRITE
  - (2) LOCK STATE
  - (3) ISOLATE
  - (4) COMPLEMENT WRITE MODE
  - (5) ACTIVATE PBCO
- (E) ISSUE A START PBC
- (F) TEST FOR COMPLETION OF THE MEMORY CYCLE
- (G) RELOAD THE MMS REGISTER WITH THE ORIGINAL CONTENTS
- (H) RELOAD THE BR REGISTER
- (I) ISSUE A START PBC
- (J) RETURN FROM COMPLEMENT CORRECTION MICROSUBROUTINE (i.e., ERAR-MAR).

THE NET RESULT OF THE COMPLEMENT CORRECTION MICROSUBROUTINE WILL BE:

- (A) STORE THE COMPLEMENT OF THE FAILING WORD IN ITS RESPECTIVE LOCATION AND BOTH PARITY BITS WILL BE FORCED TO INDICATE A DOUBLE PARITY ERROR CONDITION.
- (B) RETRY THE READ AT THE SAME LOCATION IN THE SAME STORE IN ORDER TO RETRIEVE THE CORRECTED WORD.

IN THIS MODE OF OPERATION, ONCE THE WORD IS CORRECTED, THE COMPLEMENT CORRECTION MICROSUBROUTINE WILL NOT HAVE TO BE INVOKED AGAIN UNLESS THE LOCATION IS REWRITTEN (i.e., NORMAL WRITE TO CALL STORE).

WHEN THE 3A CC'S ARE IN THE BLOCK DSR MODE AND TWO PARITY BIT ERRORS ARE DETECTED BY THE MASC, AUTOMATIC COMPLEMENT CORRECTION IS PERFORMED. MASB SIGNAL. STORE AUTOMATIC CORRECTION (SAC), IS SENT FROM THE 3A CC TO THE MASC TO INDICATE WHETHER AUTOMATIC COMPLEMENT CORRECTION IS REQUIRED, (SEE COMPOSITE DIAGRAM 11).

ANOTHER SIGNAL ADDED TO THE MASB IS THE STORE COMPLEMENT WRITE (SCW) SIGNAL WHICH IS USED IN CONJUNCTION WITH THE ACTUAL WRITING OF THE COMPLEMENT OF THE FAILING WORD BACK INTO MAIN STORE. SPECIAL MASB TIMING IS IMPLEMENTED ON THIS SIGNAL (BECOMES ACTIVE 60ns BEFORE THE SG0 SIGNAL). WHEN THE MASC RECEIVES THIS SCW SIGNAL, IT SAVES THE LAST WORD IT READ OUT OF THE MAIN STORE, COMPLEMENTS IT, AND ON A SUCCEEDING WRITE COMMAND ISSUED BY THE 3A CC WRITES THE COMPLEMENTED WORD INTO THE LOCATION SPECIFIED BY THE SAR.

THE SPECIAL TIMING BETWEEN THE SCW SIGNAL AND THE SG0 SIGNAL IS ACHIEVED BY THE METHOD IN WHICH THE MICROCODE SEQUENCES THE PBC. THE MMS IN THE PBC IS LOADED BY THE MICROPROGRAM CONTROL WITH THE CW BIT SET AND THE IS0 BITS SET. THE ACTIVATION OF THE ISOLATE STATE (RESULT IS THE EXCLUSIVE USE OF THE MEMORY BUS) ALLOWS THE SCW SIGNAL TO FLOW DIRECTLY FROM THE CW BIT IN THE PBC TO THE MASC. THEN ON A SUBSEQUENT CYCLE, THE MICROPROGRAM CONTROL ISSUES A MEMORY REQUEST WHICH IN TURN ACTIVATES THE SG0 SIGNAL. THUS, THE SG0 SIGNAL WILL BE SUFFICIENTLY DELAYED RELATIVE TO THE SCW SIGNAL TO MEET THE 60ns TIMING REQUIREMENT BETWEEN THEM AT THE MASC. NOTE THAT IF THE ISOLATE STATE WAS NOT SET UP ON A PREVIOUS MICROCYCLE, THE SCW SIGNAL AND THE SG0 WOULD ARRIVE AT THE MASC AT ABOUT THE SAME TIME. IN THE CASE OF THE COMPLEMENT CORRECTION MICROSUBROUTINE, THE EXCLUSIVE USE OF THE BUS IS GUARANTEED BY THE FACT THAT THE READ THAT ACTUALLY INCURS THE PARITY ERROR NEVER FINISHES (i.e., NO SCM). HENCE, AS LONG AS THE MMS IS LOADED WITH THE LOCK STATE AND THE ISOLATE STATE DURING THE COMPLEMENT WRITE CYCLE, THE EXCLUSIVE USE OF THE MEMORY BUS IS GUARANTEED.

IN THE CASE WHERE A COMPLEMENT WRITE IS TO BE PERFORMED BY A MACROLEVEL COMMAND (i.e., C0NL OR C0NF) WHILE THE 3A CC IS IN THE DSR MODE, IT IS FIRST NECESSARY TO ISSUE

CIRCUIT OPERATION (CONT)

A READ COMMAND WITH THE LOCK STATE SET IN THE MMS. ONCE THIS READ IS SUCCESSFUL, THE EXCLUSIVE USE OF THE MAIN STORE BUS IS GUARANTEED AND, AS A RESULT, A COMPLEMENT WRITE CAN BE PERFORMED WITH THE SAME PROCEDURE AS THE MICROSUBROUTINE USES (i.e., LOAD MSS WITH NORMAL WRITE, LOCK STATE ISOLATE STATE AND THE COMPLEMENT WRITE STATE).

ERROR DETECTION

THE PBC, LIKE THE REST OF THE 3A CC, IS DESIGNED TO BE SELF-CHECKING. IN ORDER TO ACCOMPLISH THIS, THE FOLLOWING ERROR DETECTION TECHNIQUES ARE USED:

- (A) USE OF THE SELF-CHECKING MICROCONTROL OF THE 3A CC IS USED FOR AS MUCH OF THE CONTROL AND SEQUENCING AS A REAL-TIME EFFICIENT DESIGN WOULD PERMIT.
- (B) DUPLICATION OF MOST OF THE REMAINING CONTROL SEQUENCING LOGIC.
- (C) A PARITY CHECK CODE ON THE ADDRESS AND DATA FIELDS.
- (D) A 2-OUT-OF-4 CODE ON CONTROL LEADS.
- (E) A TIMER TO CHECK THE FUNCTION EXECUTION INTERVAL OF ALL MAIN MEMORY REQUESTS.

THESE ERROR DETECTION TECHNIQUES ARE DIRECTLY ASSOCIATED WITH THE LOGIC OF THE PBC. SINCE THE MASC MUST RECEIVE ADDRESS DATA AND CONTROL FROM THE PBC, THERE ARE ERROR DETECTION CIRCUITS IN THE MASC THAT FIRE IF THE PBC MALFUNCTIONS. IN ADDITION, THE MASC MAS SOME CHECK CIRCUITS THAT ARE DEDICATED TO ITS OWN PROPER OPERATION. THE DETECTION CIRCUITS IN THE MASC CHECK FOR THE FOLLOWING CONDITIONS:

- (A) CORRECT PARITY ON THE ADDRESS DATA SIGNALS SENT TO IT FROM THE PBC
- (B) CORRECT 2-OUT-OF-4 CODE ON THE CONTROL SIGNALS FROM THE PBC
- (C) CORRECT ACCESSING OF WRITE PROTECTED AREAS OF STORE
- (D) CORRECT DATA BEING ACCESSED FROM THE MAS ON READ COMMANDS
- (E) CORRECT OPERATION OF THE MASC TIMING AND CONTROL LOGIC.

ALL OF THE OUTPUTS OF THE CHECK CIRCUITS IN THE MASC ARE RETURNED TO THE 3A CC VIA THREE ERROR SIGNALS SERA, SERB, AND SERC.

IN ADDITION TO THE CHECK CIRCUITS BOTH IN THE PBC AND THE MASC, THERE ARE A NUMBER OF 3A CC CHECK CIRCUITS THAT MAY FIRE IF THE PBC AND THE MASC FAIL TO ACCESS GOOD DATA UPON WHICH THE 3A CC ATTEMPTS TO OPERATE. THESE CHECK CIRCUITS ARE:

- (A) BRANCH ALLOWED (BA) CHECK ERROR
- (B) MAR PARITY ERROR
- (C) IB PARITY ERROR
- (D) GATING BUS PARITY ERROR
- (E) TO- OR FROM-FIELD ERRORS.

THE BA ERROR FIRES IF A BRANCH OCCURS TO A LOCATION IN MAIN MEMORY THAT DOES NOT HAVE BIT 15 OF THAT WORD SET TO ONE. NOTE THAT BIT 15 OF THE FIRST WORD (IF THE INSTRUCTION MAS A 2-WORD FORMAT) OF ALL INSTRUCTIONS IS RESERVED AS A BA CHECK BIT. THE MAR PARITY ERROR, THE IB PARITY ERROR, AND THE GATING BUS PARITY ERROR MAY (DEPENDING ON WHERE IN THE PROCESSOR THE DATA IS USED) FIRE IF DATA WITH BAD PARITY IS PROCESSED WITHIN THE 3A CC. THE TO- AND THE FROM-FIELD ERRORS WOULD FIRE IF BAD DATA WAS USED FOR A MICROINTERPRET INSTRUCTION. IN A MICROINTERPRET INSTRUCTION, THE ACCESSED DATA FROM THE MAS MUST CONSIST OF TWO 4-OUT-OF-8 CODES IN THE 16-BIT DATA WORD.

THE FOLLOWING IS A DESCRIPTION OF THOSE ERROR-DETECTION TECHNIQUES THAT APPLY DIRECTLY TO THE PBC.

1. SELF-CHECKING MICROCONTROL

ALL MAIN MEMORY REQUESTS ORIGINATE FROM THE MICROCONTROL ITSELF. THEREFORE, THE CONTROL SIGNALS TO THE PBC THAT ARE USED TO INITIATE AND TERMINATE A STORE REQUEST ARE ALL CHECKED VIA THE USUAL MEANS (i.e., TO- AND FROM-FIELD 4-OUT-OF-8 CODE CHECKERS). IN ADDITION, IF MICROCONTROL FAILS TO PERFORM THE PROPER SEQUENCING ON THE PBC, THE MICROCONTROL SEQUENCING CHECK CIRCUITS WILL FIRE (i.e., MAR-RAR MISMATCH + MAR PARITY CHECK).

2. DUPLICATION

THE OVERHEAD IN IMPLEMENTING DUPLICATION WAS GREATLY REDUCED BECAUSE A TWO-PORT ACCESS ONTO BOTH MEMORY BUSES, MASB0 AND MASB1, WAS PROVIDED. THE REQUIREMENT OF THE

CIRCUIT OPERATION (CONT)

TWO-PORT ACCESS IS NECESSARY BECAUSE THE 3A CC MUST SIMULTANEOUSLY ISSUE WRITE COMMANDS TO BOTH THE ON-LINE STORE AND THE OFF-LINE STORE WHEN IN THE DUPLEX CONFIGURATION AND IN THE UPDATE MODE. ALTHOUGH A READ CANNOT BE ISSUED SIMULTANEOUSLY TO BOTH STORE BUSES, BOTH PBC'S ARE DESIGNED TO EXECUTE AS MUCH OF THE CONTROL AND SEQUENCING AS POSSIBLE ON ALL READS. THE ONLY FUNCTION THE IDLE PBC CANNOT PERFORM IS THE SETTING OF THE SEIZE AND GO FLIP-FLOPS, SINCE THEY CONTROL THE FLOW IF INFORMATION OUT ONTO THE MASB. THE RESULT IS THAT, WHEN A STORE REQUEST IS ISSUED BY THE MICROCONTROL, THE FINAL STAGE OF DECODING OF THE MICROCONTROL CROSSPOINT, THE SETTING OF THE REQUEST FLIP-FLOP, THE CLEARING OF THE DR, THE SETTING OR CLEARING OF THE I.D FLIP-FLOP AND THE GATING OF THE SAR TO THE PA ARE ALL PERFORMED IN BOTH PBC'S. IF ONE OF THESE FUNCTIONS DOES NOT WORK PROPERLY, THE DESIGN GUARANTEES THAT EITHER THE TWO OR'S WILL GET OUT OF SYNC (CAUSING AN MAR PARITY ERROR) OR INCORRECT PARITY WILL BE LOADED INTO THE ADDRESS REGISTERS (PA OR SAR) AND/OR THE DATA REGISTERS (SIR OR SOR) ASSOCIATED WITH THE PBC.

WHEN A READ CYCLE IS BEING COMPLETED (i.e., ARRIVAL OF AN ACTIVE SCM SIGNAL), THE SETTING OF THE ENGDRO (ENABLE GATTNG TO DR) FLIP-FLOP RESULTS IN THE ACTIVATION OF THE OTHER PBC (SEE COMPOSITE DIAGRAM 3). IN THIS WAY, BY FEEDING THE SCM SIGNAL FROM ONE STORE TO BOTH PBC'S, THE SEQUENCING NEEDED TO TERMINATE A MEMORY CYCLE IS ALSO CHECKED BY DUPLICATION. THE RESULT OF A FAILURE WILL CAUSE THE DR'S TO MISMATCH AND AN MAR PARITY ERROR WILL RESULT. THE SBY SIGNAL IS ALSO FED TO BOTH PBC'S AND, BEFORE EACH PBC CAN BE RESET AT THE END OF A READ CYCLE, BOTH THE SBY AND SCM MUST RETURN TO THEIR IDLE STATES. IF THE PBC CANNOT BE RESET, IT CANNOT INITIATE ANOTHER REQUEST. THE RESULT OF THIS TYPE OF FAILURE WILL TYPICALLY CAUSE THE FAST TIME-OUT TIMER TO FIRE.

WHEN THE UPD BIT IS SET FOR WRITE CYCLES, THE EFFECT OF THE IDL BIT IS NULLIFIED AND BOTH PBC'S PERFORM THE SAME OPERATIONS. THIS INCLUDES THE SETTING OF THE SEIZE AND GO FLIP-FLOPS. NOTE THAT IN THIS CASE, ONE OR BOTH OF THE MASB'S MAY BE BUSY AND, AS A RESULT, A WRITE TO ONE STORE MAY TAKE PLACE AHEAD OF THE OTHER. THIS IS NOT A PROBLEM AND SYNCRONISM IS AGAIN ACHIEVED AT THE 3A CC BY NOT ALLOWING THE PBC'S TO SET THEIR OR FLIP-FLOPS UNTIL BOTH SCM'S HAVE BEEN RECEIVED FROM THE STORES.

WHEN THE PBC'S ARE NOT IN UPDATE MODE, THE CHECKING OF A WRITE TO A SINGLE STORE IS EXACTLY THE SAME AS THE CHECKING OF THE READ. ALSO, IM RESPECT TO THEIR OPERATION AND THEIR CHECKING, THERE IS NO DIFFERENCE IN THE ISSUING OF A READ OR WRITE COMMAND (WHEN NOT IN UPDATE) TO EITHER MY STORE OR THE OTHER STORE, OTHER THAN THE STATE OF THE IDL BIT AND/OR THE R.W BIT.

3. PARITY CHECK CODE

AS HAS BEEN PREVIOUSLY OUTLINED, PARITY IS USED TO CHECK THE CORRECT TRANSMISSION OF THE ADDRESS AND DATA FIELDS THAT IS SENT TO AND FROM THE MASC. THE PARITY CHECK CODE IS SUFFICIENT TO COVER ALL SINGLE CIRCUIT PACK FAILURES (i.e., WILL DETECT MULTIPLE FAILURES WITHIN A CIRCUIT PACK) BY BIT SLICING ALL THE ADDRESS AND DATA LEADS.

THE SAME ADDRESS AND DATA PARITY THAT IS CARRIED WITHIN THE 3A CC IS USED WHEN SENDING ADDRESS AND DATA TO THE MASC. THEREFORE, NO NEW PARITY GENERATION IS REQUIRED WHEN COMMUNICATION IS REQUIRED TO AND FROM THE MASC. IF THE 3A CC SENDS BAD PARITY TO THE STORE STORE ERROR A FIRES. IF THE STORE SENDS DATA TO THE 3A CC WITH BAD PARITY, IT WILL CAUSE ONE OF THE FOLLOWING DEPENDING ON HOW THE DATA IS USED:

- (A) GATING BUS PARITY ERROR (DATA COMMAND)
- (B) MAR PARITY ERROR
- (C) IB PL ERROR (INSTRUCTION FETCH).
- (D) TO OR FROM ERRORS (MICROINTERPRET).

4. 2-OUT-OF-4 CODE ON CONTROL LEADS (SEE COMPOSITE DIAGRAM 2)

SINCE IT IS NOT CONVENIENT TO BIT SLICE THE CONTROL FIELD, A 2-OUT-OF-4 CODE WAS USED TO CHECK THE CONTROL INFORMATION SENT FROM THE 3A CC TO THE MASC. A 2-OUT-OF-4 CODE WILL DETECT ALL SINGLE ERRORS AND ALL MULTIPLE UNIDIRECTIONAL ERRORS AND HENCE IS APPROPRIATE. IF A 2-OUT-OF-4 ERROR IS DETECTED AT THE STORE, STORE ERROR A WILL FIRE.

5. TIMER TO CHECK FUNCTIONAL EXECUTION INTERVAL OF MAIN MEMORY REQUESTS (SEE COMPOSITE DIAGRAM 4)

SOME FAULTS MAY OCCUR THAT RESULT IN A LOCK OF A RESPONSE TO THE INITIAL STORE REQUEST. TO COVER SUCH FAULTS A SO-CALLED "FAST TIMER" IS IMPLEMENTED IN THE 3A CC. THIS TIMER IS ACTIVATED BY THE CLEARING OF THE OR AND WILL FIRE FROM 38 TO 57us AFTER AN MAS REQUEST IS GIVEN IF THE MEMORY CYCLE DOES NOT COMPLETE (i.e., DR IS NOT SET). THE TYPICAL CASES CAUSING THIS TIMER TO FIRE ARE:

- (A) AN OTHER STORE READ WAS ISSUED AND THE OTHER 3A CC WAS IN THE ISOLATE STATE.
- (B) A MALFUNCTION IN THE STORE THAT CAUSED IT NOT TO RESPOND TO A MEMORY REQUEST.
- (C) FAILURE TO SET THE GO OR THE SEIZE FLIP-FLOPS IN THE PBC OF THE 3A CC.
- (D) AN OUT OF RANGE ADDRESS (i.e., UNEQUIPPED STORE) WAS USED TO READ A MEMORY LOCATION (i.e., PROGRAM BUG).

CIRCUIT OPERATION (CONT)

THERE ARE TWO FAST TIMERS ASSOCIATED WITH THE PBC'S. THERE IS ONE FOR "MY" STORE AND ONE FOR THE "OTHER" STORE. THE STORE ASSOCIATED FAST TIMERS ARE A CHECK MECHANISM ON PROPER STORE ACCESS TIME. IF THE FAST TIMER WERE NOT IMPLEMENTED, THE SYSTEM WOULD HAVE TO DEPEND UPON THE PROGRAM TIMER TIME-OUT. THE PROGRAM TIMER IS NOT INTENDED AS A PRIMARY CHECK MECHANISM FOR MOST HARDWARE FAILURES. THE IMPLEMENTATION OF THE TWO FAST TIMERS PERMITS THE USE OF TWO DIFFERENT RECOVERY MECHANISMS DEPENDING UPON WHICH STORE (IE., ON-LINE OR OFF-LINE) DID NOT RESPOND.

6. MAIN STORE ASSOCIATED ERRORS (SEE COMPOSITE DIAGRAM 11)

LIKE THE OUTPUTS OF THE OTHER ERROR CIRCUITS WITHIN THE 3A CC, STORE ASSOCIATED ERRORS ARE COLLECTED AND MONITORED IN THE ER REGISTER IN THE 3A CC. THERE ARE A TOTAL OF EIGHT ERRORS THAT ARE ASSOCIATED DIRECTLY WITH THE STORES IN THE 3A CC. THERE ARE FOUR TYPES OF ERRORS FOR THE ON-LINE STORE AND FOUR EQUIVALENT ERROR TYPES FOR THE OFF-LINE STORE. THEY ARE:

- (A) STORE ERROR A (SERA) - THIS ERROR ORIGINATES FROM THE MASC AND INDICATES AN ERROR IN ANY ONE OF THE CHECK CIRCUITS CONTAINED IN THE MASC EXCEPT THE WRITE PROTECT CHECK (SERB) AND THE READ ERROR PARITY CHECK (SERC). THERE IS ALSO AN ERROR REGISTER IN THE MASC THAT IS USED TO MONITOR THE INDIVIDUAL ERROR CIRCUITS IN THE STORE. THE OUTPUTS OF THIS ERROR REGISTER ARE STORED AND SENT TO THE 3A CC AS STORE ERROR A.
- (B) STORE ERROR B (SERB) - THIS ERROR ORIGINATES FROM THE MASC AND INDICATES THAT AN ATTEMPT HAS BEEN MADE TO WRITE INTO A 4K BLOCK OF MEMORY WHICH HAS BEEN PREVIOUSLY WRITE PROTECTED.
- (C) STORE ERROR C (SERC) - THIS ERROR ORIGINATES FROM THE MASC AND INDICATES THAT A PARITY ERROR HAD BEEN DETECTED ON DATA READOUT OF THE STORE.
- (D) FAST TIME-OUT - THIS CHECK ORIGINATES FROM THE PBC OF THE 3A CC. THIS ERROR INDICATES THAT A MEMORY REQUEST HAS TAKEN TOO LONG TO COMPLETE.

PART OF FS 4
PART OF COMPOSITE DIAGRAM 11

3A CENTRAL CONTROL
2

DWG SIZE 6S
ISSUE 5A

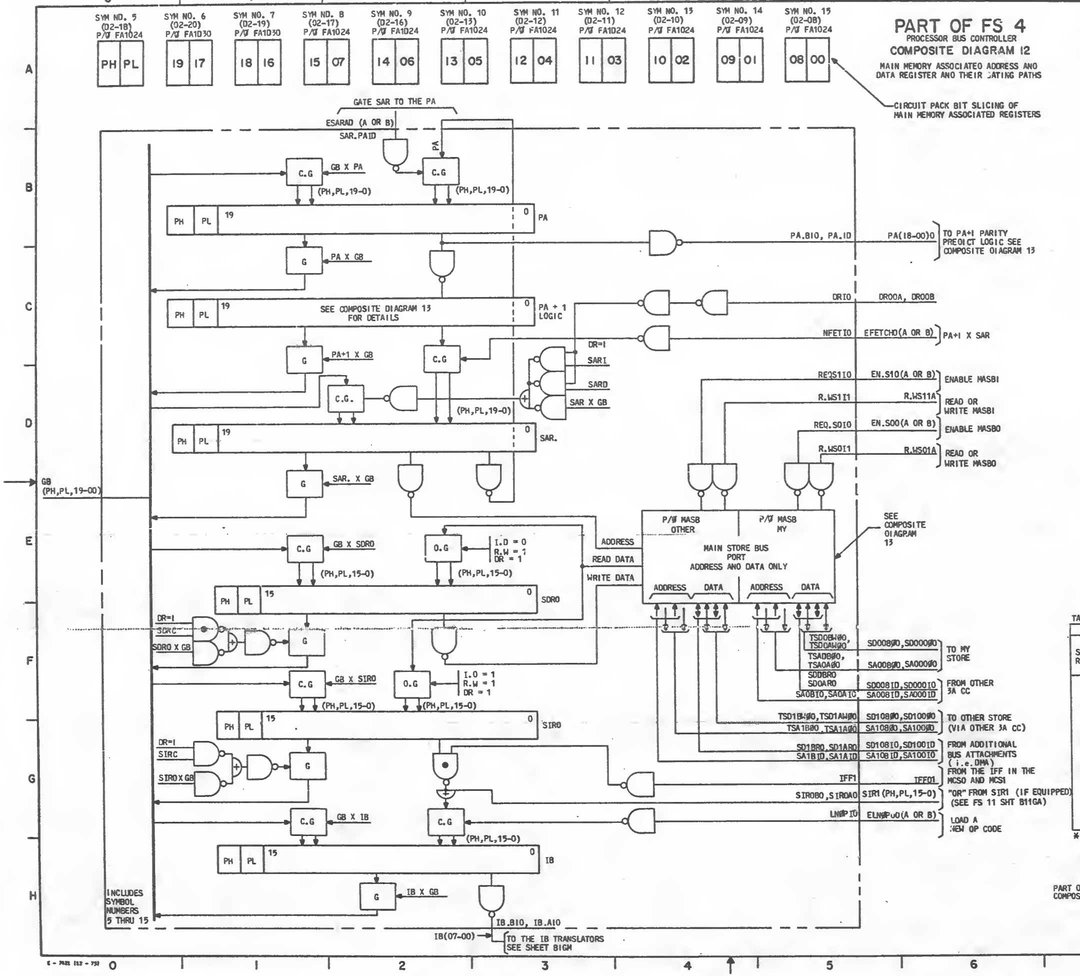
BELL LABORATORIES
SD-1C900-01
B4GR

PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 12

MAIN MEMORY ASSOCIATED ADDRESS AND
DATA REGISTER AND THEIR GATING PATHS



CIRCUIT OPERATION

THE ADDRESS AND DATA PORTION OF THE PBC CONSISTS OF FOUR SPECIALLY DESIGNED REGISTERS THAT ARE USED TO ADDRESS THE MAS AND TO BUFFER DATA TO AND FROM THE MAS. AS SHOWN IN COMPOSITE DIAGRAM 12, THESE REGISTERS ARE:

(A) PA - THE PROGRAM ADDRESS REGISTER IS GENERALLY USED TO SAVE THE LAST ADDRESS FROM WHICH AN INSTRUCTION WAS FETCHED.

(B) SAR - THE STORE ADDRESS REGISTER IS USED TO BUFFER THE ADDRESS OF THE PRESENT MAS REQUEST.

(C) SIR - THE STORE INSTRUCTION REGISTER IS USED TO BUFFER THE INSTRUCTIONS AS THEY ARE FETCHED FROM THE MAS.

(D) SDR - THE STORE DATA REGISTER IS USED TO BUFFER DATA FROM THE MAS ON A READ REQUEST. ON A WRITE REQUEST, IT CONTAINS THE DATA TO BE WRITTEN INTO THE MAS.

(E) IB - THE INSTRUCTION BUFFER IS USED TO BUFFER OR SAVE THE CONTENTS OF THE OP CODE AND THE OPERAND DATA FROM SIR REGISTER, EITHER SIRO OR SIR1, DURING THE EXECUTION OF THAT OP CODE SO THAT THE PBC LOGIC CAN IMMEDIATELY ISSUE THE NEXT MAS REQUEST. NOTE THAT WHICH SIR, 0 OR 1, IS GATED TO THE IB BY THE LNOP SIGNAL IS DETERMINED BY THE IFF. SEE FS 11 FOR ADDITIONAL DETAILS.

IN ADDITION TO THE ADDRESS REGISTERS, PA AND SAR, THERE IS COMBINATIONAL LOGIC ATTACHED DIRECTLY TO THE OUTPUTS OF THE PA REGISTER AND THIS CIRCUITRY IS REFERRED TO AS THE PA+1 LOGIC. THE PA+1 LOGIC IS USED TO INCREMENT THE MAS ADDRESSES FOR REQUESTS TO CONSECUTIVE MAIN MEMORY LOCATIONS (SEE COMPOSITE DIAGRAM 13).

THE TYPICAL MANNER IN WHICH THESE REGISTERS ARE USED IS AS FOLLOWS:

(A) A STARTING ADDRESS IS LOADED INTO THE SAR BY THE MICROPROGRAM CONTROL.

(B) THE PBC IS ACTIVATED BY THE MICROPROGRAM CONTROL AND AS A RESULT, ISSUES A MEMORY REQUEST (ASSUME AN INSTRUCTION FETCH). AT THIS POINT, THE MICROCONTROL IS FREE TO CONTINUE EXECUTING MICROINSTRUCTIONS.

(C) THE PBC ISSUES A GO SIGNAL TO THE MASC, AND AT THE SAME TIME, GATES THE CONTENTS OF THE SAR TO THE PA. THIS ALLOWS THE PA+1 CIRCUITRY TO START COMPUTING THE NEXT SEQUENTIAL MEMORY ADDRESS CONCURRENT WITH THE PRESENT MEMORY CYCLE. THE PRESENCE OF THE GO SIGNAL AT THE MASC SIGNALS THAT THE ADDRESS, DATA, AND CONTROL LEADS ARE STABLE AND HENCE A MEMORY CYCLE SHOULD BEGIN.

(D) WHEN THE MASC HAS COMPLETED THE REQUEST, IT WILL BE INDICATED WITH THE STORE COMPLETE (SCM) SIGNAL WHICH WILL SET THE DR FLIP-FLOP IN THE PBC. THIS RESULTS IN THE DATA BEING LOADED INTO THE SIR. THE DESTINATION OF THE DATA IS DETERMINED BY THE INSTRUCTION OR DATA (I·D) FLIP-FLOP WHICH IS SET OR CLEARED AS A FUNCTION OF THE TYPE OF MICROINSTRUCTION THAT INITIATED THE MEMORY REQUEST. IN THIS CASE, AN INSTRUCTION FETCH WAS ISSUED (I·D=1). THEREFORE, THE SIR IS USED. IF A DATA REQUEST IS GIVEN (I·D=0), THE SDR IS USED TO BUFFER THE RETURNING DATA.

(E) THE MICROCONTROL THEN TESTS FOR THE COMPLETION OF THE MEMORY REQUEST AND, FINDING THE DR=1, IT WILL USE THE ACCESSED DATA ACCORDINGLY.

(F) THE CYCLE IS THEN REPEATED WHEN THE MICROPROGRAM CONTROL ISSUES A NEW REQUEST. IF THE FOLLOWING REQUEST IS AN INSTRUCTION FETCH FROM THE NEXT SEQUENTIAL ADDRESS, THE OUTPUT OF THE PA+1 LOGIC IS GATED INTO THE SAR. STEPS B THROUGH E ARE REPEATED. IF THE NEXT INSTRUCTION IS A BRANCH, THE MICROPROGRAM CONTROL FIRST DETERMINES WHETHER THE BRANCH IS TO BE MADE (I.E., A CONDITIONAL BRANCH) AND, IF SO, THE NEXT SEQUENTIAL ADDRESS IS NOT ACCESSED. INSTEAD, THE SAR IS LOADED, VIA MICROPROGRAM CONTROL, USUALLY FROM THE DML WHICH IS USED TO COMPUTE THE TARGET ADDRESS. STEPS B THROUGH E ARE AGAIN REPEATED.

TABLE 0

TO AND FROM FIELD DECODER ASSIGNMENTS

SPECIAL REGISTER	GB X SPECIAL REGISTER (TO FIELD PAIR) NETNAME	(PIN NO.)	SPECIAL REGISTER X GB (FROM FIELD PAIR) NETNAME	(PIN NO.)
PA	T204L90A (009)	T204R60A (109)	F204L90A (016)	F204R60B (315)
	*T204L90B (316)	T204R60C (317)	*F204L90B (111)	F204R60C (113)
PA + 1			F204LCOA (116)	F204RCOB (113)
			*F204LCOB (012)	F204RCOC (014)
SAR	T204L90A (009)	T204R50B (309)	F204L90A (016)	F204R50B (115)
	*T204L90B (316)	T204R50C (018)	*F204L90B (111)	F204R50C (313)
SARI	T204LCOA (108)	T204R50B (309)		
	*T204LCOB (017)	T204R50C (018)		
SARD	T204LCOA (108)	T204R30B (010)		
	*T204LCCB (017)	T204R30C (118)		
SIRO	T104L10A (215)	T304REOB (208)	F104L10A (014)	F304REDB (214)
SIRC			F204LCOA (116)	F204R30B (213)
SDRO	T104L20A (015)	T304REOB (208)	F104L20A (313)	F304REDB (214)
SDRC			F204LCOA (116)	F204R50B (115)
IB	T204LCOA (108)	T204R60B (109)	F204LCOA (116)	F204R60B (315)

* THESE TERMINALS ARE FOR FA1D30 ALL OTHERS ARE FOR FA1024

PART OF FS 4
COMPOSITE DIAGRAM 12

3A CENTRAL CONTROL

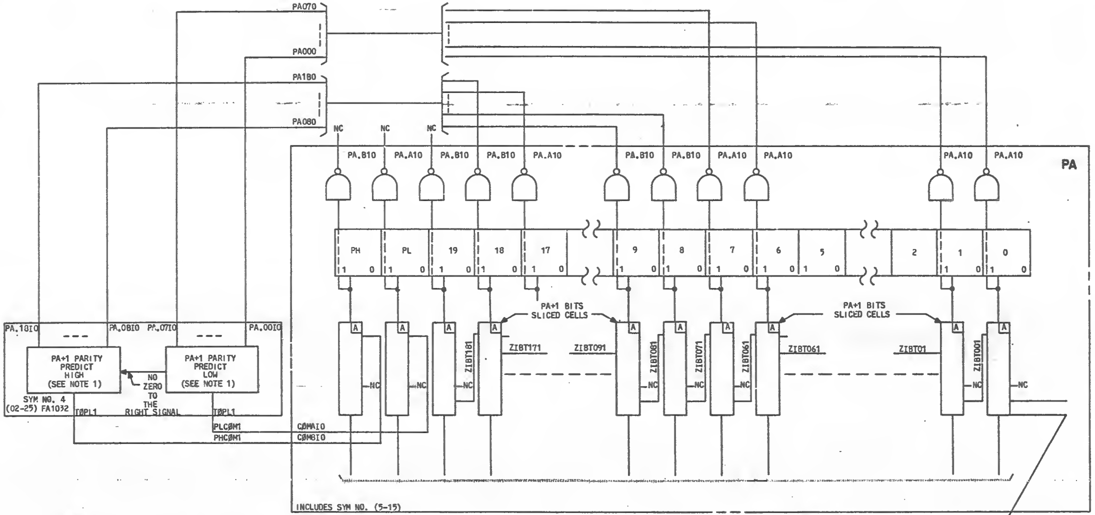
DWG SIZE: bS
ISSUE: 5A

BELL LABORATORIES
SD-1C900-01
B4GT

PRINTED IN U.S.A.

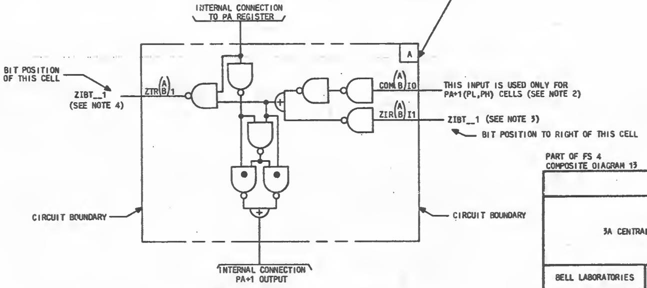
PART OF FS 4
PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 13
PA+1 LOGIC



NOTES:

1. THE OUTPUT OF THIS CIRCUIT, WHEN ACTIVE (HIGH LEVEL SIGNAL), WILL COMPLEMENT THE RESPECTIVE PA PARITY BIT.
2. A HIGH LEVEL INPUT SIGNAL WILL COMPLEMENT THE PA PARITY BIT.
3. WHEN THIS SIGNAL IS INACTIVE (LOW LEVEL) THERE ARE NO "0" TO THE RIGHT OF THIS BIT POSITION IN THE PA REGISTER. HENCE, THIS PA BIT IS TO BE COMPLEMENTED.
4. THIS SIGNAL INDICATES, WHEN ACTIVE (HIGH LEVEL), WHETHER THERE ARE ANY "0" EITHER IN THIS BIT POSITION OR ANY BIT POSITION TO THE RIGHT OF THIS BIT POSITION OF THE PA REGISTER.


INTERNAL CONNECTION TO PA REGISTER
A
BIT POSITION OF THIS CELL
ZIBT__1 (SEE NOTE 4)
ZTR(A/B)1
COM(A/B)IO
ZIR(A/B)I1
THIS INPUT IS USED ONLY FOR PA+1(PL,PH) CELLS (SEE NOTE 2)
ZIBT__1 (SEE NOTE 3)
BIT POSITION TO RIGHT OF THIS CELL
CIRCUIT BOUNDARY
CIRCUIT BOUNDARY
INTERNAL CONNECTION PA+1 OUTPUT

CIRCUIT OPERATION

THE PA+1 LOGIC PERFORMS THE FUNCTION OF INCREMENTING BY ONE, THE CURRENT LOCATION OF THE PROGRAM ADDRESS (PA) REGISTER. THIS LOGICAL ENTITY THUS PROVIDES THE ABILITY TO LINEARLY SEQUENCE THROUGH PROGRAM STORE WITHOUT USING THE ADDER LOGIC IN THE DML.

THE PA+1 LOGIC CONSISTS OF COMBINATIONAL LOGIC ATTACHED TO THE OUTPUT OF THE PA REGISTER. THE LOGIC IS USED TO DETECT THE POSITION OF THE LOWER ORDER ZERO IN THE PA REGISTER. THEN, THE BIT IN THIS POSITION AS WELL AS ALL BITS TO THE RIGHT OF THAT POSITION ARE COMPLEMENTED. THE BITS TO THE LEFT ARE NOT CHANGED. FOR EXAMPLE

```
0 0 1 1¦0 1 1 1  PA
       ¦
_______¦_______1  +1
       ¦
0 0 1 1¦1 0 0 0  PA+1
       ¦
       |→   COMPLEMENT BITS TO RIGHT
            OF HERE.
```

THE IMPLEMENTATION OF THE CIRCUIT TO PROVIDE THIS FUNCTION IS SHOWN IN COMPOSITE DIAGRAM 13. NOTE THAT THIS CIRCUIT IS BIT SLICED IN ORDER TO PROVIDE SELF-CHECKING ON THE PA+1 LOGIC. PARITY ON THE RESULT IS OBTAINED BY INDEPENDENTLY PREDICTING PARITY ON THE RESULT OF THE PA+1 FUNCTION.

THE PARITY PREDICTION CIRCUITRY OPERATES BY DETECTING WHETHER THE LOW ORDER ZERO IN THE PA IS IN AN EVEN POSITION OR AN ODD POSITION. IF THE LOW ORDER ZERO IS IN AN EVEN POSITION, THE PARITY BIT IS COMPLEMENTED FOR THAT FIELD. OTHERWISE, THE PARITY BIT IS LEFT UNCHANGED.

```
PARITY  7 6 5 4 3 2 1 0
   0    0 0 1 1 0 1 1 1  PA   ⎫
                      1  +1   ⎬ NO PARITY
        _______________       ⎪ CHANGE
   0    0 0 1 1 1 0 0 0  PA+1 ⎭

   0    0 0 1 1 1 0 1 1  PA   ⎫
                      1  +1   ⎬ COMPLEMENT
        _______________       ⎪ PARITY
   1    0 0 1 1 1 1 0 0  PA+1 ⎭ BIT
```

SINCE THERE ARE TWO SEPARATE PARITY FIELDS ON THE PA REGISTER (PL AND PH) IF THE LOW ORDER ZERO IS IN ONE FIELD, THE PARITY BIT FOR THE OTHER FIELD IS LEFT UNCHANGED.

PART OF FS 4
COMPOSITE DIAGRAM 13

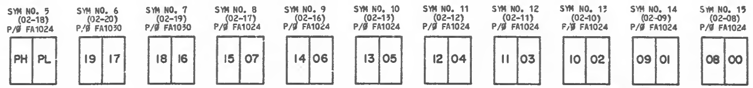
3A CENTRAL CONTROL ②
DWG SIZE 6S
ISSUE 5A
BELL LABORATORIES
SD-1C900-01
B4GU

PART OF FS 4

PROCESSOR BUS CONTROLLER

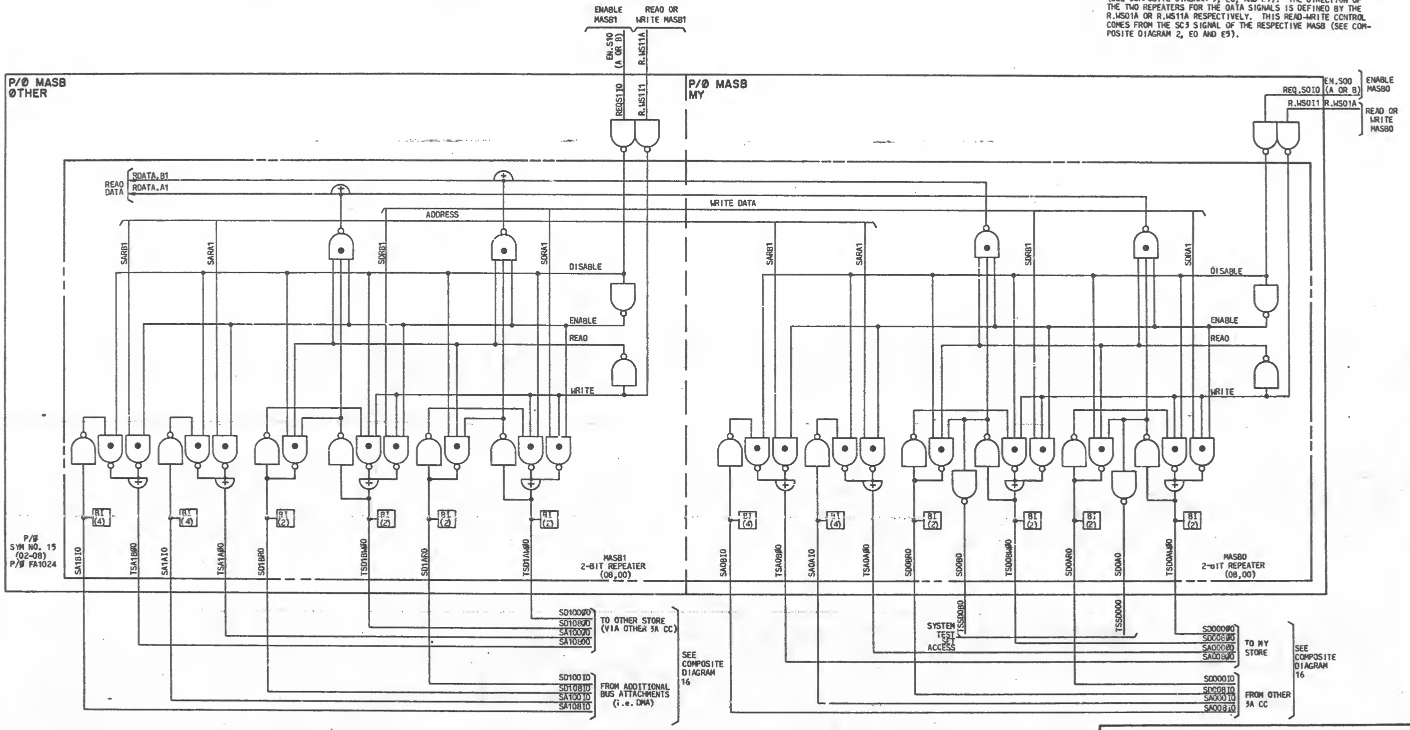
COMPOSITE DIAGRAM 14

BIT SLICED PARTITIONING OF MAIN MEMORY BUS REPEATER


SYM NO. 5 (02-18) P/Ø FA1024
PH
PL
SYM NO. 6 (02-20) P/Ø FA1030
19
17
SYM NO. 7 (02-19) P/Ø FA1030
18
16
SYM NO. 8 (02-17) P/Ø FA1024
15
07
SYM NO. 9 (02-16) P/Ø FA1024
14
06
SYM NO. 10 (02-13) P/Ø FA1024
13
05
SYM NO. 11 (02-12) P/Ø FA1024
12
04
SYM NO. 12 (02-11) P/Ø FA1024
11
03
SYM NO. 13 (02-10) P/Ø FA1024
10
02
SYM NO. 14 (02-09) P/Ø FA1024
09
01
SYM NO. 15 (02-08) P/Ø FA1024
08
00

CIRCUIT OPERATION

COMPOSITE DIAGRAM 14 SHOWS THE 2-BIT REPEATERS FOR THE ADDRESS AND DATA LEADS TO BOTH MASB0 AND MASB1. TO PROVIDE ISOLATION AND DIAGNOSTIC CAPABILITY BETWEEN UNITS ATTACHED TO THE DC BUS, EACH UNIT PROVIDES A NONINVERTING REPEATER FOR EACH OF THE SIGNAL LEADS. THE ABILITY TO SELECTIVELY BLOCK THE REPEATERS AT A GIVEN UNIT IS REQUIRED. THE REPEATERS ARE ENABLED BY THE EN.S00 OR EN.S10 NETS RESPECTIVELY. THIS CONTROL ORIGINATES FROM THE PBC CONTROL LOGIC (SEE COMPOSITE DIAGRAM 3, E0, AND E9). THE DIRECTION OF THE TWO REPEATERS FOR THE DATA SIGNALS IS DEFINED BY THE R.WS01A OR R.WS11A RESPECTIVELY. THIS READ-WRITE CONTROL COMES FROM THE SC3 SIGNAL OF THE RESPECTIVE MASB (SEE COMPOSITE DIAGRAM 2, E0 AND E5).



PART OF FS 4
COMPOSITE DIAGRAM 14

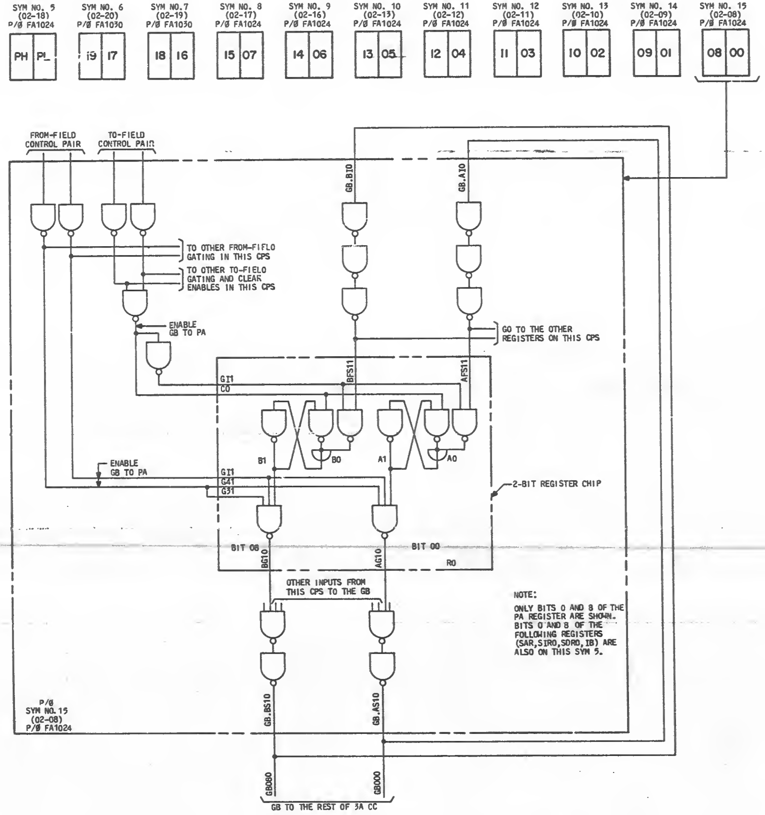
3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B4GV

PART OF FS 4
PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 15
BIT SLICED PARTITIONING OF MAIN MEMORY INTERFACE REGISTERS

CIRCUIT OPERATION

(SEE SHEET B3GB)



SYM NO. 5 (02-18) P/Ø FA1024
PH PL
SYM NO. 6 (02-20) P/Ø FA1030
19 17
SYM NO. 7 (02-19) P/Ø FA1030
18 16
SYM NO. 8 (02-17) P/Ø FA1024
15 07
SYM NO. 9 (02-16) P/Ø FA1024
14 06
SYM NO. 10 (02-13) P/Ø FA1024
13 05
SYM NO. 11 (02-12) P/Ø FA1024
12 04
SYM NO. 12 (02-11) P/Ø FA1024
11 03
SYM NO. 13 (02-10) P/Ø FA1024
10 02
SYM NO. 14 (02-09) P/Ø FA1024
09 01
SYM NO. 15 (02-08) P/Ø FA1024
08 00
FROM-FIELD CONTROL PAIR
TO-FIELD CONTROL PAIR
GB.BI0
GB.AI0
TO OTHER FROM-FIFLO GATING IN THIS CPS
TO OTHER TO-FIELO GATING AND CLEAR ENABLES IN THIS CPS
ENABLE GB TO PA
GO TO THE OTHER REGISTERS ON THIS CPS
GI1
CO
BFS11
AFS11
B1
B0
A1
A0
ENABLE GB TO PA
GI1
G41
G31
2-BIT REGISTER CHIP
BIT 08
BIT 00
BG10
AG10
R0
OTHER INPUTS FROM THIS CPS TO THE GB
GB.BS10
GB.AS10
P/Ø SYM NO. 15 (02-08) P/Ø FA1024
GB080
GB000
GB TO THE REST OF 3A CC

NOTE:

ONLY BITS 0 AND 8 OF THE PA REGISTER ARE SHOWN. BITS 0 AND 8 OF THE FOLLOWING REGISTERS (SAR, SIRO, SDRO, IB) ARE ALSO ON THIS SYM 5.

PART OF FS 4
COMPOSITE DIAGRAM 15

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	5A

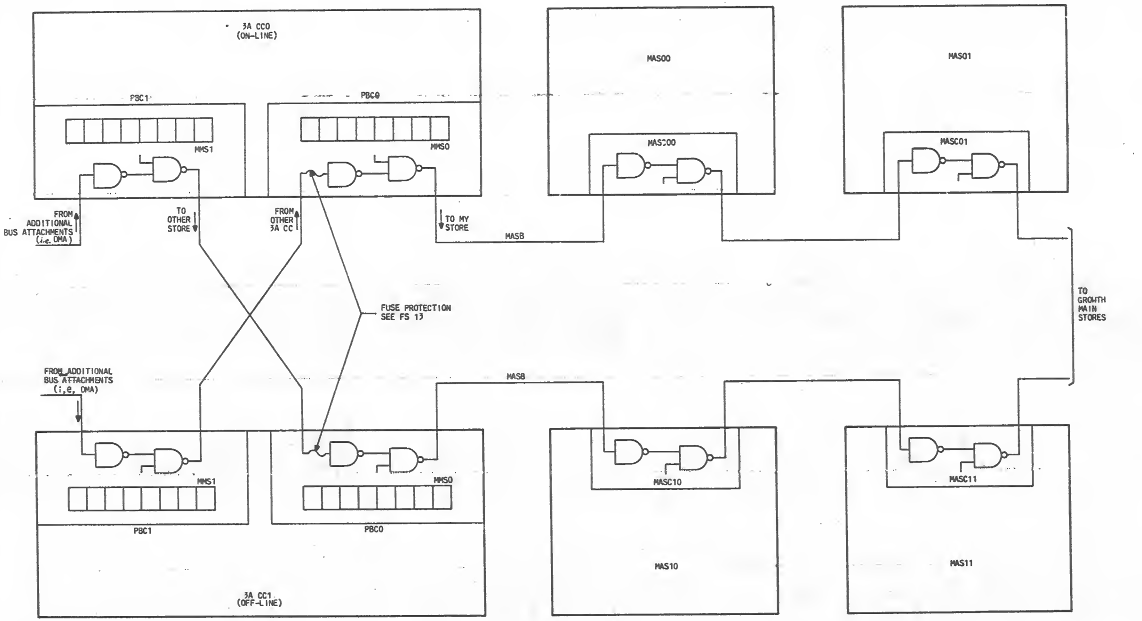
BELL LABORATORIES SD-1C900-01 B4GW

PART OF FS 4

PROCESSOR BUS CONTROLLER

COMPOSITE DIAGRAM 16

3A CC - MAIN MEMORY INTERCONNECTIONS
(ONLY AN ADDRESS SIGNAL SHOWN)



PART OF FS 4
COMPOSITE DIAGRAM 16

3A CENTRAL CONTROL ②

DWG SIZE
6S

ISSUE
5A

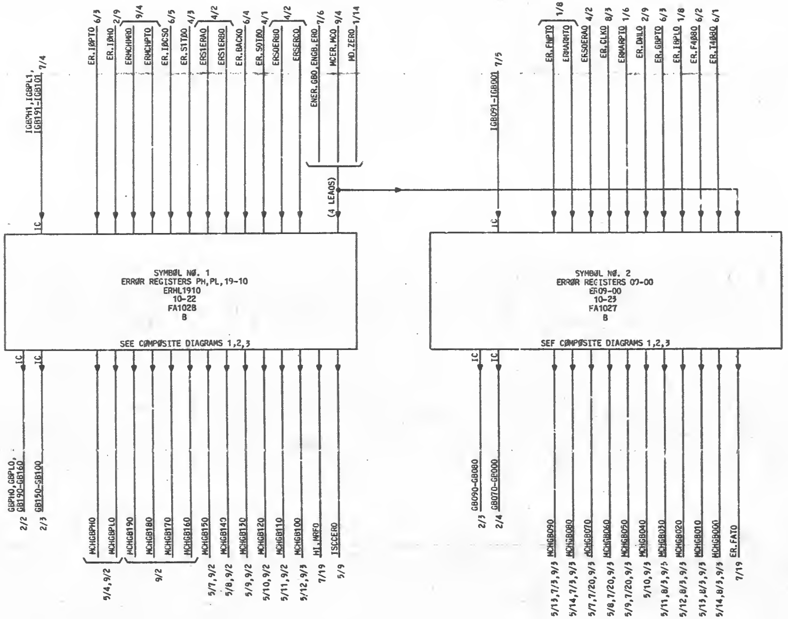
BELL LABORATORIES

SD-1C900-01

B4GX

PART OF FS 5

SPECIAL REGISTERS
INTERCONNECTIØN AND FLØW DIAGRAM



PART ØF FS 5
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES | SD-1C900-01 | B5AA

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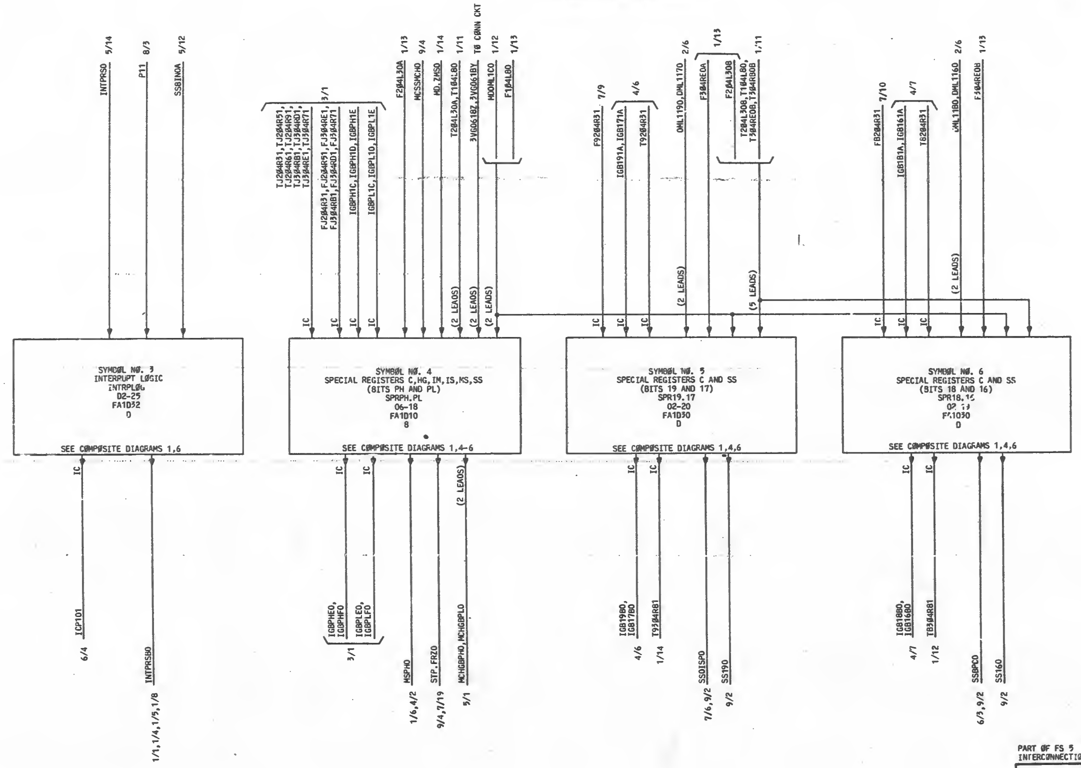
PART OF FS 5

SPECIAL REGISTERS
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR TO- AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 5
INTERCONNECTION AND FLOW DIAGRAM

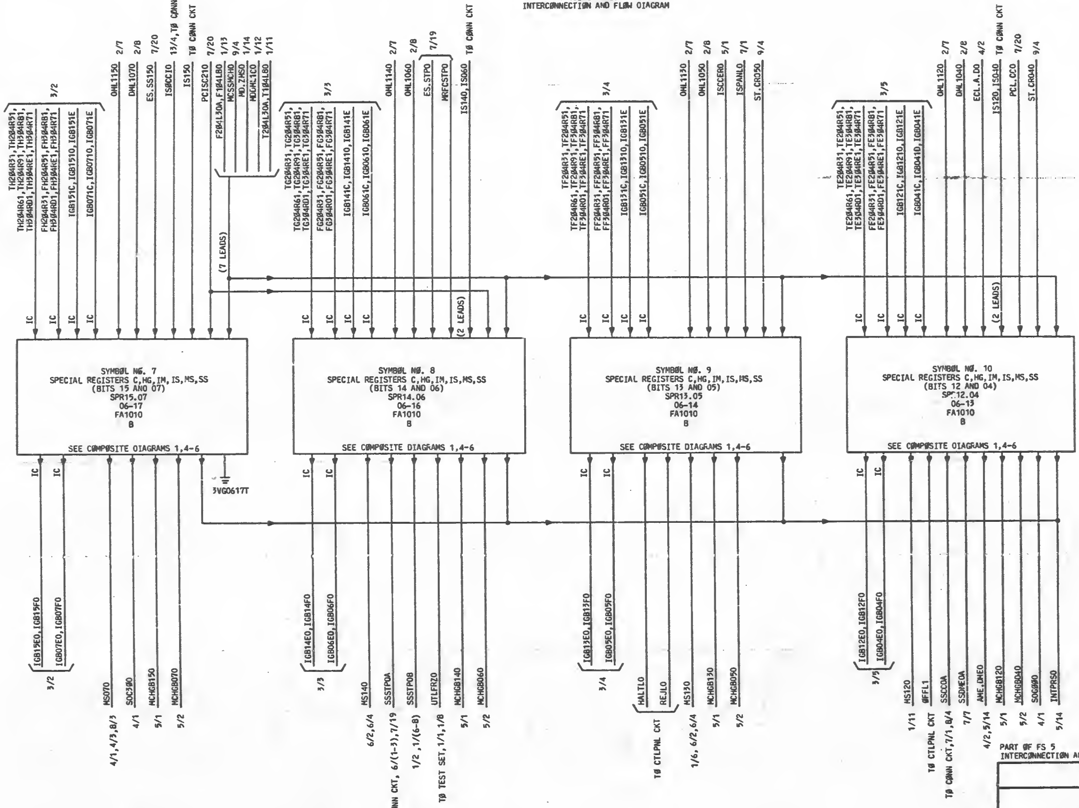
3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B5AB

PRINTED IN U.S.A.

PART OF FS 5

SPECIAL REGISTERS
INTERCØNNECTIØN AND FLØW DIAGRAM

NØTES:
1. FØR TØ- AND FRØM-FIELD DECØDING ASSIGNMENTS SEE NØTE 312.



PART ØF FS 5
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B5AC

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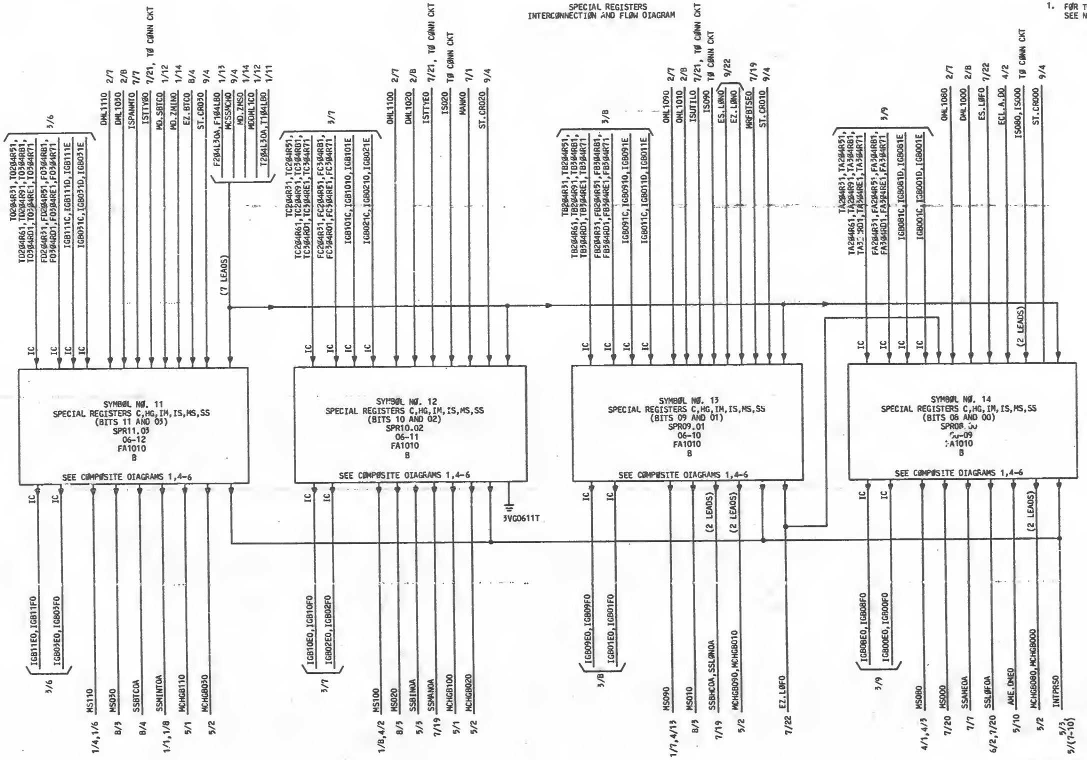
E-7921 (12-73)

PART OF FS 5

SPECIAL REGISTERS
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR TO- AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 5
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B3AD

E-7421 (12-73)

PRINTED IN U.S.A.

PART OF FS 5

SPECIAL REGISTERS

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
AME.DMEO	INDICATION THAT THE ADDRESS AND/OR DATA MATCH BITS (AME OR DME) IN THE SS REGISTER ARE ACTIVE
CRPHO	PARITY HIGH OF THE CR REGISTER
CRPLO	PARITY LOW OF THE CR REGISTER
CR000-CR150	BITS 0-15 OF THE CR REGISTER
DML1PHO	PARITY HIGH OF DML (COPY 1)
DML1PLO	PARITY LOW OF DML (COPY 1)
DML1000-DML1190	BITS 0-19 OF DML (COPY 1)
ECL.A.00	ENABLE CLEARING OF THE ADDRESS MATCH ENABLE BIT AND THE DATA MATCH ENABLE BIT IN THE SS REGISTER (ENABLING IS PERFORMED WHEN A PARITY ERROR IS DETECTED IN THE ON-LINE STORE AND A COMPLEMENT CORRECTION IS TO BE PERFORMED)
ENER.GBO	ENABLE ERROR REGISTER TO THE GATING BUS
ENGB.ERO	ENABLE GATING BUS TO THE ER
ER.BACKO	BRANCH ALLOWED CHECK ERROR
ER.CLKO	CLOCK ERROR
ER.DMLO	DML MATCH ERROR
ER.FATO	FATAL ERROR ("OR" OF BITS 0-9 OF THE ERROR REGISTER)
ER.FNPTO	FUNCTION REGISTER PARITY ERROR
ER.F4080	FROM FIELD 4 OUT OF 8 ERROR CHECK
ER.GBPTO	GATING BUS PARITY ERROR
ER.IBPLO	IB PARITY LOW ERROR
ER.IDCSO	I/O MAIN CHANNEL SELECT ERROR
ER.IOHO	I/O CHANNEL ERROR (I/O DML MATCH ERROR, SUBCHANNEL OR CONTROL STATES ERROR)
ER.IOPTO	I/O CHANNEL PARITY ERROR
ER.SOTOO	MY STORE FAST TIMEOUT ERROR
ER.S1TOO	OTHER STORE FAST TIMEOUT ERROR
ER.T4080	TO FIELD 4 OR 8 DECODER ERROR
ERMARMTO	MAR-RAR MATCH ERROR
ERMARPTO	MAR PARITY ERROR
ERMCHMRO	SWITCH RECEIVED BY ON-LINE CENTRAL CONTROL
ERMCHPTO	PROGRAM TIMER RESET RECEIVED BY ON-LINE CENTRAL CONTROL
ERSERCO	MY STORE ERROR C OR OTHER STORE ERROR C (READ PARITY ERROR)
ERS0ERAO	MY STORE ERROR A (ALL MAIN STORE ERRORS EXCEPT WRITE PROTECT)
ERS0ERBO	MY STORE ERROR B (WRITE PROTECT ERROR)
ERS1ERAO	OTHER STORE ERROR A (ALL MAIN STORE ERRORS EXCEPT, WRITE PROTECT)
ERS1ERBO	OTHER STORE ERROR B (WRITE PROTECT ERROR)
ES.LOFO	ENABLE SET OF LOCK OFF-LINE FLIP-FLOP (BIT 8 OF THE SS)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ES.LONO	ENABLE SET LOCK ON-LINE FLIP-FLOP (BIT 9 OF THE SS)
ES.SS15O	ENABLE SET BIT 15 OF THE SS (SHADOW OF DISABLE FLIP-FLOP)
ES.STPO	ENABLE SET OF STOP FLIP-FLOP (BIT 14 OF THE SS)
EZ.BPCO	ENABLE ZEROING OF BLOCK BUS PARITY CHECK FLIP-FLOP
EZ.BTCO	ENABLE ZEROING OF BLOCK TIMER CHECK FLIP-FLOP
EZ.LOFO	ENABLE ZEROING OF LOCK OFF-LINE FLIP-FLOP
EZ.LONO	ENABLE ZEROING OF LOCK ON-LINE FLIP-FLOP
GBPHO	PARITY HIGH OF THE GATING BUS
GBPLO	PARITY LOW OF THE GATING BUS
GB000-GB190	BITS 0-19 OF THE GATING BUS
HALTLO	PANEL HALT LAMP INDICATOR (BIT 5 OF THE SS)
HI.MRFO	HARDWARE INITIALIZATION ERROR, "MRF" (MAINTENANCE RESET FUNCTION)
ICP101	CLOCK PHASE P1 (POSITIVE ACTIVE) [IC]
IGBPH(E,F)0	INPUTS TO PARITY HIGH OF THE GATING BUS [IC]
IGBPH1	INPUTS TO PARITY HIGH OF GATING BUS [IC]
IGBPH1(C,E)	OUTPUTS OF PARITY HIGH OF THE GATING BUS [IC]
IGBPL(E,F)0	INPUTS TO PARITY LOW OF THE GATING BUS [IC]
IGBPL1	INPUTS TO PARITY LOW OF THE GATING BUS [IC]
IGBPL1(C-E)	OUTPUTS FROM PARITY LOW OF THE GATING BUS [IC]
IGB00E0-IGB15E0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB00F0-IGB15F0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB001-IGB191	OUTPUT FROM GATING BUS BITS 0-19 [IC]
IGBPLE0	OUTPUT FROM GATING BUS BIT PL [IC]
IGBPLF0	OUTPUT FROM GATING BUS BIT PL [IC]
IGB001C-IGB151C	OUTPUT FROM GATING BUS BITS 0-15 [IC]
IGB001D-IGB151D	OUTPUT FROM GATING BUS BITS 0-15 [IC]
IGB001E-IGB151E	OUTPUT FROM GATING BUS BITS 0-15 [IC]
IGB161A-IGB191A	OUTPUTS OF GATING BUS BITS 16-19 [IC]
IGB16B0-IGB19B0	OUTPUTS OF GATING BUS BITS 16-19 [IC]
INTPRSBO	INTERRUPT PRESENT LEAD BUFFERED, (STROBED AND "ANDED" WITH BIN)
INTPRSO	INTERRUPT PRESENT LEAD (UNSTROBED)
ISCCERO	INTERRUPT SET ERROR CONDITION IN THE CENTRAL CONTROL ("OR" AT THE BITS 14-19 OF THE ERROR REGISTER)
ISOCCIO	INTERRUPT SET FROM OTHER CENTRAL CONTROL (FUSED) (SETS BIT 7 OF THE IS)
ISPANLO	PANEL INTERRUPT SET INPUT (SETS BIT 13 OF THE IS)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ISPANMTO	PANEL MATCH INTERRUPT INPUT (SETS BIT 3 OF THE IS)
ISTTYEO	EVEN TTY INTERRUPT SET INPUT (SETS BIT 10 OF THE IS)
ISTTYOO	ODD TTY INTERRUPT SET INPUT (SETS BIT 11 OF THE IS)
ISUTILO	UTILITY INTERRUPT SET INPUT
IS000	DIRECT SET TO THE IS BIT 0
IS020	DIRECT SET TO THE IS BIT 2
IS040	DIRECT SET TO THE IS BIT 4
IS060	DIRECT SET TO THE IS BIT 6
IS080	DIRECT SET TO THE IS BIT 8
IS090	DIRECT SET TO THE IS BIT 9
IS120	DIRECT SET TO THE IS BIT 12
IS140	DIRECT SET TO THE IS BIT 14
IS150	DIRECT SET TO THE IS BIT 15
MANKO	PANEL MANUAL KEY
MCER.MCO	MCA CONTROL, ERROR REGISTER TO THE MCA
MCHGBPHO	PARITY HIGH OF MCA GATING BUS
MCHGBPLO	PARITY LOW OF MCA GATING BUS
MCHGB000-MCHGB190	BITS 0-19 OF MCA GATING BUS
MCSSMCHO	MCA CONTROL, GATE THE SS TO THE MCA
MD.SBTCO	MISC. DECODER, SET BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)
MD.ZERO	MISC. DECODER, ZERO THE ERROR REGISTER
MD.ZMINO	MISC. DECODER, ZERO THE MICROINTERPRET BIT (BIT 11 OF THE SS)
MD.ZMSO	MISC. DECODER, ZERO THE MAINTENANCE STATE REGISTER
MDDML1CO	MISC. DECODER, GATE THE DML COPY 1 TO THE CR REGISTER
MRFBTSEO	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) SET THE BTC FLIP-FLOP AND CLEAR THE SEMI-ENABLE FLIP-FLOPS FOR THE DISABLE FUNCTION
MRFCSTPO	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF), CLEAR STOP FLIP-FLOP
MSPHO	PARITY HIGH OF MAINTENANCE STATE REGISTER
MS000	BIT 0 OF THE MAINTENANCE STATE REGISTER (OVERRIDE I/O DISABLING)
MS010	BIT 1 OF MAINTENANCE STATE REGISTER (CLOCK TEST)
MS020	BIT 2 MAINTENANCE STATE REGISTER (CLOCK TEST)
MS030	BIT 3 MAINTENANCE STATE REGISTER (CLOCK TEST)
MS070	BIT 7 MAINTENANCE STATE REGISTER (ACTIVATE MY STORE)
MS080	BIT 8 MAINTENANCE STATE REGISTER (ACTIVATE OTHER STORE)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MS090	BIT 9 MAINTENANCE STATE REGISTER (ENABLE IB 3 OF 6 TRANSLATORS AND DISABLE FROM FIELD OF CHECK)
MS100	BIT 10 MAINTENANCE STATE REGISTER (ENABLE MAR-RAR MATCH)
MS110	BIT 11 MAINTENANCE STATE REGISTER (HOLD MAR PARITY)
MS120	BIT 12 MAINTENANCE STATE REGISTER (DISABLE TO FIELD)
MS130	BIT 13 OF MAINTENANCE STATE REGISTER
MS140	BIT 14 OF THE MAINTENANCE STATE REGISTER
OFFLI	PANEL LAMP INDICATOR, OUTPUT OF THE CC FLIP-FLOP INDICATES MACHINE IS IN THE STAND-BY MODE (BIT 12 OF THE SS)
PCISC21O	POWER INITIALIZATION, CLEAR ISC BITS 1 AND 2 (BITS 6 AND 7 OF THE SS)
PCL.CCO	POWER INITIALIZATION, CLEAR CC FLIP-FLOP (BIT 12 OF THE SS)
P11	CLOCK PHASE P1 (POSITIVE ACTIVE)
REJLO	PANEL REJECT LAMP INDICATOR
SSAMEOA	ADDRESS MATCH ENABLE BIT (BIT 0 OF THE SS)
SSBHCOA	BLOCK HARDWARE CHECK BIT (BIT 1 OF THE SS)
SSBHCOB	BLOCK HARDWARE CHECK BIT (BIT 1 OF THE SS)

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	DWG SIZE C2	ISSUE 4A
			BSAE

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09/02/76

PART OF FS 5

SPECIAL REGISTERS

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SSBINOA	BLOCK INTERRUPT BIT (BIT 2 OF THE SS)
SSBPCO	BLOCK BUS PARITY CHECK BIT (BIT 18 OF THE SS)
SSBTCO(A,B)	BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)
SSCCOA	CENTRAL CONTROL ON-LINE BIT (BIT 12 OF THE SS)
SSDISPO	DISPLAY BIT (BIT 17 OF THE SS)
SSDMEOA	DATA MATCH ENABLE BIT (BIT 4 OF THE SS)
SSHLTOA	HALT BIT (BIT 5 OF THE SS)
SSISC10(A,B)	ISC BIT 1 (BIT 6 OF THE SS)
SSISC20(A,B)	ISC BIT 2 (BIT 7 OF THE SS)
SSLOFO(A,B)	LOCK OFF-LINE BIT (BIT 8 OF THE SS)
SSLONOA	LOCK ON-LINE BIT (BIT 9 OF THE SS)
SSMANOA	MANUAL BIT (BIT 10 OF THE SS)
SSMINTO(A,B)	MICROINTERPRET BIT (BIT 11 OF THE SS)
SSREJOA	PANEL REJECT BIT (BIT 13 OF SS)
SSSTPO(A,B)	STOP FLIP-FLOP BIT (BIT 14 OF THE SS)
SS160	BIT 16 OF THE SS REGISTER
SS190	BIT 19 OF THE SS REGISTER
ST.BPCO	DIRECT SET OF BLOCK BUS PARITY CHECK BIT OF THE SS REGISTER (BIT 18 OF THE SS)
ST.CRPHO	DIRECT SET OF PARITY HIGH OF THE CR REGISTER
ST.CRPLO	DIRECT SET OF PARITY LOW OF THE CR REGISTER
ST.CR000-ST.CR150	DIRECT SET OF BITS 0-15 OF THE CR REGISTER
STP.FRZO	"OR" OF THE STOP FLIP-FLOP AND THE FREEZE FLIP-FLOP
SOC300	MY MAIN STORE BUS CONTROL LEAD OUTPUT
SOG000	MY MAIN STORE BUS STORE GO SIGNAL OUTPUT
UTLFRZO	UTILITY FREEZE LEAD (INHIBIT LOADING OF NEW OPCODES

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

85AF

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02/21/77

PART OF FS 5

SPECIAL REGISTERS

SYMBOL NO. 1

ERROR REGISTERS PH,PL,19-10

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
ERHL1910	10-22	FA1028	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ENER.GB0	I	304	7/6		EER.GB10	7A3
ENGB.ER0	I	015	7/6		EGB.ER10	5A1
ER.BACK0	I	308	6/4		STER1310	6A4
ER.IOCS0	I	201	6/5		STER1710	5A6
ER.IOH0	I	002	2/9		STERPL10	5A3
ER.IOPT0	I	202	6/3		STERPH10	5A2
ER.S0T00	I	108	4/1		STER1210	6A5
ER.S1T00	I	001	4/3		STER1610	5A6
ERMCHMR0	I	301	9/4		STER1910	5A4
ERMCHPT0	I	101	9/4		STER1810	5A5
ERSERC0	I	008	4/2		STER1010	6A8
ERS0ERB0	I	208	4/2		STER1110	6A7
ERS1ERA0	I	300	4/2		STER1510	6A1
ERS1ERB0	I	100	4/2		STER1410	6A2
GBPH0	OT	IC307	2/2		TGB.PH0	7G0
GBPL0	OT	IC107	2/2		TGB.PL0	7G1
GB100	OT	IC310	2/3		TGB.100	7G7
GB110	OT	IC110	2/3		TGB.110	7G6
GB120	OT	IC210	2/3		TGB.120	7G5
GB130	OT	IC010	2/3		TGB.130	7G5
GB140	OT	IC006	2/3		TGB.140	7G4
GB150	OT	IC206	2/3		TGB.150	7G3
GB160	OT	IC106	2/2		TGB.160	7G3
GB170	OT	IC306	2/2		TGB.170	7G2
GB180	OT	IC007	2/2		TGB.180	7G2
GB190	OT	IC207	2/2		TGB.190	7G1
HI.MRF0	0	312	7/19		ERS0	6H6
IGBPH1	I	IC	7/4		GB.PH11	5A2
IGBPL1	I	IC	7/4		GB.PL11	5A2
IGB101	I	IC	7/4		GB.1011	6C0
IGB111	I	IC	7/4		GB.1111	6C0
IGB121	I	IC	7/4		GB.1211	6C0
IGB131	I	IC	7/4		GB.1311	6C0
IGB141	I	IC	7/4		GB.1411	6C0
IGB151	I	IC	7/4		GB.1511	6D0
IGB161	I	IC	7/4		GB.1611	5A6
IGB171	I	IC	7/4		GB.1711	5A5
IGB181	I	IC	7/4		GB.1811	5A4
IGB191	I	IC	7/4		GB.1911	5A4
ISCCER0	0	009	5/9		ER10	6H3
MCER.MC0	I	305	9/4		ER.ENB10	5A0
MCHGBPH0	OT I	102	5/4 9/2	202	ERPH0	5H2
MCHGBPL0	OT I	204	5/4 9/2	202	ERPL0	5H3
MCHGB100	OT I	013	5/12 9/3	202	ER100	6H8
MCHGB110	OT I	213	5/11 9/2	202	ER110	6H7
MCHGB120	OT I	113	5/10 9/2	202	ER120	6H5
MCHGB130	OT I	313	5/9 9/2	202	ER130	6H4
MCHGB140	OT I	302	5/8 9/2	202	ER140	6H2
MCHGB150	OT I	003	5/7 9/2	202	ER150	6H1
MCHGB160	0	203	9/2	202	ER160	5H7
MCHGB170	0	103	9/2	202	ER170	5H5
MCHGB180	0	303	9/2	202	ER180	5H5
MCHGB190	0	004	9/2	202	ER190	5H4
MD.ZER0	I	005	1/14		CLR.ER10	5A3

SYMBOL NO. 2

ERROR REGISTERS 09-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
ER09-00	10-23	FA1027	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ENER.GB0	I	214	7/6		EER.GB10	9A1
ENGB.ER0	I	313	7/6		EGB.ER10	8A1
ER.CLK0	I	118	8/3		STER0610	7A5
ER.OML0	I	018	2/9		STER0410	7A6
ER.FAT0	0	215	7/19		ERS0	9G9
ER.FNPT0	I	219	1/8		STER0910	7A2
ER.F4080	I	116	6/2		STER0110	8A5
ER.GBPT0	I	317	6/3		STER0310	8A3
ER.IBPL0	I	117	1/8		STER0210	8A3
ER.T4080	I	216	6/1		STER0010	8A5
ERMARMT0	I	019	1/8		STER0810	7A3
ERMARPT0	I	218	1/6		STER0510	7A6
ERS0ERA0	I	318	4/2		STER0710	7A4
GB000	OT	IC301	2/4		TGB.000	9G7
GB010	OT	IC101	2/4		TGB.010	9G7
GB020	OT	IC205	2/4		TGB.020	9G6
GB030	OT	IC105	2/4		TGB.030	9G5
GB040	OT	IC005	2/4		TGB.040	9G5
GB050	OT	IC305	2/4		TGB.050	9G4
GB060	OT	IC208	2/4		TGB.060	9G3
GB070	OT	IC108	2/4		TGB.070	9G3
GB080	OT	IC008	2/3		TGB.080	9G2
GB090	OT	IC308	2/3		TGB.090	9G1
IGB001	I	IC	7/5		GB.0011	8A5
IGB011	I	IC	7/5		GB.0111	8A4
IGB021	I	IC	7/5		GB.0211	8A3
IGB031	I	IC	7/5		GB.0311	8A2
IGB041	I	IC	7/5		GB.0411	7A6
IGB051	I	IC	7/5		GB.0511	7A5
IGB061	I	IC	7/5		GB.0611	7A4
IGB071	I	IC	7/5		GB.0711	7A3
IGB081	I	IC	7/5		GB.0811	7A2
IGB091	I	IC	7/5		GB.0911	7A2
MCER.MC0	I	015	9/4		ER.ENB10	7A1
MCHGB000	OT I	202	5/14,8/3 9/3	202	ER000	8H5
MCHGB010	OT I	002	5/13,8/3 9/3	202	ER010	8H4
MCHGB020	OT I	006	5/12,8/3 9/3	202	ER020	8H3
MCHGB030	OT I	206	5/11,8/3 9/3	202	ER030	8H2
MCHGB040	OT I	106	5/10 9/3	202	ER040	7H6
MCHGB050	OT I	306	5/9,7/20 9/3	202	ER050	7H5
MCHGB060	OT I	007	5/8,7/20 9/3	202	ER060	7H5
MCHGB070	OT I	207	5/7,7/20 9/3	202	ER070	7H4
MCHGB080	OT I	107	5/14,7/3 9/3	202	ER080	7H3
MCHGB090	OT I	307	5/13,7/3 9/3	202	ER090	7H2
MD.ZER0	I	114	1/14		CLR.ER10	7A1

SYMBOL NO. 3

INTERRUPT LOGIC

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
INTRPLOG	02-25	FA1032	0	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ICP101	0	IC	6/4		P101	7H3
INTPRSB0	0	307	1/1,1/4 1/5,1/8		INTRP0	7H4
INTPRS0	I	104	5/14		INTRP10	7A2
PTT	I	103	8/3		P11	7A3
SSBIN0A	I	110	5/12	202	BIN10	7A3

SYMBOL NO. 4

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPRPH.PL	06-18	FA1010	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		004			MK.ISB0	11H7
		007			TGRDHGA0	10A8
		010			SS.A10A	11H5
		106			DSTISA10	10A2
		115			SS.B10B	11H4
		204			MK.ISA0	11H7
		209			TGRDHGB0	10A9
		210			SS.B10A	11H4
		306			DSTISB10	10A1
		315			SS.A10B	11H5
CRPH0		016			CR.B10	9H3
CRPL0		216			CR.A10	9H4
DML1PH0		118			DML1.B0	9A2
DML1PL0		308			DML1.A0	9A5
FJ204R31	I	IC	3/1		F204R31	9A2
FJ204R51	I	IC	3/1		F204R51	10A6
FJ304RB1	I	IC	3/1		F304RB1	10E0
FJ304RD1	I	IC	3/1		F304RD1	10A4
FJ304RE1	I	IC	3/1		F304RE1	11A2
FJ304R71	I	IC	3/1		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGBPHE0	0	IC	3/1		TA9	10G7
IGBPHF0	0	IC	3/1		TB9	10G7
IGBPH1C	I	IC	3/1		GB.BD1C	10A3
IGBPH10	I	IC	3/1		GB.BD10	9E0
IGBPH1E	I	IC	3/1		GB.BD1A	10A5
IGBPLE0	0	IC	3/1		TA8	10H4
IGBPLF0	0	IC	3/1		TB8	10H3
IGBPL1C	I	IC	3/1		GB.AD1C	10A4
IGBPL10	I	IC	3/1		GB.AD10	9E0
IGBPL1E	I	IC	3/1		GB.AD1A	10A6
MCHGBPH0	OT	104	5/1	202	GSS.B10C	11H4
MCHGBPL0	OT	304	5/1	202	GSS.A10C	11H6
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMS10	10A6
MDDML1C0	I	219	1/12		DML1.C10	9A1
MSPH0	0	309	1/6,8/3	202	MS.B10	10H5
ST.CRPH0		019			DSET.CB0	9A3

SYMBOL NO. 4 (CONT)

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS PH AND PL)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPRPH.PL	06-18	FA1010	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ST.CRPL0		318			DSET.CA0	9A4
STP.FR20	OT I	109	7/19 9/4		MS.A10	10H6
TJ204R31	I	IC	3/1		T204R31	9A2
TJ204R51	I	IC	3/1		T204R51	10A6
TJ204R61	I	IC	3/1		T204R61	9A5
TJ204R91	I	IC	3/1		T204R91	9A6
TJ304RB1	I	IC	3/1		T304RB1	11A1
TJ304RD1	I	IC	3/1		T304RD1	10A5
TJ304RE1	I	IC	3/1		T304RE1	11F0
TJ304R71	I	IC	3/1		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6
3VG0618Y	I	116			OCLASS10	11A5
	I	117	TO CONN CKT		OSTBSS10	11A3
3VG0618Z	I	316			OSTASS10	11A5
	I	317	TO CONN CKT		OCLBSS10	11A4

PART OF FS 5
SYMBOL(S) 1 2 3 4

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B5CA

PRINTED IN U. S. A.

06/10/77

PART OF FS 5

SPECIAL REGISTERS

SYMBOL NO. 5

SPECIAL REGISTERS C AND SS
(BITS 19 AND 17)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR19.17	02-20	FA1030	0	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		102			CL.SSBI0	6A6
		315			ST.SSBI0	6A4
OML1170	I	214	2/6	202	DML.A0	6A3
OML1190	I	314	2/6	202	DML.B0	6A3
F104L80	I	312	1/13		F104L80	6A4
F204L30B	I	213	1/13		F204L30	6A0
F304RE0A	I	013	1/13		F304RE0	6A4
F9204R31	I	IC	7/9		F204R31	6A0
IGB17B0	0	IC	4/6		TIGBAC0	6H5
IGB171A	I	IC	4/6		GB.B01	6A0
IGB19B0	0	IC	4/6		TIGBBC0	6H5
IGB191A	I	IC	4/6		GB.A01	6A0
MODML1C0	I	114	1/12		DML1.CI0	6A1
SS0ISP0	0	208	7/6,9/2	202	SSA10	6H7
SS190	0	008	9/2		SSB10	6H6
T104L80	I	015	1/11		T104L80	6A5
T204L30B	I	117	1/11		T204L30	6A1
T304RB0B	I	215	1/11		T304RB0	6A5
T304RE0B	I	115	1/11		T304RE0	6A7
T9204R31	I	IC	4/6		T204R31	6A0
T9304RB1	0	IC	1/14		T304RB1	6C8

SYMBOL NO. 6

SPECIAL REGISTERS C AND SS
(BITS 18 AND 16)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR18.16	02-19	FA1030	0	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
OML1160	I	214	2/6	202	OML.A0	6A3
OML1180	I	314	2/6	202	DML.B0	6A3
E2.BPC0		102			CL.SSBI0	6A6
F104L80	I	312	1/13		F104L80	6A4
F204L30B	I	213	1/13		F204L30	6A0
F304RE0B	I	013	1/13		F304RE0	6A4
F8204R31	I	IC	7/10		F204R31	6A0
IGB16B0	0	IC	4/7		TIGBAC0	6H5
IGB161A	I	IC	4/7		GB.B01	6A0
IGB18B0	0	IC	4/7		TIGBBC0	6H5
IGB181A	I	IC	4/7		GB.A01	6A0
MODML1C0	I	114	1/12		DML1.CI0	6A1
SS8PC0	0	008	6/3,9/2		SSB10	6H6
SS160	0	208	9/2		SSA10	6H7
ST.BPC0		315			ST.SSBI0	6A4
T104L80	I	015	1/11		T104L80	6A5
T204L30B	I	117	1/11		T204L30	6A1
T304RB0B	I	215	1/11		T304RB0	6A5
T304RE08	I	115	1/11		T304RE0	6A7
T8204R31	I	IC	4/7		T204R31	6A0
T8304RB1	0	IC	1/12		T304RB1	6C8

SYMBOL NO. 7

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR15.07	06-17	FA1010	8	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		115			SS.B10B	11H4
		209			TGRDHGB0	10A9
		210			SS.B10A	11H4
		316			OSTASSI0	11A5
CR070		216			CR.A10	9H4
CR150		016			CP.B10	9H3
OML1070	I	308	2/8	202	OML1.A0	9A5
OML1150	I	118	2/7	202	DML1.B0	9A2
ES.SS150	I	117	7/20		DSTBSSI0	11A3
FH204R31	I	IC	3/2		F204R31	9A2
FH204R51	I	IC	3/2		F204R51	10A6
FH304RB1	I	IC	3/2		F304RB1	10E0
FH304RD1	I	IC	3/2		F304RD1	10A4
FH304RE1	I	IC	3/2		F304RE1	11A2
FH304R71	I	IC	3/2		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGB07E0	0	IC	3/2		TA8	10H4
IGB07F0	0	IC	3/2		TB8	10H3
IGB071C	I	IC	3/2		GB.AD1C	10A4
IGB071D	I	IC	3/2		GB.AD10	9E0
IGB071E	I	IC	3/2		GB.AD1A	10A6
IGB15E0	0	IC	3/2		TA9	10G7
IGB15F0	0	IC	3/2		TB9	10G7
IGB151C	I	IC	3/2		GB.BD1C	10A3
IGB1510	I	IC	3/2		GB.BD10	9E0
IGB151E	I	IC	3/2		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	OT	204	5/14		MK.ISA0	11H7
ISOCCIJ	I	106	13/4 TO CONN CKT		DSTISAI0	10A2
IS150	I	306	TO CONN CKT		DSTISBI0	10A1
MCHGB070	OT	304	5/2	202	GSS.A10C	11H6
MCHGB150	OT	104	5/1	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MODML1C0	I	219	1/12		DML1.CI0	9A1
MS070	0	109	4/1,4/3 8/3		MS.A10	10H6
PCISC210	I	116	7/20		OCLASSI0	11A5
SSISC20A		010			SS.A10A	11H5
SSISC20B		315			SS.A10B	11H5
ST.CR070		318			DSET.CA0	9A4
ST.CR150		019			DSET.CB0	9A3
S0C300	0	309	4/1		MS.B10	10H5
TH204R31	I	IC	3/2		T204R31	9A2
TH204R51	I	IC	3/2		T204R51	10A6
TH204R61	I	IC	3/2		T204R61	9A5
TH204R91	I	IC	3/2		T204R91	9A6
TH304RB1	I	IC	3/2		T304RB1	11A1
TH304RD1	I	IC	3/2		T304RD1	10A5
TH304RE1	I	IC	3/2		T304RE1	11F0
TH304R71	I	IC	3/2		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6
3VG0617T	I	317	3/2		OCLBSSI0	11A4

SYMBOL NO. 8

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR14.06	06-16	FA1010	8	

FS INFO / CP INFO

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		209			TGRDHGB0	10A9
		316			DSTASSI0	11A5
CR060		216			CR.A10	9H4
CR140		016			CR.B10	9H3
OML1060	I	308	2/8	202	DML1.A0	9A5
OML1140	I	118	2/7	202	OML1.B0	9A2
ES.STP0	I	117	7/19		OSTBSSI0	11A3
FG204R31	I	IC	3/3		F204R31	9A2
FG204R51	I	IC	3/3		F204R51	10A6
FG304RB1	I	IC	3/3		F304RB1	10E0
FG304RD1	I	IC	3/3		F304RD1	10A4
FG304RE1	I	IC	3/3		F304RE1	11A2
FG304R71	I	IC	3/3		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGB06E0	0	IC	3/3		TA8	10H4
IGB06F0	0	IC	3/3		TB8	10H3
IGB061C	I	IC	3/3		GB.AD1C	10A4
IGB0610	I	IC	3/3		GB.AD10	9E0
IGB061E	I	IC	3/3		GB.AD1A	10A6
IGB14E0	0	IC	3/3		TA9	10G7
IGB14F0	0	IC	3/3		TB9	10G7
IGB141C	I	IC	3/3		GB.BD1C	10A3
IGB1410	I	IC	3/3		GB.BD10	9E0
IGB141E	I	IC	3/3		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	OT	204	5/14		MK.ISA0	11H7
IS060	I	106	TO CONN CKT		OSTISAI0	10A2
IS140	I	306	TO CONN CKT		OSTISBI0	10A1
MCHGB060	OT	304	5/2	202	GSS.A10C	11H6
MCHGB140	OT	104	5/1	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MODML1C0	I	219	1/12		DML1.CI0	9A1
MRFCSTP0	I	317	7/19		OCLBSSI0	11A4
MS140	0	309	6/2,6/4		MS.B10	10H5
PCISC210	I	116	7/20		OCLASSI0	11A5
SSISC10A		010			SS.A10A	11H5
SSISC10B		315			SS.A10B	11H5
SSSTP0A	0	115	6/1,6/2 6/3,7/19 TO CONN CKT		SS.B10B	11H4
SSSTP0B	0	210	1/2,1/6 1/7,1/8		SS.B10A	11H4
ST.CR060		318			OSET.CA0	9A4
ST.CR140		019			OSET.CB0	9A3
TG204R31	I	IC	3/3		T204R31	9A2
TG204R51	I	IC	3/3		T204R51	10A6
TG204R61	I	IC	3/3		T204R61	9A5
TG204R91	I	IC	3/3		T204R91	9A6
TG304RB1	I	IC	3/3		T304RB1	11A1
TG304RD1	I	IC	3/3		T304RD1	10A5
TG304RE1	I	IC	3/3		T304RE1	11F0
TG304R71	I	IC	3/3		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6
UTLFR20	0	109	1/1,1/8		MS.A10	10H6

PART OF FS 5
SYMBOL(S) 5 6 7 8

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	5A

BELL LABORATORIES
SD-1C900-01
B5C8
PRINTED IN U. S. A.
06/10/77

PART OF FS 5

SPECIAL REGISTERS

SYMBOL NO. 9

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR13.05	06-14	FA1010	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		109			MS.A10	10H6
		116			DCLASSI0	11A5
		117			DSTBSSI0	11A3
		209			TGRDHGB0	10A9
		316			DSTASSI0	11A5
		317			DCLBSSI0	11A4
CR050		216			CR.A10	9H4
CR130		016			CR.B10	9H3
DML1050	I	308	2/8	202	DML1.A0	9A5
DML1130	I	118	2/7	202	DML1.B0	9A2
FF204R31	I	IC	3/4		F204R31	9A2
FF2D4R51	I	IC	3/4		F2D4R51	10A6
FF3D4RB1	I	IC	3/4		F304RB1	10E0
FF3D4RD1	I	IC	3/4		F304RD1	10A4
FF3D4RE1	I	IC	3/4		F304RE1	11A2
FF304R71	I	IC	3/4		F3D4R71	10A2
F1D4L80	I	003	1/13		F104L80	10A0
F2D4L30A	I	107	1/13		F204L30	9A2
HALTL0	D	315	TO CTLPNL CKT		SS.A10B	11H5
IGB05E0	D	IC	3/4		TA8	10H4
IGB05F0	O	IC	3/4		TB8	10H3
IGB051C	I	IC	3/4		GB.AD1C	10A4
IGB051D	I	IC	3/4		GB.AD1D	9E0
IGB051E	I	IC	3/4		GB.AD1A	10A6
IGB13E0	D	IC	3/4		TA9	10G7
IGB13F0	O	IC	3/4		TB9	10G7
IGB131C	I	IC	3/4		GB.BD1C	10A3
IGB131D	I	IC	3/4		GB.BD1D	9E0
IGB131E	I	IC	3/4		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	OT	204	5/14		MK.ISA0	11H7
ISCCER0	I	106	5/1		DSTISAI0	10A2
ISPANL0	I	306	7/1		DSTISBI0	10A1
MCHGB050	DT	304	5/2	202	GSS.A10C	11H6
MCHGB130	DT	104	5/1	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MDDML1C0	I	219	1/12		DML1.CI0	9A1
MS130	O	309	1/6,6/2 6/4		MS.B10	10H5
REJL0	D	115	TO CTLPNL CKT		SS.B10B	11H4
SSHLT0A		010			SS.A10A	11H5
SSREJ0A		210			SS.B10A	11H4
ST.CR050	I	318	9/4		DSET.CA0	9A4
ST.CR130		019			DSET.CB0	9A3
TF204R31	I	IC	3/4		T204R31	9A2
TF204R51	I	IC	3/4		T204R51	10A6
TF2D4R61	I	IC	3/4		T204R61	9A5
TF204R91	I	IC	3/4		T204R91	9A6
TF304RB1	I	IC	3/4		T304RB1	11A1
TF3C4RD1	I	IC	3/4		T3D4RD1	10A5
TF3D4RE1	I	IC	3/4		T304RE1	11F0
TF3D4R71	I	IC	3/4		T304R71	10A3
T1D4L80	I	011	1/11		T104L80	11A2
T2D4L30A	I	009	1/11		T2D4L30	11A6

SYMBOL NO. 10

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR12.04	06-13	FA1010	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		117			DSTBSSI0	11A3
		209			TGRDHGB0	10A9
		316			DSTASSI0	11A5
AME.OME0	OT	315	5/14		SS.A10B	11H5
	I		4/2			
CR040		216			CR.A10	9H4
CR120		016			CR.B10	9H3
DML1040	I	308	2/8	202	DML1.A0	9A5
DML1120	I	118	2/7	202	DML1.B0	9A2
ECL.A.D0	I	116	4/2		DCLASSI0	11A5
FE2D4R31	I	IC	3/5		F204R31	9A2
FE2D4R51	I	IC	3/5		F204R51	10A6
FE304RB1	I	IC	3/5		F304RB1	10E0
FE304RD1	I	IC	3/5		F3D4RD1	10A4
FE304RE1	I	IC	3/5		F304RE1	11A2
FE3D4R71	I	IC	3/5		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGB04E0	D	IC	3/5		TA8	10H4
IGB04F0	O	IC	3/5		TB8	10H3
IGB041C	I	IC	3/5		GB.AD1C	10A4
IGB041D	I	IC	3/5		GB.AD1D	9E0
IGB041E	I	IC	3/5		GB.AD1A	10A6
IGB12E0	D	IC	3/5		TA9	10G7
IGB12F0	O	IC	3/5		TB9	10G7
IGB121C	I	IC	3/5		GB.BD1C	10A3
IGB121D	I	IC	3/5		GB.BD1D	9E0
IGB121E	I	IC	3/5		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	OT	204	5/14		MK.ISA0	11H7
IS040	I	106	TO CONN CKT		DSTISAI0	10A2
IS120	I	306	TO CONN CKT		DSTISBI0	10A1
MCHGB040	OT	304	5/2	202	GSS.A10C	11H6
MCHGB120	OT	104	5/1	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MDDML1C0	I	219	1/12		DML1.CI0	9A1
MS120	O	309	1/11		MS.B10	10H5
OFFL1	O	115	TO CTLPNL CKT	202	SS.B10B	11H4
PCL.CC0	I	317	7/20		DCLBSSI0	11A4
SSCC0A	O	210	7/1,8/4 TO CONN CKT		SS.B10A	11H4
SSDME0A	D	010	7/7		SS.A10A	11H5
ST.CR040	I	318	9/4		DSET.CA0	9A4
ST.CR120		019			DSET.CB0	9A3
S0G000	D	109	4/1		MS.A10	10H6
TE204R31	I	IC	3/5		T204R31	9A2
TE204R51	I	IC	3/5		T2D4R51	10A6
TE2D4R61	I	IC	3/5		T204R61	9A5
TE204R91	I	IC	3/5		T204R91	9A6
TE3D4RB1	I	IC	3/5		T304RB1	11A1
TE3D4RD1	I	IC	3/5		T304RD1	10A5
TE3D4RE1	I	IC	3/5		T304RE1	11F0
TE304R71	I	IC	3/5		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6

SYMBOL NO. 11

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR11.03	06-12	FA1010	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		117			DSTBSSI0	11A3
		209			TGRDHGB0	10A9
CR030		216			CR.A10	9H4
CR110		016			CR.B10	9H3
DML1030	I	308	2/8	202	DML1.A0	9A5
DML1110	I	118	2/7	202	DML1.B0	9A2
E2.BTC0	I	116	8/4		DCLASSI0	11A5
FD204R31	I	IC	3/6		F204R31	9A2
FD2D4R51	I	IC	3/6		F2D4R51	10A6
FD304RB1	I	IC	3/6		F304RB1	10E0
FD304RD1	I	IC	3/6		F304RD1	10A4
FD304RE1	I	IC	3/6		F304RE1	11A2
FD3D4R71	I	IC	3/6		F3D4R71	10A2
F104L80	I	003	1/13		F1D4L80	10A0
F204L30A	I	107	1/13		F2D4L30	9A2
IGB03E0	D	IC	3/6		TA8	10H4
IGB03F0	D	IC	3/6		TB8	10H3
IGB031C	I	IC	3/6		GB.AD1C	10A4
IGB031D	I	IC	3/6		GB.AD1D	9E0
IGB031E	I	IC	3/6		GB.AD1A	10A6
IGB11E0	D	IC	3/6		TA9	10G7
IGB11F0	D	IC	3/6		TB9	10G7
IGB111C	I	IC	3/6		GB.BD1C	10A3
IGB111D	I	IC	3/6		GB.BD1D	9E0
IGB111E	I	IC	3/6		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	DT	204	5/14		MK.ISA0	11H7
ISPANMT0	I	106	7/7		DSTISAI0	10A2
ISTTY00	I	306	7/21 TD CONN CKT		DSTISBI0	10A1
MCHGB030	OT	304	5/2	202	GSS.A10C	11H6
MCHGB110	DT	104	5/1	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.SBTC0	I	316	1/12		DSTASSI0	11A5
MD.ZMIN0	I	317	1/14		DCLBSSI0	11A4
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MDDML1C0	I	219	1/12		DML1.CI0	9A1
MS030	D	109	8/3		MS.A10	10H6
MS110	O	309	1/4,1/6		MS.B10	10H5
SSBTC0A	D	010	8/4	202	SS.A10A	11H5
SSBTC0B		315			SS.A10B	11H5
SSMINT0A	O	210	1/1,1/8		SS.B10A	11H4
SSMINT0B		115			SS.B10B	11H4
ST.CR030	I	318	9/4		DSET.CA0	9A4
ST.CR110		019			DSET.CB0	9A3
TD204R31	I	IC	3/6		T204R31	9A2
TD204R51	I	IC	3/6		T204R51	10A6
TD204R61	I	IC	3/6		T204R61	9A5
TD204R91	I	IC	3/6		T204R91	9A6
TD304RB1	I	IC	3/6		T304RB1	11A1
TD304RD1	I	IC	3/6		T304RD1	10A5
TD304RE1	I	IC	3/6		T304RE1	11F0
TD304R71	I	IC	3/6		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6

PART OF FS 5
SYMBOL(S) 9 10 11

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B5CC

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PART OF FS 5

SPECIAL REGISTERS

SYMBOL NO. 12

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR10.02	06-11	FA1010	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		115			SS.B108	11H4
		116			OCLASSI0	11A5
		209			TGRDHGB0	10A9
		315			SS.A108	11H5
		316			DSTASSI0	11A5
CR020		216			CR.A10	9H4
CR100		016			CR.B10	9H3
DML1020	I	308	2/8	202	DML1.A0	9A5
DML1100	I	118	2/7	202	DML1.B0	9A2
FC204R31	I	IC	3/7		F204R31	9A2
FC204R51	I	IC	3/7		F204R51	10A6
FC304R81	I	IC	3/7		F304R81	10E0
FC304RD1	I	IC	3/7		F304RD1	10A4
FC304RE1	I	IC	3/7		F304RE1	11A2
FC304R71	I	IC	3/7		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGB02E0	O	IC	3/7		TA8	10H4
IGB02F0	O	IC	3/7		TB8	10H3
IGB021C	I	IC	3/7		GB.AD1C	10A4
IGB021D	I	IC	3/7		GB.AD1D	9E0
IGB021E	I	IC	3/7		GB.AD1A	10A6
IGB10E0	O	IC	3/7		TA9	10G7
IGB10F0	O	IC	3/7		TB9	10G7
IGB101C	I	IC	3/7		GB.BD1C	10A3
IGB101D	I	IC	3/7		GB.BD1D	9E0
IGB101E	I	IC	3/7		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	OT	204	5/14		MK.ISA0	11H7
ISTTYE0	I	306	7/21 TO CONN CKT		DSTISBI0	10A1
IS020	I	106	TO CONN CKT		DSTISAI0	10A2
MANK0	I	117	7/1		OSTBSSI0	11A3
MCHGB020	OT	304	5/2	202	GSS.A10C	11H6
MCHGB100	OT	104	5/1	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MODML1C0	I	219	1/12		DML1.CI0	9A1
MS020	O	109	8/3		MS.A10	10H6
MS100	O	309	1/8,4/2		MS.B10	10H5
SSB1N0A	O	010	5/3	202	SS.A10A	11H5
SSMAN0A	O	210	7/19	202	SS.B10A	11H4
ST.CR020	I	318	9/4		DSET.CA0	9A4
ST.CR100		019			DSET.CB0	9A3
TC204R31	I	IC	3/7		T204R31	9A2
TC204R51	I	IC	3/7		T204R51	10A6
TC204R61	I	IC	3/7		T204R61	9A5
TC204R91	I	IC	3/7		T204R91	9A6
TC304R81	I	IC	3/7		T304R81	11A1
TC304RD1	I	IC	3/7		T304RD1	10A5
TC304RE1	I	IC	3/7		T304RE1	11F0
TC304R71	I	IC	3/7		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6
ZVG0611T	I	317	3/7		OCLBSSI0	11A4

SYMBOL NO. 13

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR09.01	06-10	FA1010	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		116			OCLASSI0	11A5
		209			TGRDHGB0	10A9
CR010		216			CR.A10	9H4
CR090		016			CR.B10	9H3
DML1010	I	308	2/8	202	DML1.A0	9A5
DML1090	I	118	2/7	202	DML1.B0	9A2
ES.LON0	I	117	7/22		DSTBSSI0	11A3
E2.LOF0	OT	115	7/22		SS.B108	11H4
	I		5/14			
E2.LON0	I	317	7/22		DCLBSSI0	11A4
FB204R31	I	IC	3/8		F204R31	9A2
FB204R51	I	IC	3/8		F204R51	10A6
FB304R81	I	IC	3/8		F304R81	10E0
FB304RD1	I	IC	3/8		F304RD1	10A4
FB304RE1	I	IC	3/8		F304RE1	11A2
FB304R71	I	IC	3/8		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGB01E0	O	IC	3/8		TA8	10H4
IGB01F0	O	IC	3/8		TB8	10H3
IGB011C	I	IC	3/8		GB.AD1C	10A4
IGB011D	I	IC	3/8		GB.AD1D	9E0
IGB011E	I	IC	3/8		GB.AD1A	10A6
IGB09E0	O	IC	3/8		TA9	10G7
IGB09F0	O	IC	3/8		TB9	10G7
IGB091C	I	IC	3/8		GB.BD1C	10A3
IGB091D	I	IC	3/8		GB.BD1D	9E0
IGB091E	I	IC	3/8		GB.BD1A	10A5
INTPRS0	OT	004	5/14		MK.ISB0	11H7
	OT	204	5/14		MK.ISA0	11H7
ISUTIL0	I	106	7/21 TO CONN CKT		DSTISAI0	10A2
IS090	I	306	TO CONN CKT		DSTISBI0	10A1
MCHGB010	OT	304	5/2	202	GSS.A10C	11H6
MCHGB090	OT	104	5/2	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MODML1C0	I	219	1/12		DML1.CI0	9A1
MRFBTSE0	I	316	7/19		DSTASSI0	11A5
MS010	O	109	8/3		MS.A10	10H6
MS090	O	309	1/7,4/13		MS.B10	10H5
SSBHC0A	O	010	7/19	202	SS.A10A	11H5
SSBHC0B		315			SS.A10B	11H5
SSLON0A	O	210	7/19		SS.B10A	11H4
ST.CR010	I	318	9/4		DSET.CA0	9A4
ST.CR090		019			DSET.CB0	9A3
TB204R31	I	IC	3/8		T204R31	9A2
TB204R51	I	IC	3/8		T204R51	10A6
TB204R61	I	IC	3/8		T204R61	9A5
TB204R91	I	IC	3/8		T204R91	9A6
TB304R81	I	IC	3/8		T304R81	11A1
TB304RD1	I	IC	3/8		T304RD1	1CA5
TB304RE1	I	IC	3/8		T304RE1	11F0
TB304R71	I	IC	3/8		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6

SYMBOL NO. 14

SPECIAL REGISTERS C,HG,IM,IS,MS,SS
(BITS 08 AND 00)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPR08.00	06-09	FA1010	8	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		007			TGRDHGA0	10A8
		209			TGRDHGB0	10A9
		316			DSTASSI0	11A5
AME.DME0	OT	315	5/10		SS.A108	11H5
CR000		216			CR.A10	9H4
CR080		016			CR.B10	9H3
DML1000	I	308	2/8	202	DML1.A0	9A5
DML1080	I	118	2/7	202	DML1.B0	9A2
ECL.A.D0	I	116	4/2		DCLASSI0	11A5
ES.LOF0	I	117	7/22		OSTBSSI0	11A3
E2.LOF0	I	317	5/13		DCLBSSI0	11A4
FA204R31	I	IC	3/9		F204R31	9A2
FA204R51	I	IC	3/9		F204R51	10A6
FA304R81	I	IC	3/9		F304R81	10E0
FA304RD1	I	IC	3/9		F304RD1	10A4
FA304RE1	I	IC	3/9		F304RE1	11A2
FA304R71	I	IC	3/9		F304R71	10A2
F104L80	I	003	1/13		F104L80	10A0
F204L30A	I	107	1/13		F204L30	9A2
IGB00E0	O	IC	3/9		TA8	10H4
IGB00F0	O	IC	3/9		TB8	10H3
IGB001C	I	IC	3/9		GB.AD1C	10A4
IGB001D	I	IC	3/9		GB.AD1D	9E0
IGB001E	I	IC	3/9		GB.AD1A	10A6
IGB08E0	O	IC	3/9		TA9	10G7
IGB08F0	O	IC	3/9		TB9	10G7
IGB081C	I	IC	3/9		GB.BD1C	10A3
IGB081D	I	IC	3/9		GB.BD1D	9E0
IGB081E	I	IC	3/9		GB.BD1A	10A5
INTPRS0	OT	204	5/7,5/8 5/9,5/10 5/11,5/12 5/13		MK.ISAG	11H7
	I		5/3			
	OT	004	5/14		MK.ISB0	11H7
IS000	I	106	TO CONN CKT		DSTISAI0	10A2
IS080	I	306	TO CONN CKT		DSTISBI0	10A1
MCHGB000	OT	304	5/2	202	GSS.A10C	11H6
MCHGB080	OT	104	5/2	202	GSS.B10C	11H4
MCSSMCH0	I	207	9/4		GSS.MCH0	11A1
MD.ZMS0	I	018	1/14		CLRMSI0	10A6
MODML1C0	I	219	1/12		DML1.CI0	9A1
MS000	O	109	7/20		MS.A10	10H6
MS080	O	309	4/1,4/3		MS.B10	10H5
SSAME0A	O	010	7/7	202	SS.A10A	11H5
SSLOF0A	O	210	6/2.7/20	202	SS.B10A	11H4
SSLOF0B		115			SS.B108	11H4
ST.CR000	I	318	9/4		DSET.CA0	9A4
ST.CR080		019			DSET.CB0	9A3
TA204R31	I	IC	3/9		T204R31	9A2
TA204R51	I	IC	3/9		T204R51	10A6
TA204R61	I	IC	3/9		T204R61	9A5
TA204R91	I	IC	3/9		T204R91	9A6
TA304R81	I	IC	3/9		T304R81	11A1
TA304RD1	I	IC	3/9		T304RD1	10A5
TA304RE1	I	IC	3/9		T304RE1	11F0
TA304R71	I	IC	3/9		T304R71	10A3
T104L80	I	011	1/11		T104L80	11A2
T204L30A	I	009	1/11		T204L30	11A6

PART OF FS 5
SYMBOL(S) 12 13 14

3A CENTRAL CONTROL

DWG SIZE C2
ISSUE 5A

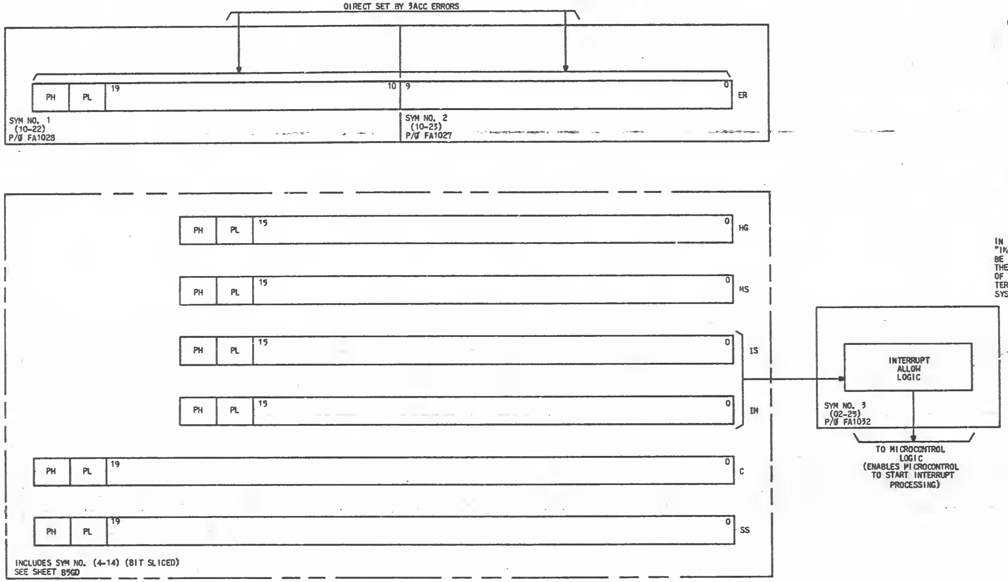
BELL LABORATORIES
SD-1C900-01
B5CD
06/10/77
PRINTED IN U. S. A.

PART OF FS 5

SPECIAL REGISTERS

COMPOSITE DIAGRAM 1

FUNCTION PARTITION OF SPECIAL REGISTERS



CIRCUIT OPERATION

FS 5 CONTAINS A NUMBER OF SPECIAL REGISTERS THAT ARE DEDICATED FOR UNIQUE FUNCTIONS WITHIN THE 3ACC. NOTE THAT THESE SPECIAL REGISTERS ARE NOT DIRECTLY RELATED TO THE SPECIAL REGISTER SET THAT IS DEFINED IN 3ACC CENTRAL PANEL. THE FUNCTION OF THE SPECIAL REGISTERS IN FS 5 IS AS FOLLOWS:

(1) ER - THE ERROR REGISTER BUFFERS ALL OF THE ERRORS FROM CHECK CIRCUITS WITHIN THE 3ACC AS WELL AS THE CHECK CIRCUITS COMING FROM THE MAIN STORE.

(2) HG - THE HOLD GET REGISTER SAVES A POINTER INTO CALL STORE (TEMPORARY MEMORY) IN THE MAIN STORE THAT INDICATES THE LEVEL AT WHICH EACH SUBROUTINE IS EXECUTING. AS EACH SUBROUTINE IS CALLED THE HOLD GET LEVEL IS DECREMENTED, AND THE HG REGISTER POINTS TO A STARTING ADDRESS OF A BLOCK OF 16 WORDS THAT USED TO SAVE THE PRESENT STATE OF THE MACHINE.

(3) MS - THE MS REGISTER BUFFERS MAINTENANCE STATES THAT ARE USED TO SET UP TEST CONDITIONS WITHIN THE 3ACC. THESE TEST CONDITIONS ARE USED BY DIAGNOSTIC PROGRAMS TO IDENTIFY THE LOCATION OF FAILING HARDWARE.

(4) IS - THE INTERRUPT STATUS REGISTER BUFFERS INTERRUPTS. EACH BIT OF THE IS IS ASSIGNED A PRIORITY. THE LOWER THE BIT POSITION IN THE IS, THE HIGHER THE PRIORITY OF THE INTERRUPT.

(5) IM - THE INTERRUPT MASK-REGISTER ALLOWS INTERRUPTS TO BE MASKED OR BLOCKED SO THAT AN INTERRUPT OF HIGHER PRIORITY MAY BE SERVICED.

(6) CR - THE C REGISTER IS A 20-BIT REGISTER THAT IS USED AS A GENERAL PURPOSE REGISTER FOR THE MICROPROGRAMMER. IT IS TYPICALLY USED TO BUFFER THE RESULTS OF DML OPERATIONS.

(7) SS - THE SYSTEM STATUS REGISTER IS A 20-BIT REGISTER THAT CONTAINS SYSTEM STATE INFORMATION.

IN ADDITION TO THE SPECIAL REGISTERS, FS 5 CONTAINS THE "INTERRUPT ALLOW" LOGIC THAT DETERMINES WHEN AN INTERRUPT CAN BE SERVICED. THAT IS, INTERRUPTS CAN ONLY BE SERVICED WHEN THE BIN (BLOCK INTERRUPTS) FLIP-FLOP IS CLEARED. THE SETTING OF BIN BY THE INTERRUPT SERVING MICROCODE PERMITS ANY INTERRUPT, INDEPENDENT OF ITS PRIORITY, TO BE RECORDED INTO THE SYSTEM ONCE THE INTERRUPT HAS BEEN RECOGNIZED.

PART OF FS 5
COMPOSITE DIAGRAM 1

3A CENTRA' ONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B5GA

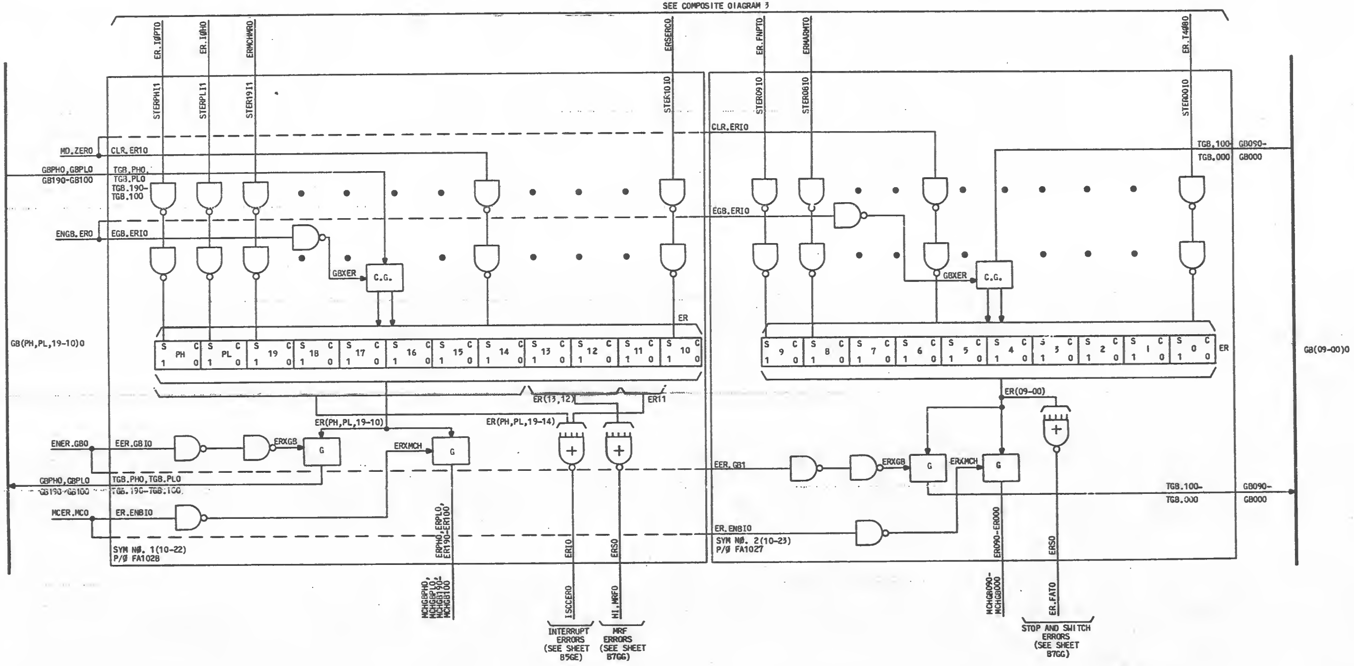
PART OF FS 5

SPECIAL REGISTERS

COMPOSITE DIAGRAM 2

ERRØR (ER) REGISTER
ØUTPUT FRØM 3A CC CHECK
CIRCUITS SET BITS IN ER DIRECTLY

CIRCUIT OPERATION
(SEE SHEET B5GC)



PART ØF FS 5
CØMPØSITE DIAGRAM 2

3A CENTRAL CØNTRØL ②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES | SD-IC900-01 | B5GB

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COMPOSITE DIAGRAM 3

ERROR (ER) REGISTER

OUTPUT FROM 3A CC CHECK CIRCUITS SET BITS IN ER DIRECTLY

TERM. MOD.	NETNAME (PIN NO.)	TYPE OF ERROR CIRCUIT	
STER00I0	ER.T4080 (216)	TO-FIELD 4-OUT-OF-8 DECODER ERROR	"STOP AND SWITCH" CLASS
STER01I0	ER.F4080 (116)	FROM-FIELD 4-OUT-OF-8 DECODER ERROR	
STER02I0	ER.IBPLu (117)	IB PARITY ERROR (PL FIELD ONLY)	
STER03I0	ER.GBPTO (317)	GATING BUS PARITY ERROR	
STER04I0	ER.DMLO (018)	DML MATCH ERROR	
STER05I0	ERMARPTO (218)	MAR PARITY ERROR	
STER06I0	ER.CLKO (118)	CC CLOCK ERROR	
STER07I0	ERSOERAO (318)	MY STORE ERROR A *	
STER08I0	ERMARMTO (019)	MAR-RAR MATCHER ERROR	
STER09I0	ER.FNPTO (219)	FUNCTION REGISTER (DML) ERROR	
STER10I1	ERSERCO (008)	MY STORE AND OTHER STORE ERROR C (READ PARITY ERROR)	
STER11I1	ERSOERBO (208)	MY STORE ERROR B (WRITE PROTECT ERROR)	INTERRUPT CLASS
STER12I1	ER.SOTO0 (108)	MY STORE FAST TIME OUT (≈ 38-50 US.)	MRF CLASS
STER13I1	ER.BACKO (308)	BRANCH ALLOWED ERROR	
STER14I1	ERS1ERBO (100)	OTHER STORE ERROR A *	INTERRUPT CLASS
STER15I1	ERS1ERAO (300)	OTHER STORE ERROR B (WRITE PROTECT)	
STER16I1	ER.S1TO0 (001)	OTHER STORE FAST TIMEOUT (≈ 38-50 US.)	
STER17I1	ER.IOCSO (201)	I/O MULTIPLE MAIN CHANNEL SELECT ERROR	
STER18I1	ERMCHPTO (101)	PROGRAM TIMER ERROR RECEIVED BY ON-LINE CC	
STER19I1	ERMCHMRO (301)	SWITCH ERROR RECEIVED BY ON-LINE CC	
STERPLI1	ER.IOHO (002)	I/O CHANNEL ERROR **	
STERPHI1	ER.IOPTO (202)	I/O PARITY ERROR	

* STORE ERROR A INCLUDES ALL MAIN STORE ERRORS OTHER THAN READ PARITY ERRORS AND WRITE PROTECT ERRORS.

** INCLUDES ALL INTERNAL I/O CHANNEL ERRORS PLUS THE I/O-DML MATCH ERROR.

CIRCUIT OPERATION (CONT)

THESE ERRORS ON AN INTERRUPT BASIS. NOTE THAT EACH 3A CC CONTAINS ITS OWN ER REGISTER, AND THEREFORE, IT IS POSSIBLE FOR THE OFF-LINE 3A CC TO INCUR A FATAL ERROR, A MRF ERROR OR AN INTERRUPT ERROR. (A READ PARITY ERROR IS NOT NORMALLY POSSIBLE IN THE OFF-LINE 3A CC SINCE IT IS TYPICALLY IN A MICROCODE LOOP IN WHICH MAIN STORE IS NOT BEING ACCESSED.) IF THESE ERRORS OCCUR IN THE OFF-LINE THEY WILL INVOKE A DIFFERENT RECOVERY STRATEGY THAN IN THE ON-LINE. FOR EXAMPLE, A FATAL ERROR IN THE OFF-LINE WILL INITIATE A "STOP AND SWITCH". THE SWITCH WILL BE TRANSMITTED TO THE OTHER 3A CC AND INSTEAD OF IT INITIALIZING, THE SWITCH MESSAGE WILL CAUSE AN INTERRUPT ERROR (BIT 19 OF ER) TO THE 3A CC THAT IS ALREADY ON-LINE. THUS, THE OPERATION OF THE ER IS IDENTICAL IN BOTH THE ON-LINE 3A CC'S, BUT THE ACTION TAKEN IN ERROR RECOVERY IS DEPENDENT UPON THE STATE OF THE 3A CC'S WHEN THE ERRORS OCCUR.

ERROR BIT 10, THE READ PARITY ERROR IN A STORE, CAUSES AN AUTOMATIC RECOVERY SEQUENCE THAT IN MOST CASES IS COMPLETELY AUTONOMOUS AND TRANSPARENT TO SOFTWARE. FOR EXAMPLE, WHEN THE SYSTEM IS IN THE DUPLEX MODE AND THE DOUBLE STORE READ RECOVERY MECHANISM IS USED, THE STORE ERROR C WILL TRIGGER A REREAD OF THE OFF-LINE STORE. IF THAT WORD CAN BE READ CORRECTLY, NO OTHER SYSTEM RECOVERY IS TAKEN AND NORMAL PROCESSING CONTINUES WITH SUBSEQUENT READS COMING FROM THE ON-LINE STORE. FOR A STORE ERROR C THAT OCCURS WHEN IN SIMPLEX MODE, A TECHNIQUE CALLED COMPLEMENT CORRECTION IS USED. THIS TECHNIQUE INVOKES A SPECIAL MICROCODE ROUTINE THAT ATTEMPTS TO CORRECT THE WORD IN THE ON-LINE STORE, AND IF THIS CORRECTION CAN BE MADE, NO OTHER RECOVERY MECHANISM IS INVOKED (SEE SHEET 011).

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2 AND 3

COMPOSITE DIAGRAM 2 SHOWS THE ER REGISTER AND THE VARIOUS INPUTS AND OUTPUTS FROM THE ER REGISTER. AS SHOWN, THERE ARE 22 BITS IN THE ER REGISTER THAT ARE USED TO BUFFER THE OUTPUT OF THE CHECK CIRCUITS WITHIN THE 3A CC AS WELL AS SOME OF THE ERRORS COMING FROM THE MAIN STORE. COMPOSITE DIAGRAM 3 LISTS EACH OF THESE ERRORS, THE NETNAME OF EACH OF THESE SIGNALS, AND THE TYPE OF ERROR CIRCUIT THAT ACTIVATES EACH OF THEM.

IN ADDITION TO THE DIRECT SET OF EACH BIT OF THE ER REGISTER FROM THE INDIVIDUAL CHECK CIRCUITS, THE ER REGISTER CAN BE LOADED FROM THE GB WITH THE NORMAL TO-FIELD CONTROL. ALSO, THE ERROR REGISTER CAN BE READ BY GATING IT ONTO THE GB WITH THE FROM-FIELD CONTROL. IN ADDITION, THE ER REGISTER HAS TWO CONTROL SIGNALS THAT ARE UNIQUE TO IT. ONE IS A SPECIAL SIGNAL THAT ALLOWS THE ERROR REGISTER TO BE CLEARED VIA A MISCELLANEOUS DECODER CROSSPOINT. THE SECOND IS A CONTROL SIGNAL THAT ORIGINATES FROM THE MAINTENANCE CHANNEL (NETNAME MCER.MCO) THAT ALLOWS THE ER REGISTER TO BE GATED TO THE MAINTENANCE CHANNEL. THIS ALLOWS THE ER REGISTER IN ONE 3A CC TO BE READ WITHOUT DISTURBING THE 3A CC WHOSE ER IS TO BE OBTAINED.

THE OTHER IMPORTANT ASPECT OF THE ER REGISTER IS THE LOGIC ATTACHED TO THE OUTPUT OF GROUPS OF BITS IN THE ER REGISTER. THE BITS IN ER REGISTER ARE PLACED IN GROUPS OR CLASSES SO THAT APPROPRIATE ERROR RECOVERY PROCEDURE CAN BE USED FOR EACH GROUP OF ERRORS. THE FIRST AND MOST SERIOUS CLASS OF ERRORS ARE FORMED BY BITS 0-9 OF THE ER. NOTE THAT THESE BITS INPUT INTO AN OR GATE. THE OUTPUT OF THIS GATE IS USED AS A SIGNAL THAT WILL "STOP AND SWITCH" A 3A CC IF ANY ONE OF THE BITS ARE ACTIVATED IN THE ER REGISTER. THIS CLASS OF ERRORS IS KNOWN AS THE "FATAL ERRORS". A FATAL ERROR WILL TYPICALLY CAUSE A "STOP AND SWITCH" OF THE ON-LINE 3A CC UNLESS THE BLOCK HARDWARE CHECK FLIP-FLOP IS SET OR THE ON-LINE IS "LOCKED ON-LINE" (SEE SHEET B7GG FOR ADDITIONAL DETAILS).

ANOTHER CLASS OF ERRORS IS THE "READ PARITY ERROR" ORIGINATING FROM THE MAIN STORE. BIT 10 OF THE ER REGISTER IS USED TO BUFFER THE READ PARITY ERROR SIGNAL, STORE ERROR C, COMING FROM THE MAIN STORE. STORE ERROR C WILL INITIATE, DEPENDING UPON WHETHER THE 3A CC IS OPERATING IN A DUPLEX OR A SIMPLEX MODE, EITHER THE DOUBLE STORE READ OR THE COMPLEMENT CORRECTION ERROR CORRECTION TECHNIQUE. BOTH OF THESE TECHNIQUES WILL ATTEMPT TO CORRECT THE WORD ON WHICH THE READ PARITY ERROR WAS FOUND. IF SUCCESSFUL, INSTRUCTION PROCESSING FLOW WILL CONTINUE UNINTERRUPTED (FOR ADDITIONAL DETAILS SEE SHEET B4GM).

BITS 11 THROUGH 13 FORM ANOTHER CLASS OF ERRORS CALLED THE "MRF" CLASS. IF ANY ONE OF THE ERRORS IN THIS GROUP ARE ACTIVE, THE 3A CC, CONTAINING THIS ERROR WILL INITIALIZE. SIMILAR TO THE FATAL ERRORS A 3A CC WILL INITIALIZE ONLY IF BLOCK HARDWARE CHECK IS NOT SET. (SEE SHEET B7GG).

BITS 14 THROUGH 19 PLUS PL AND PH OF THE ER REGISTER FORM THE "INTERRUPT" CLASS OF ERRORS. THESE ERRORS WILL GENERATE AN INTERRUPT. THE INTERRUPT THAT IS GENERATED, IS INTERRUPT LEVEL 5, (i.e., SIGNAL ERI 0 SETS BIT 5 OF THE IS REGISTER).

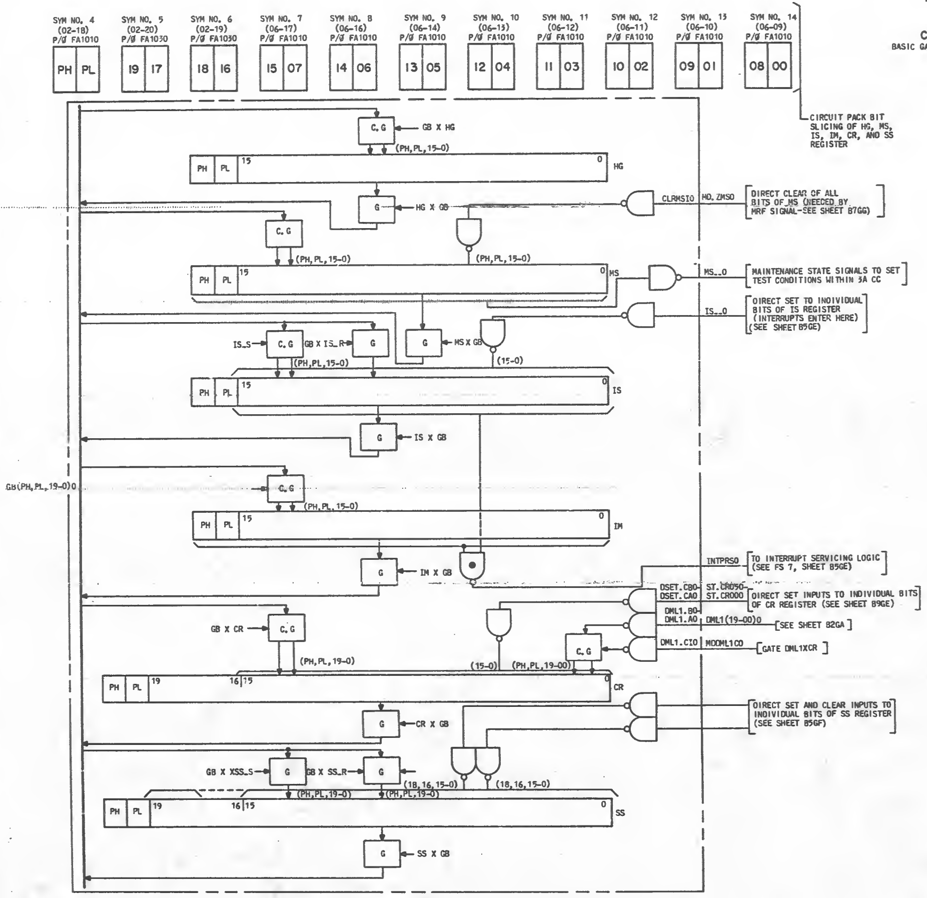
THE PARTITIONING OF THE BITS OF THE ER REGISTER IN THE MANNER DESCRIBED ALLOWS SYSTEM RECOVERY PROCEDURES TO BE MATCHED TO THE SERIOUSNESS OF THE ERROR THAT HAS OCCURRED. FOR EXAMPLE, THE FATAL ERRORS ARE TYPICALLY CAUSED BY A PROBLEM IN THE ON-LINE 3A CC THAT WILL PREVENT IT FROM CONTINUING TO EXECUTE PROPERLY. THEREFORE, A "STOP AND SWITCH" TO THE OTHER 3A CC IS IN ORDER. THE MRF TYPE OF ERROR RESULTS IN INITIALIZING THE 3A CC IN WHICH THE MRF ERROR OCCURRED. THIS TYPE OF ERROR MAY BE CAUSED BY AN ABNORMAL SOFTWARE STATE OR POSSIBLY AN ERROR IN THE OFF-LINE STORE WHICH WAS CAUSED WHEN ISSUING WRITES TO BOTH STORES. HENCE, THE INITIALIZATION OF THE ON-LINE 3A CC SHOULD BE PERFORMED INSTEAD OF SWITCHING TO THE OFF-LINE WHICH MAY HAVE A PROBLEM IN ITS STORE. THE INTERRUPT CLASS OF ERRORS ARE TYPICALLY ERRORS THAT ARE GENERATED FROM HARDWARE, EXTERNAL TO THE CORE OF THE 3A CC, FOR EXAMPLE, I/O PARITY ERRORS. THESE ERRORS DO NOT NECESSARILY INHIBIT A 3A CC FROM EXECUTING PROPERLY AND, THEREFORE, CAN BE TREATED IN A MORE GRACEFUL MANNER THAN A "STOP AND SWITCH" OR AN INITIALIZATION. HENCE, LESS INFORMATION OR DISRUPTION TO NORMAL SYSTEM OPERATION IS CAUSED BY TREATING

PART OF FS 5
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B5GC

PART OF FS 5
SPECIAL REGISTERS

COMPOSITE DIAGRAM 4
BASIC GATING PATHS FOR SPECIAL REGISTERS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SYM NO. 8 (06-16) P/0 FA1010 14 06
SYM NO. 9 (06-14) P/0 FA1010 13 05
SYM NO. 10 (06-13) P/0 FA1010 12 04
SYM NO. 11 (06-12) P/0 FA1010 11 03
SYM NO. 12 (06-11) P/0 FA1010 10 02
SYM NO. 13 (06-10) P/0 FA1010 09 01
SYM NO. 14 (06-09) P/0 FA1010 08 00
CIRCUIT PACK BIT SLICING OF HG, MS, IS, IM, CR, AND SS REGISTER
C, G
GB X HG
(PH, PL, 15-0)
HG
G
HG X GB
CLRMSI0
MO.ZMSO
DIRECT CLEAR OF ALL BITS OF MS (NEEDED BY MRF SIGNAL-SEE SHEET B7GG)
(PH, PL, 15-0)
MS
MS..0
MAINTENANCE STATE SIGNALS TO SET TEST CONDITIONS WITHIN 3A CC
IS..0
DIRECT SET TO INDIVIDUAL BITS OF IS REGISTER (INTERRUPTS ENTER HERE) (SEE SHEET B5GE)
IS-S
GB X IS-R
MS X GB
(15-0)
IS
IS X GB
GB(PH, PL, 19-0)0
IM
IM X GB
INTPRSO
TO INTERRUPT SERVICING LOGIC (SEE FS 7, SHEET B5GE)
DSET.CB0
DSET.CA0
ST.CR050
ST.CR000
DIRECT SET INPUTS TO INDIVIDUAL BITS OF CR REGISTER (SEE SHEET B9GE)
DML1.B0
DML1.A0
DML1(19-00)0
SEE SHEET B2GA
DML1.CI0
MDDML1C0
GATE DML1XCR
GB X CR
(PH, PL, 19-0)
(15-0)
(PH, PL, 19-00)
19
16
15
0
CR
CR X GB
DIRECT SET AND CLEAR INPUTS TO INDIVIDUAL BITS OF SS REGISTER (SEE SHEET B5GF)
GB X XSS-S
GB X SS-R
(18, 16, 15-0)
(PH, PL, 19-0)
SS
SS X GB

CIRCUIT OPERATION

COMPOSITE DIAGRAM 4 OUTLINES THE BASIC GATING PATHS FOR THE SPECIAL REGISTERS OTHER THAN THE ER. AS INDICATED ALL OF THE SPECIAL REGISTERS HAVE THE NORMAL ACCESS TO THE GB USING THE TO AND FROM FIELD. TABLE A SHOWS THE TO-AND FROM-FIELD ASSIGNMENTS FOR EACH OF THESE SPECIAL REGISTERS.

THE IS AND SS REGISTERS REQUIRE SPECIAL TO-FIELD CROSSPOINTS. WHEN THE NORMAL METHOD OF GATING WITH THE CLEAR AND GATE TECHNIQUE IS USED, THE REGISTER THAT IS GATED INTO CAN PASS THROUGH INTERMEDIATE STATES. FOR EXAMPLE, IF A REGISTER CONTAINS ALL ONES AND IT IS TO BE LOADED WITH ALL ONES FROM THE GB, IT IS POSSIBLE FOR THE REGISTER TO MOMENTARILY GO TO ALL ZEROS BEFORE ALL ONES ARE LOADED INTO IT FROM THE GB. SINCE THE IS AND THE SS REGISTERS HAVE THEIR OUTPUTS DIRECTLY CONNECTED TO LOGIC THAT WILL NOT PERMIT THESE TRANSIENT TYPE CONDITIONS, A SPECIAL GATING TECHNIQUE IS PROVIDED WHEN GATING TO THESE TWO REGISTERS. THIS TECHNIQUE CONSISTS OF ASSIGNING A TO FIELD THAT PERMITS GATING TO THE SET SIDE ONLY OF THE SS (OR IS) REGISTER AND ANOTHER TO FIELD THAT PERMITS GATING TO THE RESET SIDE ONLY OF SS (OR IS) REGISTER. BY PLACING DATA ON THE GB THAT CORRESPONDS TO THE BIT POSITION OF THE REGISTER THAT IS TO BE SET OR CLEARED AND THEN ENABLING AN APPROPRIATE TO-FIELD CROSSPOINT, INDIVIDUAL OR GROUPS OF THESE REGISTER BITS CAN BE SET OR CLEARED WITHOUT CAUSING A MOMENTARY CHANGE OF STATE.

BECAUSE OF THE CRITICAL NATURE OF THE MS REGISTER (ITS EFFECTS ON THE NORMAL OPERATION OF THE ON-LINE 3A CC) IT HAS A SPECIAL CLEAR INPUT [MO.ZMSO] WHICH IS USED TO CLEAR THE MS REGISTER DURING INITIALIZATION. ALSO, THERE ARE DIRECT OUTPUTS FROM EACH BIT OF THE MS REGISTER THAT ARE DISTRIBUTED THROUGHOUT THE 3A CC TO SET UP MAINTENANCE STATE CONDITIONS TO AID IN SOFTWARE DIAGNOSTICS.

THE C REGISTER IS USED AS A GENERAL PURPOSE REGISTER FOR THE MICROPROGRAMMER. IT ALSO HAS A SPECIAL INPUT FROM DML1 TO IT TO ALLOW THE REDUNDANT COPY OF THE DML LOGIC TO BE GATED INTO IT. THIS IS USED FOR MAINTENANCE PURPOSES TO GAIN ACCESS TO DML1. NOTE THAT DML0 INPUTS TO THE GB WHEREAS DML1 ONLY INPUTS TO THE DML MATCHER WHICH INSURES THAT DML1 AND DML0 PERFORM IDENTICAL FUNCTIONS. HENCE, MAINTENANCE ACCESS IS REQUIRED FOR DML1. IN ADDITION, THERE ARE DIRECT SET INPUTS TO THE LOW-ORDER BITS OF THE CR REGISTER THAT ARE USED IN CONJUNCTION WITH THE MAINTENANCE CHANNEL (MCH). A CONTROL FUNCTION IN THE MCH ALLOWS VARIOUS STATES CONTAINED WITHIN THE MCH TO BE GATED TO THE CR REGISTER. NOTE THAT THIS FUNCTION ONLY SETS BITS OF THE CR REGISTER. THEREFORE, BEFORE THIS FUNCTION CAN BE USED, THE CR REGISTER MUST BE CLEARED IN ORDER TO OBTAIN VALID RESULTS. THIS FUNCTION IS ONLY PERFORMED IN AN OFF-LINE 3A CC.

THE HG REGISTER HAS NO OTHER ACCESS EXCEPT FOR THE NORMAL TO- AND FROM-FIELD CONTROL ACCESS TO THE GB. THE HG IS MAINLY MANIPULATED BY THE MICROPROGRAMMER. THAT IS, THE MAIN MEMORY PROGRAMMER CANNOT CHANGE ITS CONTENTS. THE ONE EXCEPTION TO THIS IS VIA MICROINTERPRET WHICH ALLOWS MAIN MEMORY INITIALIZATION PROGRAMS TO PRESET THE HG LEVEL. FROM THAT POINT ON, WITH A FEW EXCEPTIONS, THE HG TENDS TO BE DECREMENTED OR INCREMENTED ONLY BY THE MICROPROGRAMMER WHEN SUBROUTINES ARE INVOLVED. FOR A DETAILED DESCRIPTION OF THE SS AND THE IS, IM REGISTERS, SEE SHEET B5GF AND B5GE RESPECTIVELY.

TABLE A

TO-AND-FROM FIELD DECODER ASSIGNMENTS

SPECIAL REGISTER	GB X SPECIAL REGISTER (TO-FIELD PAIR) NETNAME (PIN N0.)	SPECIAL REGISTER X GB (FROM-FIELD PAIR) NETNAME (PIN N0.)
HG	T204L30A (009), T204R50A (013)	F204L30A (107), F204R50A (110)
MS	T104L80 (011), T304RD0A (301)	F104L80 (003), F304RD0A (300)
IS-S	T204L30A (009), T204R90A (112)	F104L80 (003), F304RB0B (001)
IS-R	T204L30A (009), T204R60A (312)	
IM	T104L80 (011), T304R7A0 (202)	F104L80 (003), F304R70A (201)
CR	T204L30 (009), T204R30A (213) XT204L30B (117), T204R30C (118)	F204L30A (107), F204R30A (310) XF204L30B (213), F204R30C (311)
SS-S	T104L80 (011), T304RE0A (101) XT104L80 (015), T304RE06 (115)	F104L80 (003), F304RE0A (100) XF104L80 (312), F304RE0B (013) F304RE0A (013)
SS-R	T104L80 (011), T304RB0A (002) XT104L80 (015), T304RB0B (215)	

X SYM NO. 5 AND 6
(02-19 AND 02-20)

PART OF FS 5
COMPOSITE DIAGRAM 4

3A CENTRAL CONTROL
DWG SIZE 6S
ISSUE 5A
BELL LABORATORIES
SD-1C900-01
B5GD

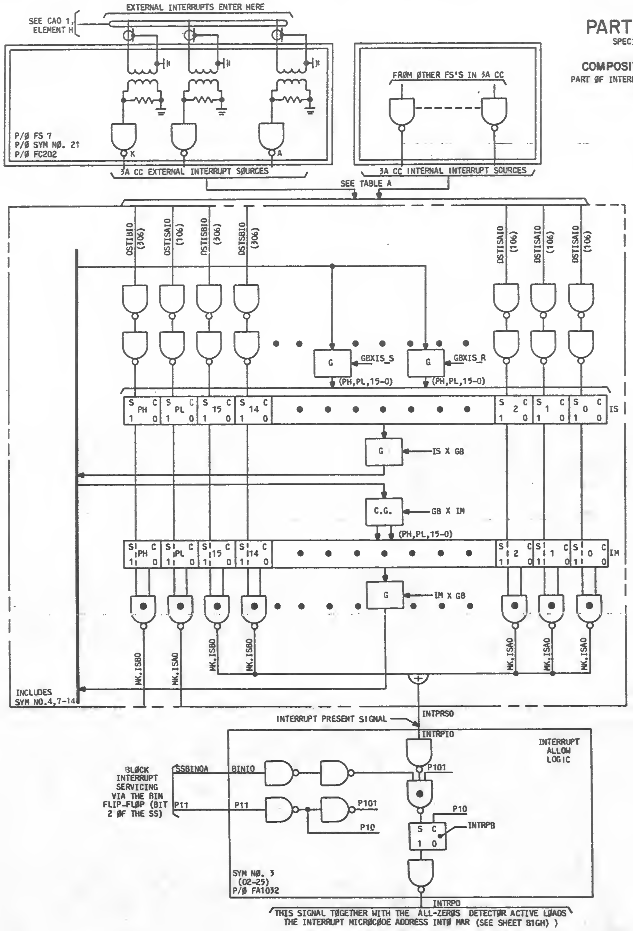
E-7621 (12-73)
PRINTED IN U.S.A.

PART OF FS 5

SPECIAL REGISTERS

COMPOSITE DIAGRAM 5

PART ØF INTERRUPT LØGIC (IM AND IS)



CIRCUIT OPERATION

ALL INTERRUPTS THAT ENTER THE 3A CC ARE BUFFERED IN A REGISTER CALLED INTERRUPT SET REGISTER (IS). THEREFORE, EACH BIT OF THE IS REGISTER HAS A DIRECT SET INPUT THROUGH WHICH AN INTERRUPT ENTERS. NOTE THAT THE IS REGISTER HAS 16 DATA BITS AND AS SUCH THERE ARE 16 DIFFERENT INTERRUPT LEVELS. THE LEVELS ARE ASSIGNED POSITIONAL PRIORITY WITH THE LOW-ORDER BIT OF THE IS (BIT 0) BEING ASSIGNED THE HIGHEST PRIORITY INTERRUPT LEVEL. NOTE ALSO THAT THE TWO PARITY BITS OF THE IS REGISTER CANNOT BE USED TO BUFFER INTERRUPTS.

THERE ARE TWO MAJOR SOURCES OF INTERRUPTS. THOSE THAT COME FROM INTERNAL SOURCES AND THOSE INTERRUPTS THAT COME FROM EXTERNAL SOURCES. THE EXTERNAL SOURCES ARE TYPICALLY BUFFERED THROUGH TRANSFORMERS THAT PERFORM AN ISOLATION FUNCTION ON SIGNALS ENTERING THE 3A CC. THIS ISOLATION PREVENTS FAULTS THAT MAY OCCUR AT THE INTERRUPT SOURCE FROM EFFECTING THE 3A CC ITSELF. THE TYPICAL EXTERNAL INTERRUPT SOURCES ARE THE TTY AND THE TDC. ONE OF THE EXTERNAL SOURCES THAT IS NOT BUFFERED THROUGH A TRANSFORMER IS THE INTERRUPT FROM THE OTHER 3A CC. THIS INTERRUPT OBTAINS ITS ISOLATION BY GOING THROUGH THE BUS PROTECTION CIRCUITRY SHOWN IN FS 13 AND THEREFORE, THE TRANSFORMER ISOLATION SHOWN IN SYMBOL 17 OF FS 7 IS NOT REQUIRED. TABLE A SHOWS EACH OF THE 16 INTERRUPT LEVELS, THE NETNAME OF THE SIGNAL THAT INPUTS TO EACH OF THESE INTERRUPT LEVEL POSITIONS, AND WHETHER THEY ARE EXTERNAL OR INTERNAL SOURCES. IT ALSO DESCRIBES THE FUNCTION OF EACH OF THE INTERRUPT SOURCES. NOTE THAT INTERRUPTS ARE GENERATED FROM PULSED SOURCES (≈ 150-NS TO 5-US PULSE WIDTH). IF AN INTERRUPT IS A DC LEVEL IT WILL BE TREATED AS A STUCK INTERRUPT AND THE APPROPRIATE ACTION WOULD BE TAKEN (i.e., IM BIT WILL BE SET).

IN ADDITION TO THE IS REGISTER, AN IM REGISTER IS USED. THE PURPOSE OF THE IM REGISTER IS TO PROVIDE THE CAPABILITY OF INHIBITING ANY GIVEN INTERRUPT LEVEL FROM OCCURING. THIS TYPICALLY ALLOWS HIGHER PRIORITY INTERRUPTS TO INHIBIT THE SERVICING OF LOWER PRIORITY INTERRUPTS UNTIL THE HIGHER PRIORITY INTERRUPT HAS BEEN COMPLETELY FINISHED. AS SHOWN IN COMPOSITE DIAGRAM 5, THE INHIBITING OF THE INDIVIDUAL BITS OF THE IS BY THE IM IS PERFORMED WITHIN THE BIT SLICED CIRCUIT PACKS. ONLY THE OR OF THE AND OF EACH OF THE RESPECTIVE BITS OF THE IS AND THE IM REGISTERS APPEAR ON THE BACKPLANE ON A NET CALLED INTPRSO. WHEN THIS NET IS ACTIVATED (i.e., LOW) AN INTERRUPT HAS ENTERED THE IS AND IT IS NOT BLOCKED FROM BEING SERVICED BY THE IM. THE SIGNAL THEN ENTERS THE "INTERRUPT ALLOW" LOGIC SHOWN IN SYMBOL 3.

TABLE A

INTERRUPT BIT PØSITIØN	NETNAME (INTØ IS)	SØURCE INTERNAL(IN) ØR EXTERNAL(EX)	FUNCTIØN
0	IS000	————	SPARE **
1	ISUTILO	EX	UTILITY SYSTEM INTERRUPT (TEST INPUT)
2	IS020	————	SPARE **
3	ISPANMTO	IN	3A CC PANEL MATCH INTERRUPT
4	IS040	————	SPARE **
5	ISCCERO	IN	3A CC ERRØR CIRCUIT INTERRUPT
6	IS060	————	SPARE **
7	ISØCCIO	* EX	ØTHER 3A CC INTERRUPT
8	IS080	————	SPARE **
9	IS090	————	SPARE **
10	ISTTYEO	EX	INTERRUPT FRØM EVEN TTY'S ØR TDC
11	ISTTYØO	EX	INTERRUPT FRØM ØDD TTY'S ØR TDC
12	IS120	————	SPARE **
13	ISPANLO	IN	3A CC PANEL INTERRUPT
14	IS140	————	SPARE **
15	IS150	————	SPARE **
PL	———(CANNØT BE ASSIGNED)———		
PH	———(CANNØT BE ASSIGNED)———		

* THIS EXTERNAL INTERRUPT ØRIGINATES FRØM THE ØTHER 3A CC AND IT IS TRANSMITTED BY ØNE ØF THE SPARE SIGNAL LEADS IN THE MAIN STØRE BUS. IT IS THE ØNLY EXTERNAL INTERRUPT THAT IS NØT ISØLATED BY TRANSFØRMER CØUPLING, BUT SINCE THIS SIGNAL PASSES THRØUGH THE FUSE PRØTECTIØN PACKS (SEE SHT B13GA) IT IS ISØLATED FOR CATASTRØPHIC FAULTS (i.e. EXCESSIVE VØLTAGE)

** CONNECTORS ARE AVAILABLE FOR WIRING THESE SPARE INTERRUPTS TO THE INPUTS OF THE TRANSFORMERS. SEE CAD 1, ELEMENT H. ADDITIONAL WIRING MUST BE PROVIDED TO CONNECT THE SET INPUTS OF THE IS. SEE CAD 1, ELEMENT P.

CIRCUIT OPERATION (CONT)

THE INTERRUPT ALLOW LOGIC DETERMINES WHETHER ANY INTERRUPT CAN PRESENTLY BE SERVICED. A FLIP-FLOP CALLED THE BIN FLIP-FLOP IS USED TO INHIBIT ANY INTERRUPT FROM BEING SERVICED. THE PURPOSE OF THE BIN FLIP-FLOP IS TO ALLOW A GIVEN INTERRUPT THAT HAS BEEN STARTED TO BE SERVICED, TO FINISH THE INITIAL PROCESSING ON THE INTERRUPT BEFORE THE INSTRUCTION STREAM SERVICING THE INTERRUPT IS REINTERRUPTED. THAT IS, WHEN ANY INTERRUPT IS SERVICED, NO MATTER WHAT ITS PRIORITY, THERE IS SOME INITIAL BOOKKEEPING THAT MUST BE PERFORMED TO RECORD THE PRESENCE OF THAT INTERRUPT. THIS INITIAL BOOKKEEPING MUST BE PERFORMED IN ITS ENTIRETY BEFORE ANOTHER INTERRUPT IS ALLOWED INTO THE SYSTEM. THE SETTING OF BIN ALLOWS THIS INITIAL RECORDING TO TAKE PLACE. ONCE THIS RECORDING HAS TAKEN PLACE, BIN IS CLEARED BY A SOFTWARE CONTROL FUNCTION AND ANY INTERRUPTS THAT HAVE NOT BEEN MASKED BY THE IM REGISTER CAN THEN BE SERVICED. IN ADDITION, THE INTERRUPT ALLOW LOGIC PERFORMS A CLOCKING FUNCTION ON THE INTERRUPT PRESENT SIGNAL. THAT IS, SINCE INTERRUPTS CAN ENTER ASYNCHRONOUSLY TO THE BASIC TIMING IN A 3A CC, IT IS NECESSARY TO STROBE THE INTERRUPT PRESENT SIGNAL INTO A FLIP-FLOP (INTRPB) SO IT WILL BE STABLE AT THE TIME THE HARDWARE IN THE 3A CC SAMPLES FOR INTERRUPTS TO BE SERVICED.

INTERRUPTS IN THE 3A CC ARE SERVICED AT THE END OF INSTRUCTION SEQUENCES. THE END OF AN INSTRUCTION SEQUENCE IS SIGNIFIED BY HAVING ALL ZEROS IN THE NEXT ADDRESS FIELD OF THE LAST MICROSTRUCTION OF THAT INSTRUCTION SEQUENCE. FOR A DETAILED DESCRIPTION OF THE OPERATION OF THE ACTUAL SERVICING OF INTERRUPTS SEE SHEET B1GH.

PART ØF FS 5
CØMPØSITE DIAGRAM 5

3A CENTRAL CØNTRØL		DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01		B5GE

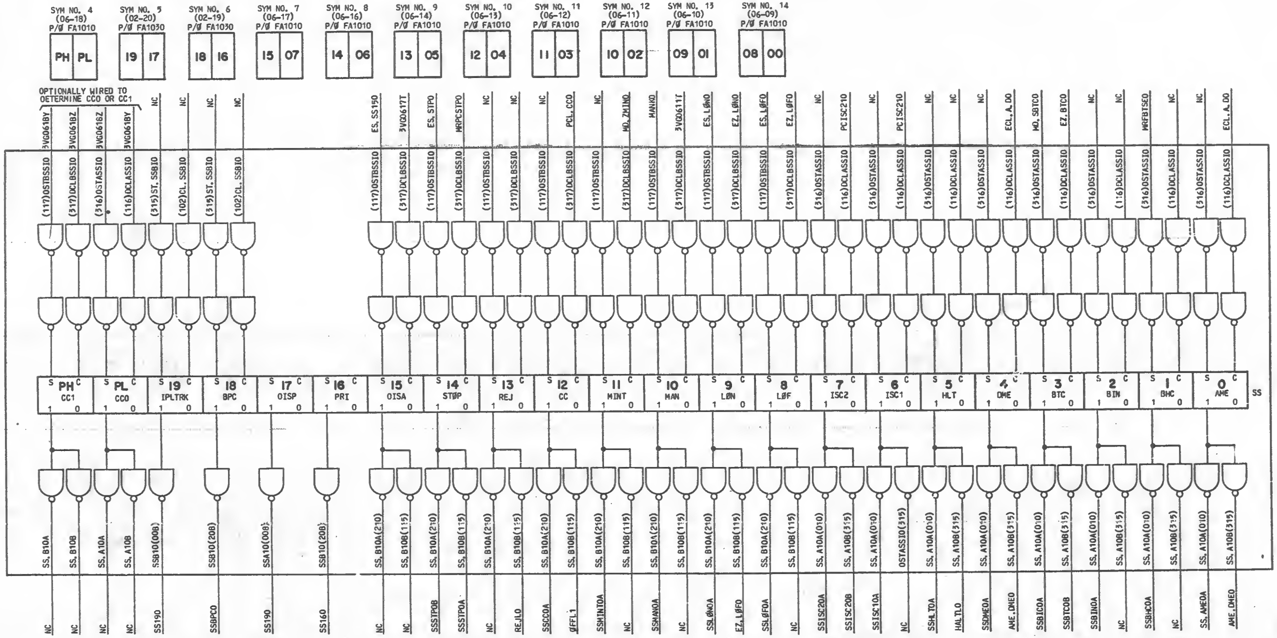
PART OF FS 5

SPECIAL REGISTERS

COMPOSITE DIAGRAM 6

SYSTEM STATUS REGISTER

CIRCUIT OPERATION
(SEE SHEET B5GG)



PART OF FS 5
COMPOSITE DIAGRAM 6

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	4A

BELL LABORATORIES

SD-1C900-01

B5GF

E-7021 (12-73)

PRINTED IN U.S.A.

PART OF FS 5

SPECIAL REGISTERS

CIRCUIT OPERATION FOR COMPOSITE DIAGRAM 6

THE SYSTEM STATUS (SS) REGISTER CONTAINS A NUMBER OF KEY STATUS FLIP-FLOPS USED BY THE 3A CC TO DEFINE BASIC MODES OR OPERATIONAL STATES OF THE SYSTEM. EACH BIT OF THE SS REGISTER, EXCEPT FOR BITS 16 AND 17, HAVE DIRECT SET AND DIRECT CLEAR INPUTS. THIS ALLOWS VARIOUS CONDITIONS OR CONTROL SIGNALS FROM THE 3A CC TO IMMEDIATELY EFFECT THE STATE OF THE RESPECTIVE BITS OF THE SS. ALSO, EACH OF THE BITS OF THE SS REGISTER HAVE A DIRECT OUTPUT THAT IS USED TO CONTROL VARIOUS MODES OR FUNCTIONS IN 3A CC. THE FOLLOWING IS A LIST OF THOSE BITS OF THE SS REGISTER AND A DEFINITION OF THEIR USE. THEY ARE LISTED IN THE ORDER THEY ARE CONTAINED IN THE SS.

AME - THE ADDRESS MATCH ENABLE BIT ENABLES THE ADDRESS MATCH REGISTERS. THE ADDRESS MATCH REGISTERS, THE AK AND THE AI REGISTERS ARE USED TO PERFORM ADDRESS MATCHES ON THE CONTENTS OF THE MAIN STORE ADDRESS BUS. IF A VALID MATCH OCCURS AND THE ADDRESS MATCH ENABLE BIT IS SET, AN INTERRUPT IS GENERATED (IS BIT 3). SEE SHEET B8GE FOR A DESCRIPTION OF THE ADDRESS MATCH REGISTERS.

BHC - THE BLOCK HARDWARE CHECK BIT IS USED TO INHIBIT THE OUTPUT OF HARDWARE CHECK CIRCUITS IN THE 3A CC. THIS INHIBITING ALLOWS THE ERROR TO BE RECORDED BUT DISALLOWS ANY AUTOMATIC ERROR RECOVERY PROCEDURES THAT MAY BE INVOKED, (SEE SHEET B7GG). NOTE THE BHC ONLY EFFECTS FATAL ERRORS AND MRF ERRORS AND DOES NOT EFFECT READ PARITY ERRORS OR INTERRUPT ERRORS. BOTH OF THESE RECOVERY STRATEGIES HAVE THEIR OWN INDIVIDUAL INHIBIT CAPABILITY.

BIN - THE BIN FLIP-FLOP PREVENTS ANY INTERRUPTS FROM BEING SERVICED UNTIL THE BIN FLIP-FLOP IS CLEARED, (SEE SHEET B5GE).

BTC - THE BLOCK TIMER CHECK FLIP-FLOP PREVENTS THE PROGRAM TIMER (PT) AND THE TIMING COUNTER (TC) FROM EXECUTING. WHILE THE BTC FLIP-FLOP IS SET NEITHER THE TC NOR THE PT REGISTERS WILL BE INCREMENTED. IN ADDITION, NO PT INITIALIZATION CAN TAKE PLACE. NOTE THAT THERE IS A SPECIAL BACKUP TIMER THAT WILL CLEAR THE BTC FLIP-FLOP IF IT HAS BEEN SET FOR MORE THAN 30 MILLISECONDS, (SEE SHEET B8GE).

DME - THE DATA MATCH ENABLE BIT OPERATION IS SIMILAR TO THE AME BIT. WHEN THE DME BIT IS SET, IT ALLOWS A DATA MATCH FUNCTION TO BE PERFORMED ON THE CONTENTS OF THE MAIN STORE DATA BUS. IF A MATCH OCCURS AN INTERRUPT IS GENERATED (IS BIT 3) IF THE DME BIT IS SET, (SEE SHEET B7GF).

HLT - THE HALT BIT IS USED TO INDICATE THAT THE 3A CC IS IN THE HALT MODE. THE HALT MODE IS DEFINED AS A STATE WHERE THE 3A CC IS LOOPING ON A UNIQUE SEQUENCE OF MICROINSTRUCTIONS CALLED THE HALT LOOP. IN THE HALT LOOP, THE ONLY FUNCTION THE MICROCODE PERFORMS IS TO CHECK FOR THE PRESENCE OF INTERRUPTS. IF AN INTERRUPT IS PRESENT THE MICROCONTROL WILL SERVICE IT. THE HALT LOOP IS TYPICALLY THE MODE IN WHICH THE OFF-LINE 3A CC IS NORMALLY RUN.

ISC 1
AND
ISC 2-THE ISC BITS ARE USED TO RECORD THE LEVEL OF INITIALIZATION BY THE MICROCODE AND THE FUNCTION THAT IS TO BE PERFORMED BY THE MICROCODE WHEN AT THIS LEVEL OF INITIALIZATION. IF ISC 1 = 0 AND ISC 2 = 0 THE MICROCODE WILL TRANSFER CONTROL TO LOCATION 0(40) IN MAIN MEMORY. AT LOCATION 40 AN INITIALIZATION PROGRAM WILL CONTINUE INITIALIZATION. IF ISC 1 = 1 AND ISC 2 = 0, THEN THE 3A CC THAT IS INITIALIZING WILL STOP AND SWITCH TO THE OFF-LINE 3A CC IN AN ATTEMPT TO HAVE IT INITIALIZE THE SYSTEM. IF ISC 1 = 1 AND ISC 2 = 1, THEN THE MICROCODE WILL RELOAD MEMORY FROM THE TAPE CARTRIDGE.

LOF - THE LOCK OFF-LINE FLIP-FLOP WHEN SET INDICATES THAT THE 3A CC IN WHICH THIS BIT IS SET IS LOCKED OFF-LINE. THE LOF FLIP-FLOP WHEN SET INHIBITS THE I/O IN THE 3A CC IN WHICH IT IS LOCATED, (SEE SHEET B7GH).

LON - THE LOCK ON-LINE FLIP-FLOP WHEN SET INDICATES THE 3A CC IN WHICH IT IS LOCATED IS LOCKED ON-LINE. NOTE THAT IF ONE 3A CC IS LOCKED ON-LINE BY DEFINITION, THE OTHER 3A CC IS LOCKED OFF-LINE. THE LON FLIP-FLOP WHEN SET WILL RESULT IN ANY "STOP AND SWITCH" FUNCTION CAUSING A MRF INSTEAD OF THE "STOP AND SWITCH" (SEE SHEET B7GG).

CIRCUIT OPERATION (CONT)

MAN - THE MANUAL BIT INDICATES THAT THE 3A CC IS IN THE MANUAL MODE. THE MANUAL BIT IS CONTROLLED DIRECTLY AND EXCLUSIVELY BY THE MANUAL KEY ON A 3A CC PANEL. WHEN IN THE MANUAL MODE, 3A CC PANEL FUNCTIONS ARE PERMITTED (SEE SHEET B7GB). THIS BIT ALSO DETERMINES WHETHER THE OFF-LINE CONTROL COMPLEX IS AVAILABLE FOR DUPLEX OPERATION, (WHETHER THE OFF-LINE MAIN STORE CAN BE KEPT IN THE UPDATE MODE). THAT IS, IF THE OFF-LINE 3A CC IS NOT IN THE MANUAL MODE AND THE OFF-LINE IS NOT REMOVED FROM SERVICE BECAUSE OF A FAILURE CONDITION, WRITE COMMANDS WILL BE ISSUED TO BOTH THE ON-LINE AND OFF-LINE STORES.

MINT - THE MICROINTERPRET BIT DEFINES THE 3A CC TO BE IN THE MICROINTERPRET MODE (MINT). WHEN IN THIS MODE INSTRUCTIONS THAT ARE FETCHED FROM MAIN MEMORY ARE GATED FROM THE SIR TO THE MIR TO- AND FROM-FIELDS INSTEAD OF FROM THE SIR TO THE MAR AND IB (FOR DETAILS SEE SHEET B1GH).

CC - THE CC FLIP-FLOP DETERMINES WHICH 3A CC IS ON-LINE AND WHICH 3A CC IS IN STANDBY. IF THE CC FLIP-FLOP IS SET THE 3A CC IN WHICH IT IS FOUND IS ON-LINE AND VICE VERSA.

REJ - THE REJECT BIT IS USED BY THE MICROCODE THAT OPERATES THE 3A CC PANEL TO INDICATE THAT AN INVALID COMBINATION OF FUNCTIONS HAS BEEN REQUESTED.

STOP - THE STOP FLIP-FLOP IS USED TO INHIBIT THE FUNCTIONING OF A 3A CC. IT IS TYPICALLY USED WHEN AN ERROR CONDITION IS ENCOUNTERED IN A 3A CC TO INHIBIT IT FROM PERFORMING ANY FURTHER FUNCTIONS. IN ADDITION THE STOP FLIP-FLOP IS SET TO ALLOW MAINTENANCE ACCESS TO THE OUTPUT OF THE MICROPROGRAM STORE. THAT IS, WHEN THE 3A CC IS STOPPED A SPECIAL ADDRESS IS JAMMED INTO THE MAR REGISTER. THIS ADDRESS CONTAINS ALL ZEROS. WITH ALL ZEROS COMING FROM THE OUTPUT OF THE MICROSTORE THE MAINTENANCE CHANNEL HAS THE ABILITY TO OR ITS CONTENTS ONTO THE OUTPUT OF THE MICROSTORE WITHOUT PERFORMING ANY OTHER INHIBIT FUNCTION ON THE MICROSTORE ITSELF. IN THIS MANNER, THE MCH CAN PERFORM MICROINSTRUCTIONS USING THE MICROCONTROL HARDWARE DIRECTLY.

DISA - THE DISABLE BIT IN THE SS REGISTER IS USED AS READ ONLY ACCESS FOR THE DISABLE FLIP-FLOP. THE DISABLE BIT IN THE SS IS HARD WIRED TO THE OUTPUT OF THE DISABLED FLIP-FLOP DESCRIBED IN FS 7 SHEET B7GH.

PRI - THE PRIVILEGE MODE BIT IS USED FOR CERTAIN APPLICATIONS OF THE 3A CC THAT REQUIRE A PRIVILEGE MODE FOR INSTRUCTION EXECUTION.

DISP - THE DISPLAY BIT IS USED TO CONDITIONALLY GATE THE GB TO THE DISPLAY BUFFER (DB) REGISTER. THE DB REGISTER APPEARS ON THE FRONT OF THE 3A CC CONTROL PANEL. WHEN THE DISPLAY BIT IS SET, THE NEXT PROGRAM ADDRESS, PLUS ONE, OF EVERY BRANCH INSTRUCTION ADDRESS IS DISPLAYED ON THE 3A CC CONTROL PANEL IN THE DB REGISTER (SEE SHEET B7GC). THIS PROVIDES A ONE WORD TRANSFER TRACE OF MAIN MEMORY PROGRAMS WHEN THE DISPLAY BIT IS SET.

BPC - THE BLOCK BUS PARITY CHECK BIT WHEN SET IS USED TO INHIBIT THE GB PARITY CHECK FUNCTION. THIS BIT IS TYPICALLY SET SO AS TO ALLOW REGISTERS WITH BAD PARITY TO BE GATED ONTO THE GB SO AS TO NOT CAUSE A GB PARITY ERROR (SEE SHEET B6GF).

IPLTRK - THE IPL TRACK BIT IS USED BY THE MICROCODE WITHIN THE SEQUENCE WHICH INITIATES PROGRAM RELOADS FROM THE TAPE (IPL). THE STATE OF THIS BIT DETERMINES WHICH OF THE TWO IDENTICAL TRACKS ON THE TAPE CARTRIDGE TO READ. THIS BIT IS ALSO USED TO DETERMINE WHEN TO PERFORM THE MORE DRASTIC INITIALIZATION OF THE MAIN STORE PRIOR TO READING DATA OFF THE TAPE. THE MICROCODE TOGGLES THIS BIT EACH TIME THROUGH THE IPL SEQUENCE AND THE SYSTEM INITIALIZATION SOFTWARE RESETS THIS BIT IF THE PROGRAM RELOAD WAS SUCESSFUL.

CC 0
AND
CC 1
BITS - THE TWO PARITY BITS IN SS REGISTER ARE HARDWIRED TO DEFINE WHETHER A 3A CC IS CC 0 OR CC 1. FOR CC 0, PL EQUALS 1 AND PH EQUALS 0. FOR CC 1, PL EQUALS 0 AND PH EQUALS 1.

PART OF FS 5

3A CENTRAL CONTROL

DWG SIZE
6S

ISSUE
5A

BELL LABORATORIES

SD-1C900-01

B5GG

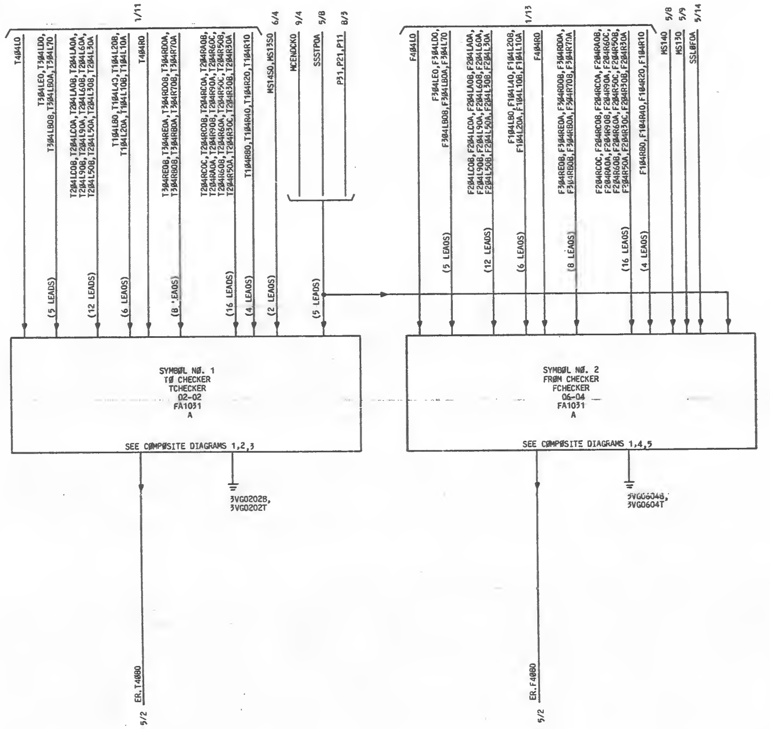
PRINTED IN U.S.A.

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.


1/11
T404L0
T304LE0,T304LD0,
T304LB0B,T304LB0A,T304L70
T204LC0B,T204LC0A,T204LA0B,T204LA0A,
T204L90B,T204L90A,T204L60B,T204L60A,
T204L50B,T204L50A,T204L30B,T204L30A
T104LB0,T104L40,T104L20B,
T104L20A,T104L10B,T104L10A
T404R0
T304RE0B,T304RE0A,T304RD0B,T304RD0A,
T304RB0B,T304RB0A,T304R70B,T304R70A
T204RC0C,T204RC0B,T204RC0A,T204RA0B,
T204RA0A,T204R90B,T204R90A,T204R60C,
T204R60B,T204R60A,T204R50C,T204R50B,
T204R50A,T204R30C,T204R30B,T204R30A
T104RB0,T104R40,T104R20,T104R10
6/4
MS14S0,MS13S0
9/4
MCENDCK0
5/B
SSSTP0A
8/3
P31,P21,P11
(5 LEADS)
(12 LEADS)
(6 LEADS)
(8 LEADS)
(16 LEADS)
(4 LEADS)
(2 LEADS)
(5 LEADS)
SYMBOL NO. 1
TO CHECKER
TCHECKER
02-02
FA1031
A
SEE COMPOSITE DIAGRAMS 1,2,3
3VG0202B,
3VG0202T
ER.T4080
5/2
1/13
F404L0
F304LE0,F304LD0,
F304LB0B,F304LB0A,F304L70
F204LC0B,F204LC0A,F204LA0B,F204LA0A,
F204L90B,F204L90A,F204L60B,F204L60A,
F204L50B,F204L50A,F204L30B,F204L30A
F104LB0,F104L40,F104L20B,
F104L20A,F104L10B,F104L10A
F404R0
F304RE0B,F304RE0A,F304RD0B,F304RD0A,
F304RB0B,F304RB0A,F304R70B,F304R70A
F204RC0C,F204RC0B,F204RC0A,F204RA0B,
F204RA0A,F204R90B,F204R90A,F204R60C,
F204R60B,F204R60A,F204R50C,F204R50B,
F204R50A,F204R30C,F204R30B,F204R30A
F104RB0,F104R40,F104R20,F104R10
5/8
MS140
5/9
MS130
5/14
SSL0F0A
(5 LEADS)
(12 LEADS)
(6 LEADS)
(8 LEADS)
(16 LEADS)
(4 LEADS)
SYMBOL NO. 2
FROM CHECKER
FCHECKER
06-04
FA1031
A
SEE COMPOSITE DIAGRAMS 1,4,5
3VG0604B,
3VG0604T
ER.F4080
5/2

PART OF FS 6
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B6AA

PRINTED IN U.S.A.

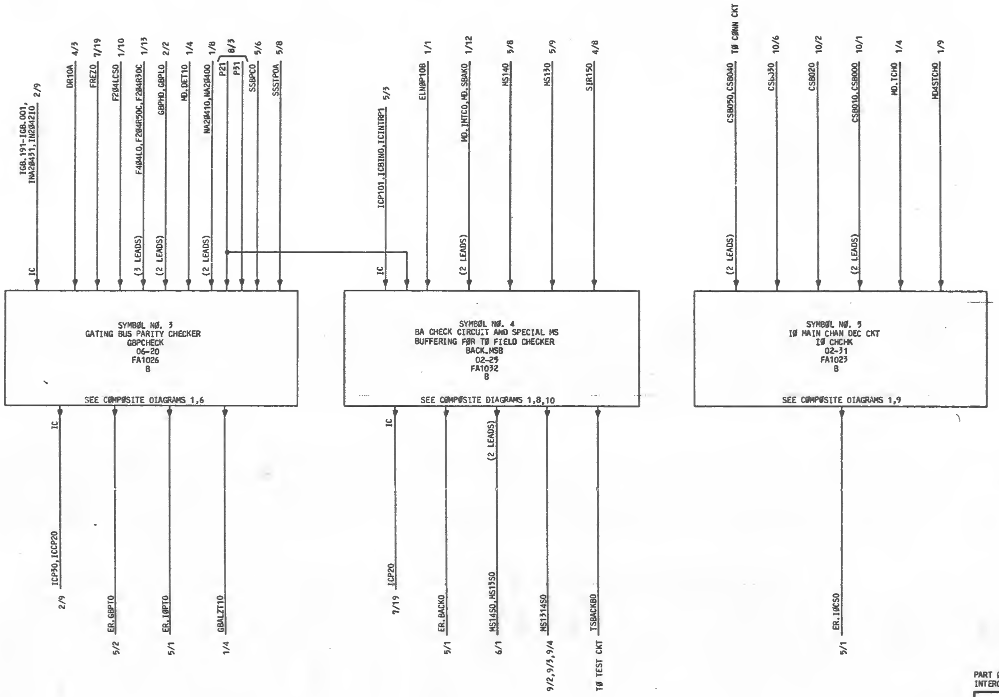
E-7421 (12-73)

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 6
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE 6S	ISSUE 3A

BELL LABORATORIES | SD-1C900-01 | 86AB

E - 7431 (12 - 73)

PRINTED IN U.S.A.

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
CSB000-CSB050	I/O MAIN CHANNEL'S 3 OUT OF 6 RETURN CHECK CODE BITS 0-5
DR10A	DATA READY FLIP-FLOP (COPY 1)
ELNOP10B	ENABLE LOAD NEW OPCODE (COPY 1)
ER.BACK0	BRANCH ALLOWED CHECK ERROR
ER.F4080	FROM FIELD 4 OUT OF 8 ERROR CHECK
ER.F4081	FROM FIELD 4 OUT OF 8 ERROR CHECK (TEST ACCESS ONLY)
ER.GBPT0	GATING BUS PARITY ERROR
ER.IOCS0	I/O MAIN CHANNEL SELECT ERROR
ER.IOPT0	I/O CHANNEL PARITY ERROR
ER.T4080	TO FIELD 4 or 8 DECODER ERROR
ER.T4081	TO FIELD 4 OR 8 DECODER ERROR (TEST PURPOSES ONLY)
FREZ0	MAR FREEZE CONTROL LEAD
GBALZT10	GATING BUS ALL ZEROS TEST (COPY 1)
GBPH0	PARITY HIGH OF THE GATING BUS
GBPL0	PARITY LOW OF THE GATING BUS
ICCP20	P2 CLOCK PHASE [IC]
ICP101	CLOCK PHASE P1 (POSITIVE ACTIVE) [IC]
ICP20	CLOCK PHASE P20 [IC]
ICP30	CLOCK PHASE P30 [IC]
IGB.001-IGB.191	OUTPUTS OF GATING BUS BITS 0-19 [IC]
INA20431	2 OUT OF 4 AUXILIARY DECODER CONTROL BIT 3 [IC]
IN204210	2 OUT OF 4 AUXILIARY DECODER CONTROL BIT 2 [IC]
MCENDCK0	MCA CONTROL ENABLE TO AND FROM FIELD CHECKERS
MD.DET10	MISC. DECODER DETECTOR
MD.IMTC0	MISC. DECODER, IDLE MAINTENANCE CHANNEL
MD.SBAK0	MISC. DECODER, SET THE BA CHECK BIT
MD.TCH0	MISC. DECODER, TEST I/O CHANNEL
MD4STCH0	MISC. DECODER, START THE SELECTED I/O CHANNEL
MS13S0	THE SPECIAL BUFFERED OUTPUT OF BIT 13 OF THE MAINTENANCE STATE CIRCUIT (CODE MERGER TEST 1)
MS130	BIT 13 OF MAINTENANCE STATE REGISTER
MS1314S0	THE "OR" OF SPECIAL BUFFERED OUTPUT OF THE MAINTENANCE STATE REGISTERS BITS 13 AND 14
MS14S0	THE SPECIAL BUFFERED OUTPUT OF BIT 14 OF THE MAINTENANCE STATE REGISTER (CODE MERGERS TEST 2)
MS140	BIT 14 OF THE MAINTENANCE STATE REGISTER
NA20400,NA20410	OUTPUTS OF THE 2 OUT OF 4 AUXILIARY DECODER ATTACHED TO BITS 8 AND 9 OF THE MIR NEXT ADDRESS FIELD
P11	CLOCK PHASE P1 (POSITIVE ACTIVE)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
P21	CLOCK PHASE P2 (POSITIVE ACTIVE)
P31	CLOCK PHASE P3 (POSITIVE ACTIVE)
SIR150	BIT 15 OF THE SIRS (SIR0 IF IFF=0, SIR1 IF IFF=1)
SSBPC0	BLOCK BUS PARITY CHECK BIT (BIT 18 OF THE SS)
SSLOF0A	LOCK OFF-LINE BIT (BIT 8 OF THE SS)
SSSTP0A	STOP FLIP-FLOP BIT (BIT 14 OF THE SS)
TSBACKB0	TEST SET ACCESS, BRANCH ALLOWED CHECK BIT

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

SYMBOL NO. 1

TO CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TCHECKER	02-02	FA1031	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		310			LR61	8A8
		110			LR51	8A7
		005			LR31	8A7
		205			LR41	8A7
ER.T4080	0	103	5/2		408ER0	12H3
ER.T4081		203			ER1	12H6
MCENOCK0	I	303	9/4		EN408ER0	12A2
MS13S0	I	104	6/4		MS0COMI0	12A5
	I	302			LR21	8A6
MS14S0	I	102	6/4		LR11	8A6
	I	304			MS1COMI0	12A6
P11	I	204	8/3		P11	12A3
P21	I	105	8/3		P21	12A3
P31	I	307	8/3		P31	12A2
SSSTPGA	I	003	5/8		IH408ER0	12A2
T104L10A	I	101	1/11		104L1AI0	3A9
T104L10B	I	219	1/11		104L1BI0	3A8
T104L20A	I	202	1/11		104L2AI0	3A8
T104L20B	I	112	1/11		104L2BI0	3A7
T104L40	I	002	1/11		104L4I0	3A7
T104L80	I	301	1/11		104L8I0	3A6
T104R10	I	006	1/11		104R1I0	5A8
T104R20	I	206	1/11		104R2I0	5A7
T104R40	I	106	1/11		104R4I0	5A6
T104R80	I	305	1/11		104R8I0	5A5
T204LA0A	I	007	1/11		204LAAI0	3A1
T204LA0B	I	207	1/11		204LABI0	2A6
T204LC0A	I	008	1/11		204LCAI0	3A0
T204LC0B	I	208	1/11		204LCBI0	2A5
T204L30A	I	308	1/11		204L3AI0	3A2
T204L30B	I	009	1/11		204L3BI0	2A8
T204L50A	I	209	1/11		204L5AI0	3A2
T204L50B	I	109	1/11		204L5BI0	2A7
T204L60A	I	309	1/11		204L6AI0	3A2
T204L60B	I	010	1/11		204L6BI0	2A7
T204L90A	I	210	1/11		204L9AI0	3A1
T204L90B	I	306	1/11		204L9BI0	2A6
T204RA0A	I	313	1/11		204RAAI0	5A1
T204RA0B	I	113	1/11		204RABI0	4A7
T204RC0A	I	213	1/11		204RCAI0	5A0
T204RC0B	I	013	1/11		204RCBI0	4A6
T204RC0C	I	312	1/11		204RCCI0	4A5
T204R30A	I	108	1/11		204R3AI0	5A3
T204R30B	I	216	1/11		204R3BI0	4A9
T204R30C	I	016	1/11		204R3CI0	4A6
T204R50A	I	315	1/11		204R5AI0	5A2
T204R50B	I	115	1/11		204R5BI0	4A8
T204R50C	I	215	1/11		204R5CI0	4A5
T204R60A	I	015	1/11		204R6AI0	5A2
T204R60B	I	314	1/11		204R6BI0	4A8
T204R60C	I	114	1/11		204R6CI0	4A5
T204R90A	I	214	1/11		204R9AI0	5A1
T204R90B	I	014	1/11		204R9BI0	4A7
T304LB0A	I	201	1/11		304LBAI0	2A3
T304LB0B	I	317	1/11		304LBBI0	2A3
T304L00	I	001	1/11		304L0I0	2A2
T304LE0	I	300	1/11		304LEI0	2A1
T304L70	I	100	1/11		304L7I0	2A4
T304RB0A	I	017	1/11		304RBAI0	4A3
T304RB0B	I	318	1/11		304RBBI0	4A3

SYMBOL NO. 1 (CONT)

TO CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TCHECKER	02-02	FA1031	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T304RD0A	I	217	1/11		304RDAI0	4A2
T304RD0B	I	118	1/11		304RDBI0	4A2
T304RE0A	I	116	1/11		304REAI0	4A1
T304RE0B	I	218	1/11		304REBI0	4A1
T304R70A	I	316	1/11		304R7AI0	4A4
T304R70B	I	019	1/11		304R7BI0	4A4
T404L0	I	117	1/11		404LI0	2A0
T404R0	I	018	1/11		404RI0	4A0
3T054B	GRD	2GD		203	GRD	
	GRD	0GD		203	GRD	
	GRD	319		203	GRD	
	GRD	200		203	GRD	
3VG0202B	GRD	200			GRD	
	GRD	107			GRD107	2G5
3VG0202T	GRD	311			GRD311	2G6
	GRD	012			GRD012	2G6
	GRD	212			GRD212	2G6
	GRD	011			GRD011	2G7
	GRD	211			GRD211	2G7
	GRD	319			GRD	
	GRD	111			GRD111	2G7
3V054B	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 2

FROM CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FCHECKER	06-04	FA1031	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		110			LR51	8A7
		302			LR21	8A6
		005			LR31	8A7
		205			LR41	8A7
		102			LR11	8A6
ER.F4080	0	103	5/2		408ER0	12H3
ER.F4081		203			ER1	12H6
F104L10A	I	101	1/13		104L1AI0	3A9
F104L10B	I	219	1/13		104L1BI0	3A8
F104L20A	I	202	1/13		104L2AI0	3A8
F104L20B	I	112	1/13		104L2BI0	3A7
F104L40	I	002	1/13		104L4I0	3A7
F104L80	I	301	1/13		104L8I0	3A6
F104R10	I	006	1/13		104R1I0	5A8
F104R20	I	206	1/13		104R2I0	5A7
F104R40	I	106	1/13		104R4I0	5A6
F104R80	I	305	1/13		104R8I0	5A5
F204LA0A	I	007	1/13		204LAAI0	3A1
F204LA0B	I	207	1/13		204LABI0	2A6
F204LC0A	I	008	1/13		204LCAI0	3A0
F204LC0B	I	208	1/13		204LCBI0	2A5

SYMBOL NO. 2 (CONT)

FROM CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FCHECKER	06-04	FA1031	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
F204L30A	I	308	1/13		204L3AI0	3A2
F204L30B	I	009	1/13		204L3BI0	2A8
F204L50A	I	209	1/13		204L5AI0	3A2
F204L50B	I	109	1/13		204L5BI0	2A7
F204L60A	I	309	1/13		204L6AI0	3A2
F204L60B	I	010	1/13		204L6BI0	2A7
F204L90A	I	210	1/13		204L9AI0	3A1
F204L90B	I	306	1/13		204L9BI0	2A6
F204RA0A	I	313	1/13		204RAAI0	5A1
F204RA0B	I	113	1/13		204RABI0	4A7
F204RC0A	I	213	1/13		204RCAI0	5A0
F204RC0B	I	013	1/13		204RCBI0	4A6
F204RC0C	I	312	1/13		204RCCI0	4A5
F204R30A	I	108	1/13		204R3AI0	5A3
F204R30B	I	216	1/13		204R3BI0	4A9
F204R30C	I	016	1/13		204R3CI0	4A6
F204R50A	I	315	1/13		204R5AI0	5A2
F204R50B	I	115	1/13		204R5BI0	4A8
F204R50C	I	215	1/13		204R5CI0	4A5
F204R60A	I	015	1/13		204R6AI0	5A2
F204R60B	I	314	1/13		204R6BI0	4A8
F204R60C	I	114	1/13		204R6CI0	4A5
F204R90A	I	214	1/13		204R9AI0	5A1
F204R90B	I	014	1/13		204R9BI0	4A7
F304LB0A	I	201	1/13		304LBAI0	2A3
F304LB0B	I	317	1/13		304LBBI0	2A3
F304L00	I	001	1/13		304L0I0	2A2
F304LE0	I	300	1/13		304LEI0	2A1
F304L70	I	100	1/13		304L7I0	2A4
F304RB0A	I	017	1/13		304RBAI0	4A3
F304RB0B	I	318	1/13		304RBBI0	4A3
F304RD0A	I	217	1/13		304RDAI0	4A2
F304RD0B	I	118	1/13		304RDBI0	4A2
F304RE0A	I	116	1/13		304REAI0	4A1
F304RE0B	I	218	1/13		304REBI0	4A1
F304R70A	I	316	1/13		304R7AI0	4A4
F304R70B	I	019	1/13		304R7BI0	4A4
F404L0	I	117	1/13		404LI0	2A0
F404R0	I	018	1/13		404RI0	4A0
MCENOCK0	I	303	9/4		EN408ER0	12A2
MS130	I	104	5/9		MS0COMI0	12A5
MS140	I	304	5/8		MS1COMI0	12A6
P11	I	204	8/3		P11	12A3
P21	I	105	8/3		P21	12A3
P31	I	307	8/3		P31	12A2
SSLOF0A	I	310	5/14		LR61	8A8
SSSTP0A	I	003	5/8		IH408ER0	12A2
3T058B	GRD	200		203	GRD	
	GRD	319		203	GRD	
	GRD	2GD		203	GRD	
	GRD	0GD		203	GRD	
3VG0604B	GRD	200			GRD	
	GRD	107			GRD107	2G5
3VG0604T	GRD	311			GRD311	2G6
	GRD	212			GRD212	2G6
	GRD	011			GRD011	2G7
	GRD	319			GRD	
	GRD	012			GRD012	2G6
	GRD	211			GRD211	2G7
	GRD	111			GRD111	2G7

SYMBOL NO. 2 (CONT)

FROM CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
FCHECKER	06-04	FA1031	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V058B	PWR	000		203	+3	
3V058B	PWR	119		203	+3	

PART OF FS 6
SYMBOL(S) 1 2

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	B6CA
DWG SIZE C2	ISSUE 4A	12/13/76

PRINTED IN U. S. A.

PART OF FS 6
DATA TRANSFER CHECK CIRCUITS

SYMBOL NO. 3
GATING BUS PARITY CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GBPCHECK	06-20	FA1026	8	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		009			ENBPC0	7A0
DR10A	I	111	4/3		DRI0	7A3
ER.GBPT0	0	106	5/2		GB.POK1	7H7
ER.IOPT0	0	306	5/1		IO.POK1	7H7
FRE20	I	208	7/19		FRE2I0	7A1
F204LCS0	I	207	1/10		F204LC0	7A3
F204R30C	I	107	1/13		F204R30	7A2
F204R50C	I	007	1/13		F204R50	7A4
F404L0	I	008	1/13		F404L0	7A1
GBAL2T10	0	314	1/4		ALL20	8G6
GBPH0	I	308	2/2		GB.PH0	5A1
GBPL0	I	108	2/2		GB.PL0	5A1
ICCP20	0	IC	2/9		P20	7C8
ICP30	0	IC	2/9		P3001	8G8
IGB.001	I	IC	2/9		GB.001	6A7
IGB.011	I	IC	2/9		GB.011	6A6
IGB.021	I	IC	2/9		GB.021	6A5
IGB.031	I	IC	2/9		GB.031	6A5
IGB.041	I	IC	2/9		GB.041	6A4
IGB.051	I	IC	2/9		GB.051	6A3
IGB.061	I	IC	2/9		GB.061	6A2
IGB.071	I	IC	2/9		GB.071	6A2
IGB.081	I	IC	2/9		GB.081	6A1
IGB.091	I	IC	2/9		GB.091	6A1
IGB.101	I	IC	2/9		GB.101	5B8
IGB.111	I	IC	2/9		GB.111	5B8
IGB.121	I	IC	2/9		GB.121	5B7
IGB.131	I	IC	2/9		GB.131	5B6
IGB.141	I	IC	2/9		GB.141	5B5
IGB.151	I	IC	2/9		GB.151	5B5
IGB.161	I	IC	2/9		GB.161	5B4
IGB.171	I	IC	2/9		GB.171	5B3
IGB.181	I	IC	2/9		GB.181	5B2
IGB.191	I	IC	2/9		GB.191	5B2
INA20431	I	IC	2/9		NA20431	7E0
IN204210	I	IC	2/9		NA204210	7C7
MD.DET10	I	307	1/4		MDXPI0	7A2
NA20400	I	110	1/8		NA20400	7A7
NA20410	I	310	1/8		NA20410	7A4
P21	I	209	8/3		P21	7A6
P31	I	010	8/3		P31	8A7
SSBPC0	I	109	5/6		SSBPC0	7A1
SSSTP0A	I	309	5/8		STOPI0	7A1

SYMBOL NO. 4
BA CHECK CIRCUIT AND SPECIAL MS
BUFFERING FOR TO FIELD CHECKER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BACK.MSB	02-25	FA1032	8	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ELNOP10B	I	109	1/1		LNOPI0	4A3
ER.BACK0	0	013	5/1		BA.ER0	4H3
ICP101	I	IC	5/3		P101	4E0
ICP20	0	IC	7/19		P20	4H1
~~MD.IMTC0~~	~~I~~	~~001~~	~~1/12~~		CL.MST00	4A5
MD.SBAK0	I	309	1/12		STBACKI0	4A2
MS13S0	0	003	6/1		MST0A0	4H6
MS130	I	300	5/9		SMST0AI0	4A6
MS1314S0	0	103	9/2,9/3 9/4		MST0AB0	4H6
MS14S0	0	201	6/1		MST0B0	4H6
MS140	I	100	5/8		SMST0BI0	4A6
P21	I	204	8/3		P21	4A1
SIR150	I	116	4/8	202	SIR815I0	4A3
TSBACK80	0	205			BA.CK0	4H2

SYMBOL NO. 5
IO MAIN CHAN DEC CKT

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IO CHCHK	02-31	FA1023	8	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
CS8000	I	308	10/1	202	CSB00	5A2
CS8010	I	209	10/1	202	CSB10	5A1
CS8020	I	009	10/2	202	CSB20	5A1
CS8030	I	210	10/6	202	CSB30	5A[illegible]
CS8040	I	109	TO CONN CKT	202	CSB40	5A[illegible]
CS8050	I	309	TO CONN CKT	202	CSB50	5A2
ER.IOCS0	0	318	5/1		IOMCSER0	5H4
MO.TCH0	I	218	1/4		IO.TST0	5A0
MD4STCH0	I	018	1/9		IO.G00	5A1

PART OF FS 6
SYMBOL(S) 3 4 5

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	4A

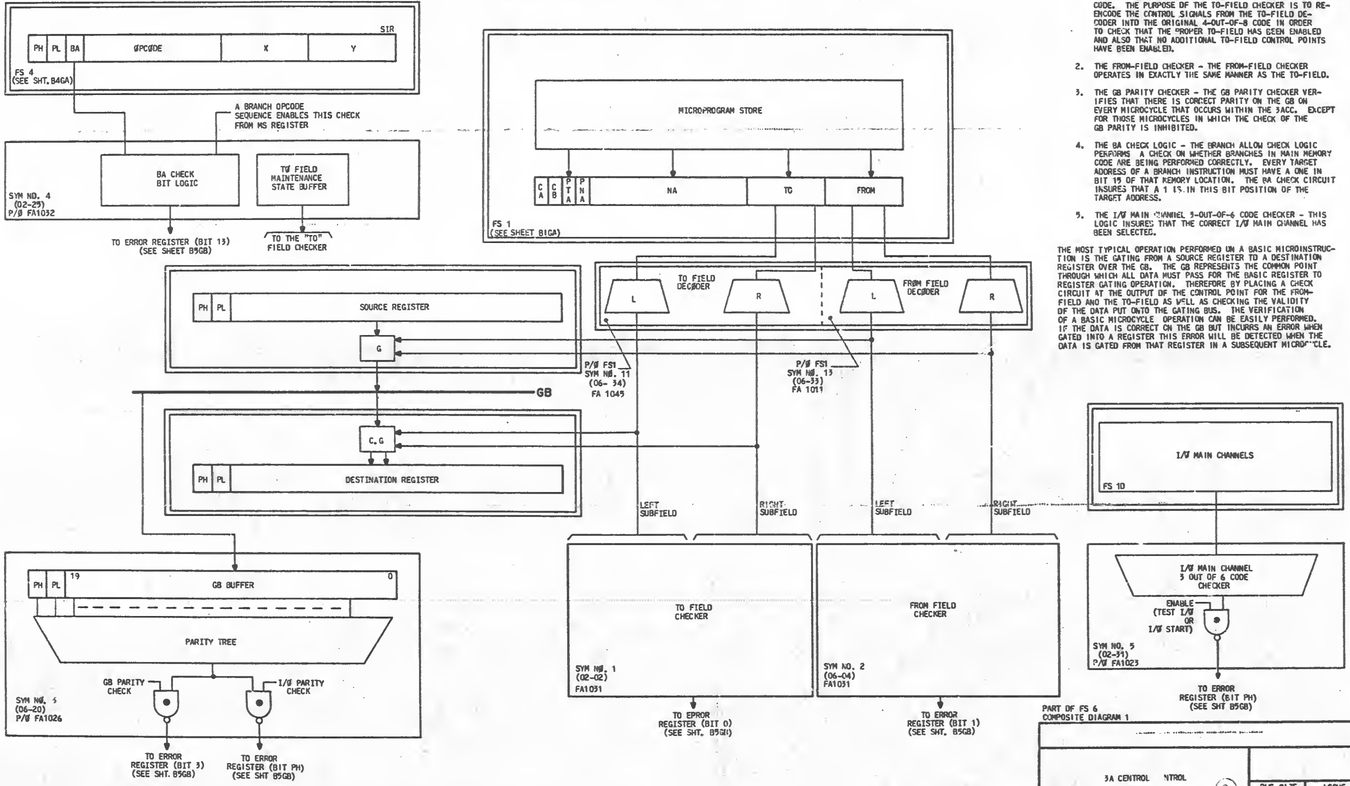
BELL LABORATORIES
SD-1C900-01
86CB
PRINTED IN U. S. A.
12/13/76

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM I

FUNCTION PARTITIONING OF DATA TRANSFER CHECK CIRCUITS



CIRCUIT OPERATION

FS 6 CONTAINS MOST OF THE CHECK CIRCUITS FOR THE DATA TRANSFER OPERATIONS IN THE 3ACC. THESE CHECK CIRCUITS ARE:

1. THE TO-FIELD CHECKER - THE TO-FIELD CHECKER PERFORMS A CHECK FUNCTION ON THE TO-FIELD DECODING MATRIX. THE TO-FIELD DECODER IS ACTIVATED FROM A 4-OUT-OF-8 CODE. THE PURPOSE OF THE TO-FIELD CHECKER IS TO RE-ENCODE THE CONTROL SIGNALS FROM THE TO-FIELD DECODER INTO THE ORIGINAL 4-OUT-OF-8 CODE IN ORDER TO CHECK THAT THE PROPER TO-FIELD HAS BEEN ENABLED AND ALSO THAT NO ADDITIONAL TO-FIELD CONTROL POINTS HAVE BEEN ENABLED.

2. THE FROM-FIELD CHECKER - THE FROM-FIELD CHECKER OPERATES IN EXACTLY THE SAME MANNER AS THE TO-FIELD.

3. THE GB PARITY CHECKER - THE GB PARITY CHECKER VERIFIES THAT THERE IS CORRECT PARITY ON THE GB ON EVERY MICROCYCLE THAT OCCURS WITHIN THE 3ACC. EXCEPT FOR THOSE MICROCYCLES IN WHICH THE CHECK OF THE GB PARITY IS INHIBITED.

4. THE BA CHECK LOGIC - THE BRANCH ALLOW CHECK LOGIC PERFORMS A CHECK ON WHETHER BRANCHES IN MAIN MEMORY CODE ARE BEING PERFORMED CORRECTLY. EVERY TARGET ADDRESS OF A BRANCH INSTRUCTION MUST HAVE A ONE IN BIT 15 OF THAT MEMORY LOCATION. THE BA CHECK CIRCUIT INSURES THAT A 1 IS IN THIS BIT POSITION OF THE TARGET ADDRESS.

5. THE I/O MAIN CHANNEL 3-OUT-OF-6 CODE CHECKER - THIS LOGIC INSURES THAT THE CORRECT I/O MAIN CHANNEL HAS BEEN SELECTED.

THE MOST TYPICAL OPERATION PERFORMED ON A BASIC MICROINSTRUCTION IS THE GATING FROM A SOURCE REGISTER TO A DESTINATION REGISTER OVER THE GB. THE GB REPRESENTS THE COMMON POINT THROUGH WHICH ALL DATA MUST PASS FOR THE BASIC REGISTER TO REGISTER GATING OPERATION. THEREFORE BY PLACING A CHECK CIRCUIT AT THE OUTPUT OF THE CONTROL POINT FOR THE FROM-FIELD AND THE TO-FIELD AS WELL AS CHECKING THE VALIDITY OF THE DATA PUT ONTO THE GATING BUS. THE VERIFICATION OF A BASIC MICROCYCLE OPERATION CAN BE EASILY PERFORMED. IF THE DATA IS CORRECT ON THE GB BUT INCURRS AN ERROR WHEN GATED INTO A REGISTER THIS ERROR WILL BE DETECTED WHEN THE DATA IS GATED FROM THAT REGISTER IN A SUBSEQUENT MICROCYCLE.

PART OF FS 6
COMPOSITE DIAGRAM 1

3A CENTROL NTROL ②

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B6GA

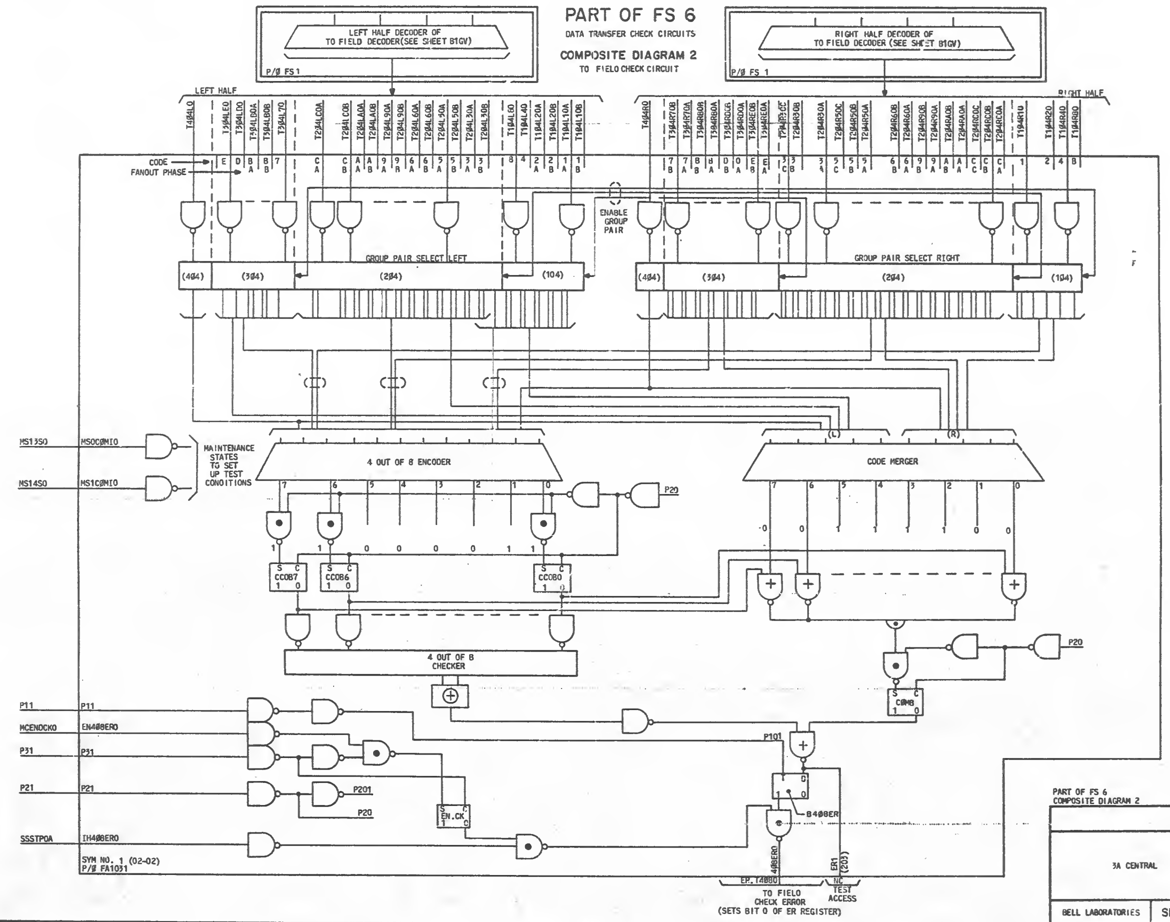
CIRCUIT OPERATION
(SEE SHT. B6GC)

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 2

TO FIELO CHECK CIRCUIT



PART OF FS 6
COMPOSITE DIAGRAM 2

3A CENTRAL TROL ②

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES | SD-IC900-01 | B6GB

E - 7421 (12 - 73)

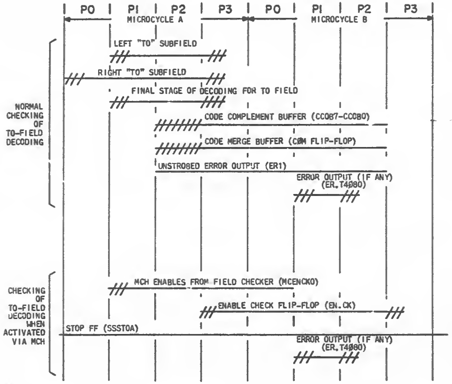
PRINTED IN U.S.A.

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 3

TIMING DIAGRAM OF TO-FIELD DECODER CHECKER


P0
P1
P2
P3
P0
P1
P2
P3
MICROCYCLE A
MICROCYCLE B
NORMAL CHECKING OF TO-FIELD DECODING
LEFT "TO" SUBFIELD
RIGHT "TO" SUBFIELD
FINAL STAGE OF DECODING FOR TO FIELD
CODE COMPLEMENT BUFFER (CC087-CC080)
CODE MERGE BUFFER (C0M FLIP-FLOP)
UNSTROBED ERROR OUTPUT (ER1)
ERROR OUTPUT (IF ANY) (ER.T4080)
CHECKING OF TO-FIELD DECODING WHEN ACTIVATED VIA MCH
MCH ENABLES FROM FIELD CHECKER (MCENCK0)
ENABLE CHECK FLIP-FLOP (EN.CK)
STOP FF (SSST0A)
ERROR OUTPUT (IF ANY) (ER.T4080)

CIRCUIT OPERATION FOR COMPOSITE DIAGRAM 2 AND 3

THE PURPOSE OF THE TO-FIELD CHECK CIRCUIT IS TO INSURE THAT A CORRECT TO-FIELD CONTROL POINT IS EXECUTED ON EVERY MICROCYCLE PERFORMED BY THE 3A CC. IN PERFORMING THIS CHECK, THE TO-FIELD CHECKER NOT ONLY INSURES THAT THE CORRECT TO-FIELD DECODER HAS BEEN ENABLED, BUT ALSO IT VERIFIES THE PROPER OPERATION OF THE ACCESSING LOGIC ASSOCIATED WITH THE MICROSTORE ITSELF. THIS INCLUDES THE MICROSTORE ADDRESS DECODING, THE ACCESS OF THE MICROSTORE WORD AND THE SUBSEQUENT GATING OF THE OUTPUT OF THE MICROSTORE TO-FIELD INTO THE MIR AND THE INPUTTING OF 4-OUT-OF-8 CODE TO THE TO-FIELD DECODER. THE REASON FOR THIS IS THAT IF A FAULT HAS OCCURRED IN THE MICROSTORE ACCESSING CIRCUITS, IT WILL TEND TO EITHER ACCESS MULTIPLE WORDS IN THE MICROSTORE OR NO WORDS AT ALL. THIS IN TURN WILL CAUSE A NON-4-OUT-OF-8 CODE TO BE LOADED IN THE MIR TO-FIELD REGISTER. HENCE, RESULTS IN A 4-OUT-OF-8 CODE FAILURE. FOR ADDITIONAL DETAILS, SEE SHEET B1GV.

AS EXPLAINED ON SHEET B1GV, THE TO FIELD IS PARTITIONED INTO A LEFT HALF AND A RIGHT HALF. THE PURPOSE OF THIS IS TO MINIMIZE THE NUMBER OF CONTROL LEADS IN THE BACKPLANE. FOR EXAMPLE, IT WOULD TAKE 70 CONTROL LEADS TO DEFINE ALL OF THE POSSIBLE STATES OF A 4-OUT-OF-8 CODE. THE PARTITIONING TECHNIQUE REQUIRES ONLY 34 CONTROL LEADS. IT SHOULD BE NOTED THAT TO PROVIDE THE NECESSARY FANOUT THERE ARE ACTUALLY MORE THAN 34 CONTROL SIGNALS (i.e. DUPLICATE FANOUT PHASES). THE RESULT OF THE DECODER PARTITIONING IS THAT TO PERFORM THE TO-FIELD DECODING IT TAKES TWO CONTROL LEADS FROM THE BACKPLANE TO BE "ADDED" TOGETHER TO PERFORM THE FINAL STAGE OF DECODING. THEREFORE, THE OPERATION OF THE TO-FIELD CHECKER MUST BE TO TAKE EACH CONTROL FIELD IN THE LEFT HALF AND PAIR IT UP WITH THE CORRESPONDING CONTROL FIELD IN THE RIGHT HALF. HENCE, THE FINAL STAGE OF DECODING OF THE TO-FIELD CROSSPOINT IS PERFORMED BEFORE IT CAN BE USED TO REENCODE THE 4-OUT-OF-8 CODE THAT PRODUCED IT.

AS SHOWN IN COMPOSITE DIAGRAM 2, THIS IS THE FIRST FUNCTIONAL OPERATION THAT IS PERFORMED ON THE TO-FIELD CONTROL SIGNALS AS THEY ENTER FROM THE BACKPLANE. IT SHOULD BE NOTED, AS WAS EXPLAINED ON SHEET B1GF, THE MNEMONIC DESCRIPTION OF THE TO-FIELD CONTROL SIGNAL INDICATES THE 4-OUT-OF-8 CODE THAT PRODUCES THEM. THIS CODE, FOR EACH OF THE SUBFIELDS, LEFT AND RIGHT, IS INDICATED AT THE TOP OF COMPOSITE DIAGRAM 2. IT SHOULD ALSO BE NOTED THAT SOME OF THESE CONTROL FIELDS HAVE MORE THAN ONE FANOUT PHASE, WITH THE FANOUT PHASE BEING INDICATED IF THERE ARE MORE THAN ONE BY THE LETTERS A,B, OR C.

THE TO-FIELD CHECK CIRCUIT MUST NOT ONLY CHECK FOR THE PROPER OPERATION OF EACH OF TO-FIELD CONTROL SIGNALS BUT ALSO IT MUST ENSURE THAT ALL OF THEIR FANOUT PHASES ARE CORRECT. THE CHECK OF THE FANOUT PHASES IS PERFORMED BY THE PORTION OF THE CHECK CIRCUIT KNOWN AS CODE MERGER. FIRST THE OPERATION OF THE 4-OUT-OF-8 ENCODER WILL BE OUTLINED.

THE 4-OUT-OF-8 ENCODER RECEIVES THE CONTROL SIGNALS THAT REPRESENT THE FINAL STAGE OF DECODING OF THE TO FIELD, AND REENCODES IT INTO THE COMPLEMENT OF THE 4-OUT-OF-8 CODE THAT PRODUCE THIS CONTROL SIGNAL. THIS 4-OUT-OF-8 CODE IS THEN GATED BY CLOCK PHASE P2 INTO A BUFFER REGISTER INDICATED AS CC087-CC080. THE OUTPUT OF THIS REGISTER IS THEN SENT TO A 4-OUT-OF-8 CHECKER TO INSURE THAT A CORRECT 4-OUT-OF-8 CODE HAS BEEN REENCODED. THIS 4-OUT-OF-8 CHECKER IS A SELF-CHECKING CHECKER; THAT IS, IT WILL DETECT FAULTS THAT OCCUR NOT ONLY IN ITS INPUTS, BUT ALSO WITHIN THE 4-OUT-OF-8 CHECKER ITSELF. THE OUTPUT OF THIS 4-OUT-OF-8 CHECKER RESULTS IN A 1-OUT-OF-2 CODE WHICH IS IN TURN

CIRCUIT OPERATION (CONT)

INPUTTED TO AN "EXCLUSIVE OR" CIRCUIT THAT REPRESENTS THE FINAL OUTPUT OF THE 4-OUT-OF-8 CHECKER. THIS OUTPUT IS THEN "OR"ED WITH THE OUTPUT OF THE CODE MERGER CIRCUIT AND THEN STROBED INTO A BUFFER FLIP-FLOP, B408ER, THAT WILL INDICATE WHETHER THE PROPER OPERATION OF THE TO FIELD HAS OCCURRED.

THE OPERATION OF THE CODE MERGER CAN BE THOUGHT OF AS GENERATING A 4-OUT-OF-8 CODE AS WELL. SINCE THE 4-OUT-OF-8 ENCODER GENERATES THE COMPLEMENT OF THE ORIGINAL 4-OUT-OF-8 CODE AND THE CODE MERGER GENERATES THE 4-OUT-OF-8 CODE ITSELF, IF THE TWO ARE "OR"ED TOGETHER ON A BIT BY BIT BASIS THE RESULT SHOULD BE ALL ONES. IF THE CORRECT 4-OUT-OF-8 CODE HAS BEEN GENERATED FROM THE 4-OUT-OF-8 ENCODER AND THE CODE MERGER INDICATES AN ERROR, THEN THIS MEANS THAT ONE OF THE FANOUT PHASES OF THE TO-FIELD CONTROL SIGNALS HAS FAILED. THE RESULT OF THIS CHECK IS GATED INTO A BUFFER FLIP-FLOP, CALLED THE COMB FLIP-FLOP, VIA CLOCK PHASE P2. THE OUTPUT OF THIS CHECK TOGETHER WITH THE 4-OUT-OF-8 CHECK IS "OR"ED TOGETHER AND IS STROBED INTO A TO-FIELD CHECK CIRCUIT FLIP-FLOP CALLED THE B408ER. AS CAN BE SEEN BY THE TIMING DIAGRAM IN COMPOSITE DIAGRAM 3, THIS FLIP-FLOP IS STROBED AT THE START OF CLOCK PHASE P1 AND CLEARED AT THE START OF CLOCK PHASE P2. THE OUTPUT OF THIS CHECK CIRCUIT INPUTS DIRECTLY INTO THE ERROR REGISTER BIT D; THEREFORE, IF A TO-FIELD CHECK CIRCUIT FIRES, A DC CONDITION IS SET IN THE ERROR REGISTER BIT 0.

AS WAS INDICATED EARLIER, THE TO-FIELD CHECK CIRCUIT INSURES THAT A VALID TO-FIELD CONTROL POINT IS OPERATED ON EVERY MICROCYCLE PERFORMED IN A 3A CC. THERE ARE CERTAIN STATES OR CONDITIONS WHERE A VALID TO FIELD MAY NOT BE PERFORMED AND HENCE, THE CHECK CIRCUIT MUST BE INHIBITED. THIS INHIBIT IS PERFORMED BY THE OUTPUT OF THE STOP FLIP-FLOP. THE STOP FLIP-FLOP IS USED TO INHIBIT THE SEQUENCING OF THE MICROCONTROL. IN THIS STATE, ALL ZEROS ARE NORMALLY READ OUT OF THE MICROSTORE AND HENCE, THE VALID TO-FIELD CHECK WOULD NOT BE OBTAINED. TO ALLOW THE MAINTENANCE CHANNEL TO CHECK THE PROPER EXECUTION OF THE MICROINSTRUCTIONS, ORIGINATING FROM THE OTHER 3A CC, A SPECIAL TO-FIELD CHECK CIRCUIT ENABLE LEAD IS PROVIDED. THIS LEAD IS ENABLED BY THE MAINTENANCE CHANNEL WHEN IT LOADS THE TO FIELD IN THE MIR REGISTER. THE LOADING OF THE TO FIELD RESULTS IN THE EXECUTION OF A TO-FIELD CONTROL POINT AND BY TURNING ON THE ENABLE CHECK LEAD, ITS CORRECT OPERATION IS VERIFIED.

THERE ARE TWO MAINTENANCE STATES SHOWN IN COMPOSITE DIAGRAM 2(D1) THAT ARE USED TO SET UP MAINTENANCE TEST CONDITIONS TO ALLOW DIAGNOSTIC TEST ACCESS TO THE TO-FIELD CHECK LOGIC.

PART OF FS 6
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL
DWG SIZE 6S
ISSUE 5A.
BELL LABORATORIES
SD-1C900-01
B6GC

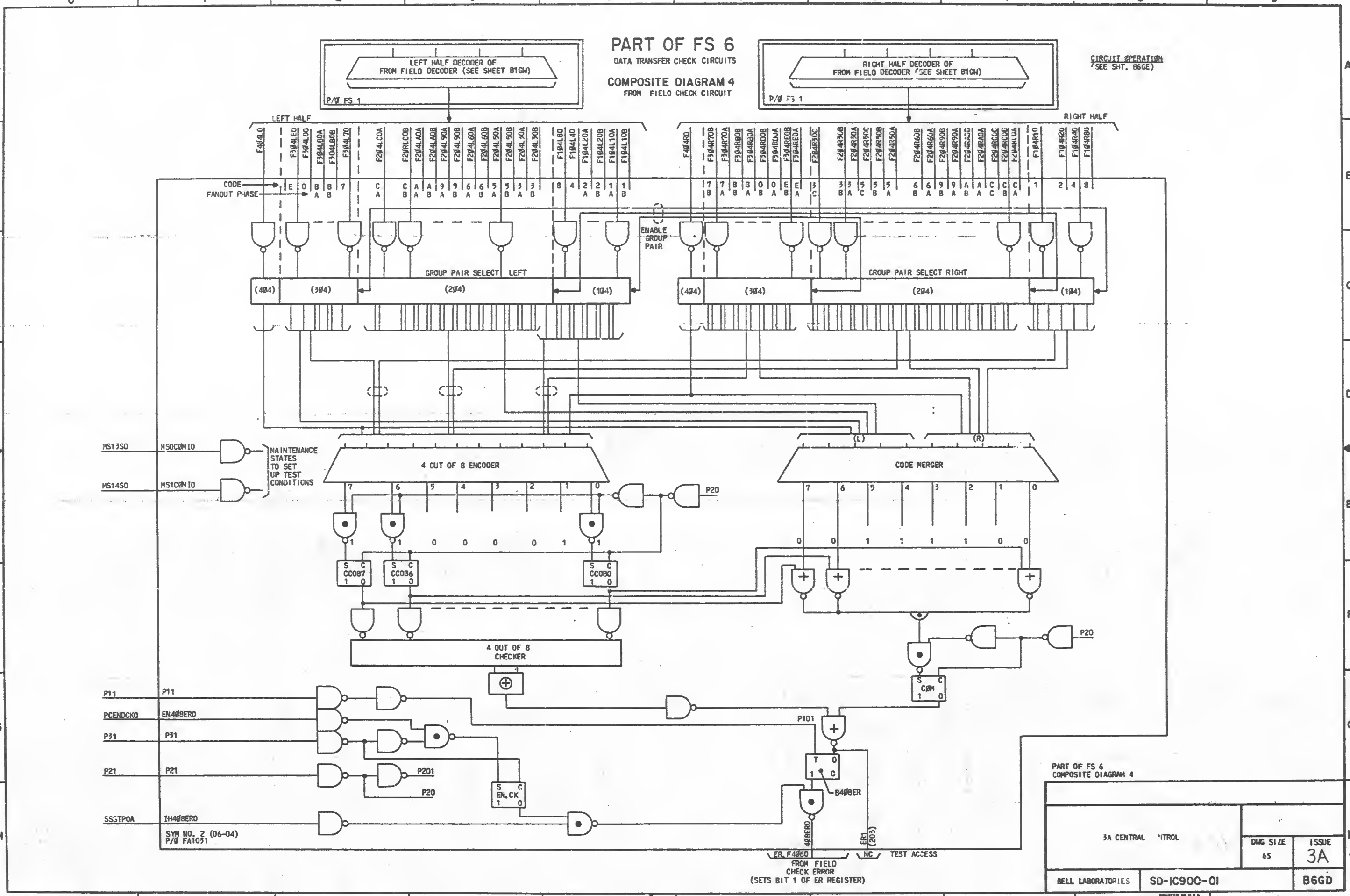
PRINTED IN U.S.A.

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 4

FROM FIELD CHECK CIRCUIT



PART OF FS 6
COMPOSITE DIAGRAM 4

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	3A

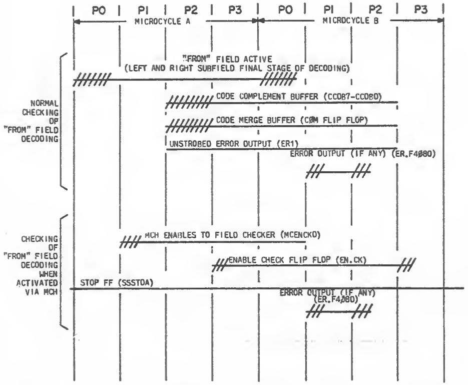
BELL LABORATORIES SD-1C900-01 B6GD

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 5

TIMING DIAGRAM OF "FROM" FIELD DECODER CHECKER



P0
P1
P2
P3
P0
P1
P2
P3
MICROCYCLE A
MICROCYCLE B
NORMAL CHECKING OF "FROM" FIELD DECODING
"FROM" FIELD ACTIVE (LEFT AND RIGHT SUBFIELD FINAL STAGE OF DECODING)
CODE COMPLEMENT BUFFER (CCOB7-CCOB0)
CODE MERGE BUFFER (C0M FLIP FLOP)
UNSTROBED ERROR OUTPUT (ER1)
ERROR OUTPUT (IF ANY) (ER.F4080)
CHECKING OF "FROM" FIELD DECODING WHEN ACTIVATED VIA MCH
MCH ENABLES TO FIELD CHECKER (MCENCK0)
ENABLE CHECK FLIP FLOP (EN.CK)
STOP FF (SSSTOA)
ERROR OUTPUT (IF ANY) (ER.F4080)

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 4 AND 5

THE OPERATION OF THE FROM FIELD CHECKER IS EXACTLY THE SAME AS THE TO-FIELD CHECKER. THE ONLY MINOR DIFFERENCE BETWEEN THE TWO IS THAT THE FROM-FIELD CONTROL SIGNALS, BOTH THE LEFT SUBFIELD AND THE RIGHT SUBFIELD, HAVE A SLIGHTLY DIFFERENT TIMING, AS INDICATED IN COMPOSITE DIAGRAM 5. THE TIMING OF THE FROM-FIELD CHECKER ITSELF REMAINS IDENTICAL TO THE TO-FIELD.

PART OF FS 6
COMPOSITE DIAGRAM 5

3A CENTRAL CONTROL ②
DWG SIZE 6S
ISSUE 3A
BELL LABORATORIES
SD-1C900-01
B6GE

PRINTED IN U.S.A.

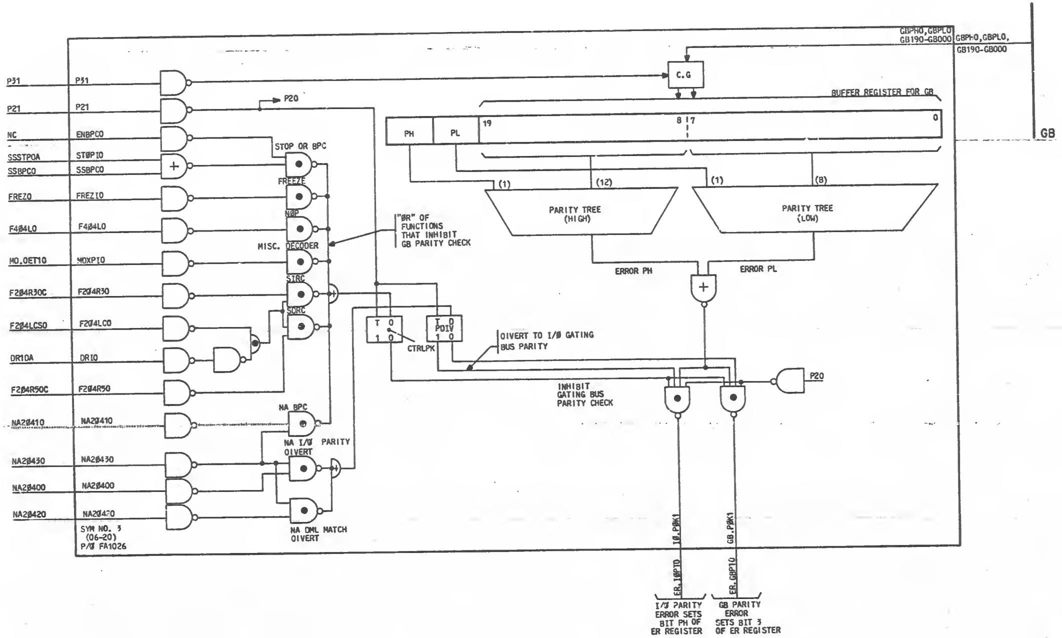
PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 6

GATING BUS PARITY CHECKER

CIRCUIT OPERATION
(SEE SHT. B6GG)



PART OF FS 6
COMPOSITE DIAGRAM 6

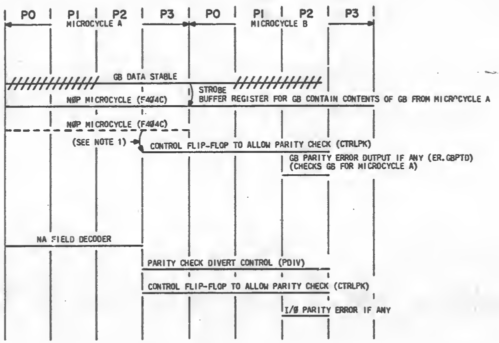
5A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	B6GF

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 7

DIAGRAM FOR GATING BUS PARITY CHECK OPERATION


P0
P1
P2
P3
P0
P1
P2
P3
MICROCYCLE A
MICROCYCLE B
GB DATA STABLE
STROBE
BUFFER REGISTER FOR GB CONTAIN CONTENTS OF GB FROM MICROCYCLE A
NOP MICROCYCLE (F404C)
NOP MICROCYCLE (F404C)
(SEE NOTE 1)
CONTROL FLIP-FLOP TO ALLOW PARITY CHECK (CTRLPK)
GB PARITY ERROR OUTPUT IF ANY (ER.GBPTD)
(CHECKS GB FOR MICROCYCLE A)
NA FIELD DECODER
PARITY CHECK DIVERT CONTROL (PDIV)
CONTROL FLIP-FLOP TO ALLOW PARITY CHECK (CTRLPK)
I/O PARITY ERROR IF ANY

NOTES:

1. THE NOP MICROCYCLE IS AN EXAMPLE OF ONE OF THE CONTROL SIGNALS THAT CAN INHIBIT THE GB PARITY CHECK. IF THE NOP MICROCYCLE WAS ACTIVE THE CTRLPK WOULD NOT GET SET AND THE GB PARITY CHECK WOULD BE PREVENTED.

CIRCUIT OPERATION (CONT)

5. MISCELLANEOUS DECODER - THE MISCELLANEOUS DECODER MUST INHIBIT THE GB PARITY CHECKER BECAUSE ON THE MICROCYCLE IN WHICH THE MISCELLANEOUS DECODER OPERATES, NO DATA IS GATED TO THE GB.

6. SIRC - THE SIRC IS A FROM-FIELD CROSSPOINT THAT CONDITIONALLY GATES FROM THE SIRC REGISTER WHEN WAITING FOR THE MEMORY OPERATION TO COMPLETE. IF THE MEMORY OPERATION HAS NOT COMPLETED, NO DATA IS GATED FROM THE SIRC REGISTER TO THE GB AND HENCE, THE GB PARITY CHECKER MUST BE DISABLED FOR EACH MICROCYCLE IN WHICH NO DATA IS GATED FROM THE SIRC.

7. SORC - THE SORC PERFROMS EXACTLY THE SAME TO THE SIRC EXCEPT THAT IT GATES FROM THE SORC REGISTER TO THE GB.

8. NA-BPC - THE NEXT ADDRESS FIELD AUXILLIARY DECODER BLOCK PARITY CHECK IS AN INDEPENDENT CONTROL SIGNAL (i.e. PERFORMS ONLY THIS FUNCTION) THAT PERMITS THE GB PARITY CHECK TO BE TURNED OFF FOR ONE MICROCYCLE. THIS TYPICALLY ALLOWS A REGISTER WITH BAD PARITY TO BE GATED TO THE DML WHERE PARITY CAN BE COMPUTED.

THERE IS ANOTHER SET OF CONTROL SIGNALS THAT INSTEAD OF INHIBITING THE GB PARITY CHECK, DIVERT THE ERROR OUTPUT TO ANOTHER BIT IN THE 3A CC ER REGISTER. THS DIVERSION PERMITS MORE GRACEFUL ERROR RECOVERY STRATEGY THAN THE "STOP AND SWITCH" OF 3A CC THAT WOULD OTHERWISE OCCUR IF A GB PARITY ERROR RESULTS. THE DIVERTED ERROR IS CALLED AN I/O PARITY ERROR AND WILL CAUSE AN ERROR INTERRUPT. AS THE NAME IMPLIES THE GB PARITY CHECK IS TYPICALLY USED TO CHECK THE PARITY ON INCOMING MESSAGES FROM THE I/O CHANNELS. THERE ARE TWO CONTROL SOURCES THAT DIVERT THE GB PARITY ERROR TO AN I/O PARITY ERROR AND BOTH ARE ENABLED FROM THE NEXT ADDRESS FIELD AUXILLIARY DECODER. THEY ARE:

1. NA I/O PARITY DIVERT. THIS CONTROL IS TYPICALLY ENABLED WHEN GATING R11 TO THE GB AFTER R11 HAS BEEN LOADED FROM THE I/O. FOR THE SERIAL I/O CHANNELS R11 IS LOADED FROM THE IOD REGISTER (SEE SHEET B1DGA).

2. NA DML MATCH DIVERT. AS EXPLAINED IN FS 2, SHEET B2GR, THE ABILITY TO DIVERT A DML MATCH ERROR IS PROVIDED. IT GIVES THE SAME TYPE OF CAPABILITY AS THE I/O PARITY DIVERT. THAT IS, AN INTERRUPT ERROR IS CAUSED INSTEAD OF A "STOP AND SWITCH" ERROR. SINCE PARITY IN THE DML IS GENERATED FROM DML1 AND THE DATA ORIGINATES FROM DMLD IF DML MISMATCH OCCURS A GB PARITY ERROR WILL ALSO OCCUR. THEREFORE, THE GB PARITY ERROR MUST BE DIVERTED WHEN THE DML MATCH DIVERT FUNCTION IS PERFORMED IF A "STOP AND SWITCH" IS TO BE PREVENTED.

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 6 AND 7

THE PURPOSE OF THE GB PARITY CHECKER IS TO INSURE THAT ON EVERY MICROCYCLE CORRECT PARITY IS PLACED ON THE GB. THE CORRECT PARITY IS DEFINED AS HAVING ODD PARITY IN THE BIT POSITIONS 0 THROUGH 7 TOGETHER WITH THE PL BIT ON THE GB AND ODD PARITY IN THE BIT POSITION 8 THROUGH 19 TOGETHER WITH THE PH BIT.

THE GB PARITY CHECKER OPERATES BY STROBING THE CONTENTS OF THE GB INTO A BUFFER REGISTER ON CLOCK PHASE P3 OF EVERY MICROCYCLE. BY PLACING THE GB CONTENT IN A BUFFER REGISTER, SUFFICIENT TIME IS ALLOWED FOR THE CONTENTS OF THIS BUFFER REGISTER TO RIPPLE THROUGH THE PARITY TREES ATTACHED TO IT. SINCE PARITY CHECK WILL NOT BE COMPUTED UNTIL THE FOLLOWING MICROCYCLE ON WHICH THE DATA WAS ACTUALLY PLACED ON THE GB, IT IS ALSO NECESSARY TO BUFFER CONTROL SIGNALS THAT INDICATE WHETHER THE GB PARITY CHECK MUST BE INHIBITED. THESE CONTROL FUNCTIONS ARE USED TO INDICATE THAT INCORRECT PARITY MAY OR WILL BE PLACED ON THE GB. THIS PROVIDES THE ABILITY TO ACCESS REGISTERS VIA THE GB WHOSE CONTENTS, FOR ONE REASON OR ANOTHER, MAY CONTAIN INVALID PARITY.

IN ADDITION, THERE ARE SOME MICROCYCLES IN WHICH NO DATA IS GATED TO THE GB, AND AS A RESULT, THIS IS TREATED AS ALL-ZEROS DATA WITH EVEN PARITY. THEREFORE, THIS REPRESENTS AN INVALID CONDITION ON THE GB AND FOR THIS MICROCYCLE AND GB PARITY CHECK MUST BE INHIBITED. MOST OF THE CONTROL SIGNALS THAT INHIBIT THE GB PARITY CHECK INHIBIT IT FOR A SINGLE CYCLE WHERE KNOWN BAD PARITY OR UNKNOWN DATA IS PLACED ON THE GB.

THERE ARE SOME CONTROL SIGNALS WHICH PERMANENTLY DISABLE THE GB PARITY CHECK. FOR EXAMPLE, THE BLOCK BUS PARITY CHECK BIT IN THE SS REGISTER (SSBPCD). IT IS TYPICALLY SET DURING INITIALIZATION TO ALLOW THE MACHINE TO BE INITIALIZED AND TO PURGE REGISTERS OF POSSIBLE BAD PARITY THROUGHOUT THE MACHINE. ONCE GOOD PARITY HAS BEEN ENSURED WITHIN THE MACHINE, THE BPC STATE IS CLEARED AND HENCE A PARITY CHECK IS PERFORMED FROM THAT POINT ON.

THE FOLLOWING IS A LIST OF THE CONTROL FUNCTIONS THAT CAN INHIBIT THE GB PARITY CHECKER:

1. THE STOP FLIP-FLOP - THE STOP FLIP-FLOP IS A DC CONDITION AND THEREFORE WILL INHIBIT THE GB PARITY CHECK UNTIL THE STOP FLIP-FLOP IS CLEARED. THE STOP STATE RESULTS IN INHIBITING THE MICROCONTROL SEQUENCING AND HENCE THE GB PARITY CHECK SHOULD BE INHIBITED.

2. THE BLOCK BUS PARITY CHECK - THE BLOCK BUS PARITY CHECK IS A DC CONDITION AND, AS DESCRIBED ABOVE, WILL INHIBIT THE GB PARITY CHECK UNTIL IT IS CLEARED.

3. THE FREEZE FLIP-FLOP - THE FREEZE FLIP-FLOP IS A DC CONDITION AND WILL INHIBIT THE GB PARITY CHECK UNTIL IT IS CLEARED. THE FREEZE STATE ALSO INHIBITS MICROCONTROL SEQUENCING.

4. THE NOP MICROINSTRUCTION - THE NOP MICROINSTRUCTION ALLOWS THE MICROCONTROL TO WAIT ONE MICROCYCLE BEFORE PERFORMING ANOTHER OPERATION. BECAUSE ZEROS ARE IN EFFECT GATED TO THE GB, THE NOP CONTROLPOINT WHICH IS GENERATED FROM A FROM-FIELD CROSSPOINT MUST INHIBIT THE GB PARITY CHECKER FOR THAT SINGLE CYCLE.

PART OF FS 6
COMPOSITE DIAGRAM 7

3A CENTRAL CONTROL

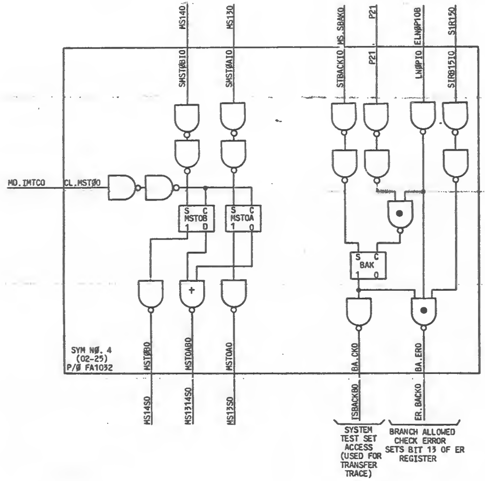
	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	96GG

PART OF FS 6

DATA TRANSFER CHECK CIRCUITS

COMPOSITE DIAGRAM 8

SPECIAL MS BUFFERING FOR BRANCH ALLOWED CHECK CIRCUIT



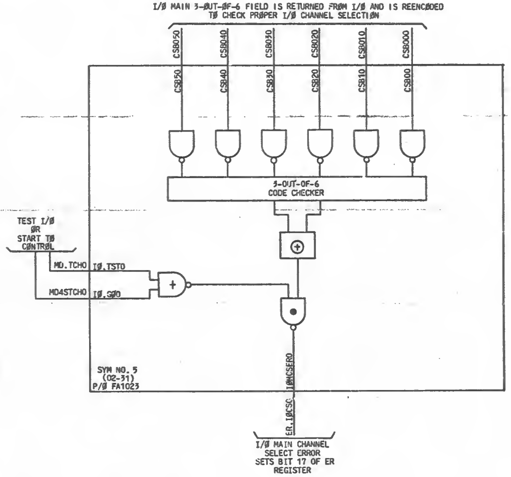
SYSTEM TEST SET ACCESS (USED FOR TRANSFER TRACE)

BRANCH ALLOWED CHECK ERROR SETS BIT 13 OF ER REGISTER

COMPOSITE DIAGRAM 9

I/O MAIN CHANNEL
3-OUT-OF-6 CODE CHECK

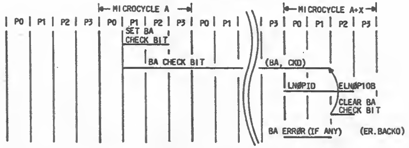
I/O MAIN 3-OUT-OF-6 FIELD IS RETURNED FROM I/O AND IS REENCODED TO CHECK PROPER I/O CHANNEL SELECTION



I/O MAIN CHANNEL SELECT ERROR SETS BIT 17 OF ER REGISTER

COMPOSITE DIAGRAM 10

TIMING DIAGRAM FOR THE BRANCH ALLOWED CHECK CIRCUIT



CIRCUIT OPERATION

IN ADDITION TO THE BA CHECK LOGIC, COMPOSITE DIAGRAM 8 CONTAINS TWO BUFFER FLIP-FLOPS FOR THE MAINTENANCE STATE SIGNALS USED FOR THE TESTING OF THE TO-FIELD CHECK LOGIC. THIS BUFFERING ON THE MAINTENANCE STATES IS PROVIDED BECAUSE IN THE PROCESS OF TESTING THE TO-FIELD CHECKER, THE CONTENTS OF THE MS REGISTER ARE DESTROYED BY THE ACTIVATION OF MULTIPLE TO-FIELD DECODER CROSSPOINTS. THE BUFFER FLIP-FLOPS WILL NOT BE AFFECTED BY THIS BECAUSE A MISCELLANEOUS DECODER CROSSPOINT IS USED TO CLEAR IT AND MULTIPLE TO-FIELD CONTROL SIGNALS WILL NOT ACTIVATE A MISCELLANEOUS DECODER UNLESS A UNIQUE FROM-FIELD CROSSPOINT IS ACTIVE.

THE BA CHECK LOGIC IS USED TO CHECK THE CORRECT OPERATION OF BRANCH INSTRUCTION IN THE EXECUTION FLOW OF MAIN MEMORY CODE. THE CHECK LOGIC OPERATES AS FOLLOWS: ON EVERY BRANCH INSTRUCTION A MICROCYCLE IS USED TO ACTIVATE A BA CHECK BIT (BAK). ON CONDITION BRANCHES THIS CHECK IS ONLY ACTIVATED IF THAT BRANCH IS TO BE TAKEN. WITH THE BAK BIT SET, THE HARDWARE LOGIC WAITS FOR THE NEXT INSTRUCTION TO BE LOADED FROM THE SIR TO IB AND MAR, AS SIGNALLED BY THE ELNOP10B CONTROL. AT THIS POINT IN TIME, THE STATE OF BIT 15 OF THE SIR IS SAMPLED. THE SAMPLING CORRESPONDS TO CHECKING BIT 15 OF THE TARGET ADDRESS AT WHICH EXECUTION FLOW IS TO BE CONTINUED. IF THIS BIT IS NOT SET, AN ERROR WILL OCCUR. THIS ERROR IS A MRF CLASS OF ERROR AND IT WILL CAUSE THE 3A CC TO INITIALIZE ITSELF.

COMPOSITE DIAGRAM 9 INDICATES HOW THE SELECTION OF THE CORRECT I/O MAIN CHANNEL IS VERIFIED. EACH EQUIPPED I/O MAIN CHANNEL REENCODES ITS ENABLE SIGNAL TO THE 3-OUT-OF-6 CODE THAT PRODUCED IT. THESE 3-OUT-OF-6 CODES ARE "OR"ED ONTO A COMMON I/O BUS AND ARE RETURNED TO THE 3-OUT-OF-6 CHECKER SHOWN IN COMPOSITE DIAGRAM 9. THE OUTPUT OF THIS CHECK IS THEN STROBED EACH TIME THE I/O IS EITHER TESTED (i.e. USING THE TEST I/O MICROINSTRUCTION) OR STARTED (i.e. USING THE START I/O MICROINSTRUCTION).

PART OF FS 6
COMPOSITE DIAGRAM 8,9,10

3A CENTRAL CONTROL
DWG SIZE 6S
ISSUE 5A
BELL LABORATORIES
SD-1C900-01
B6GH

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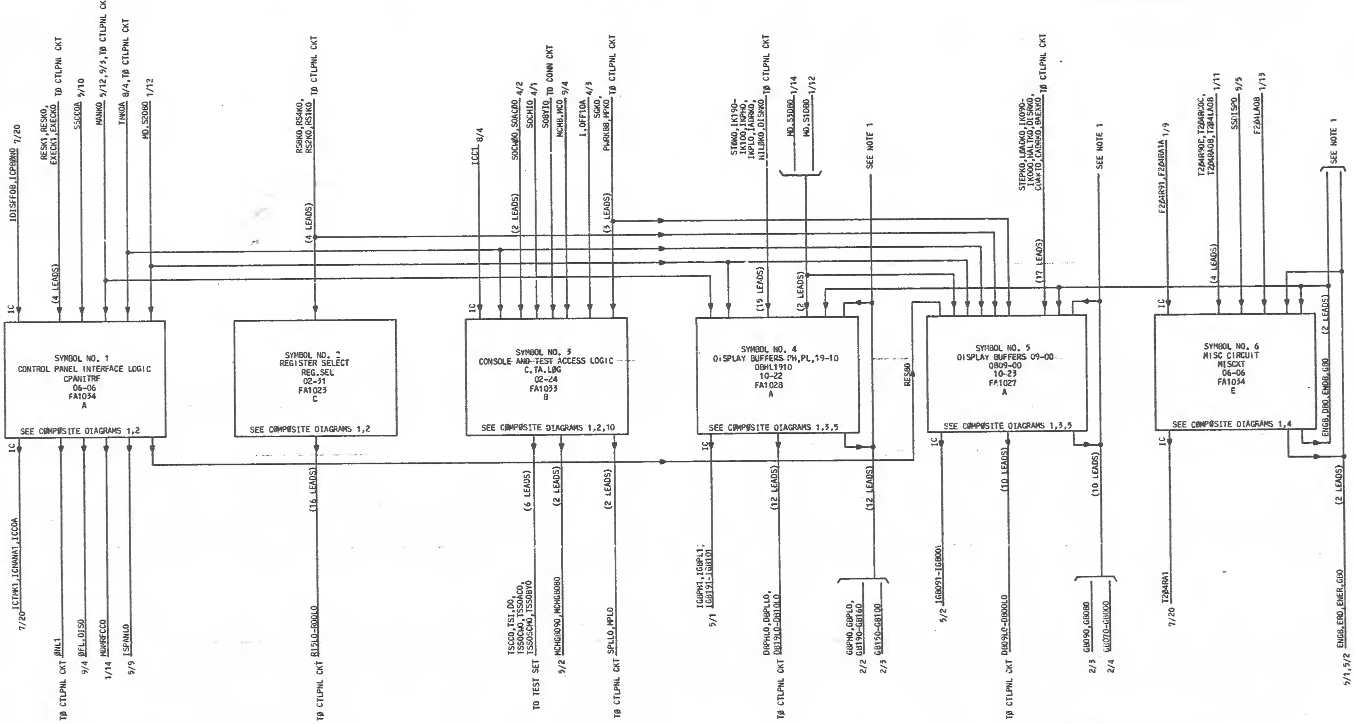
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (OI). ALL OFF-PAGE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.
2. FOR TO- AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 7
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B7AA

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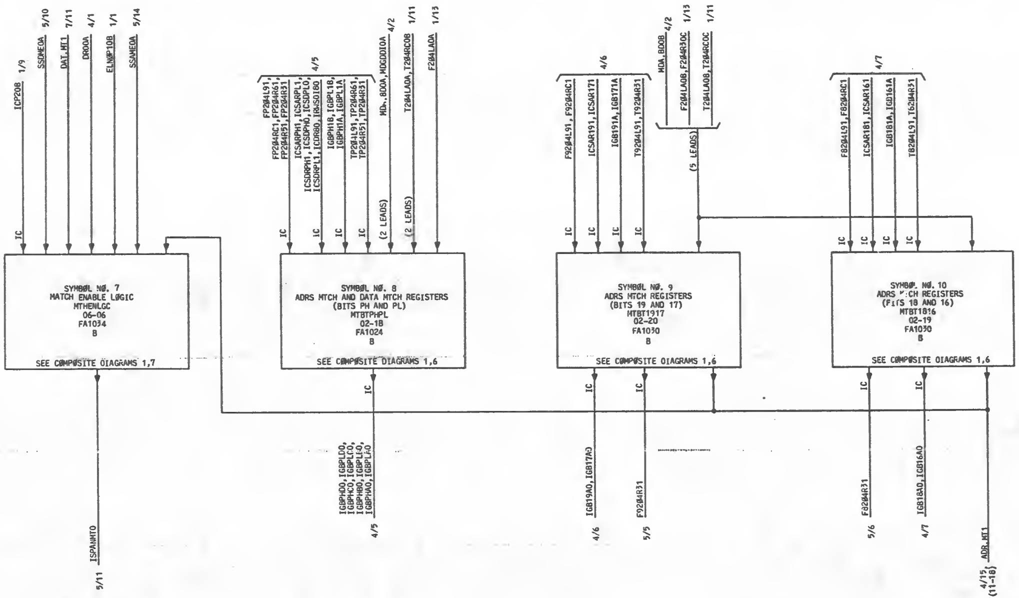
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FR[illegible]" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 7
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	B7AB

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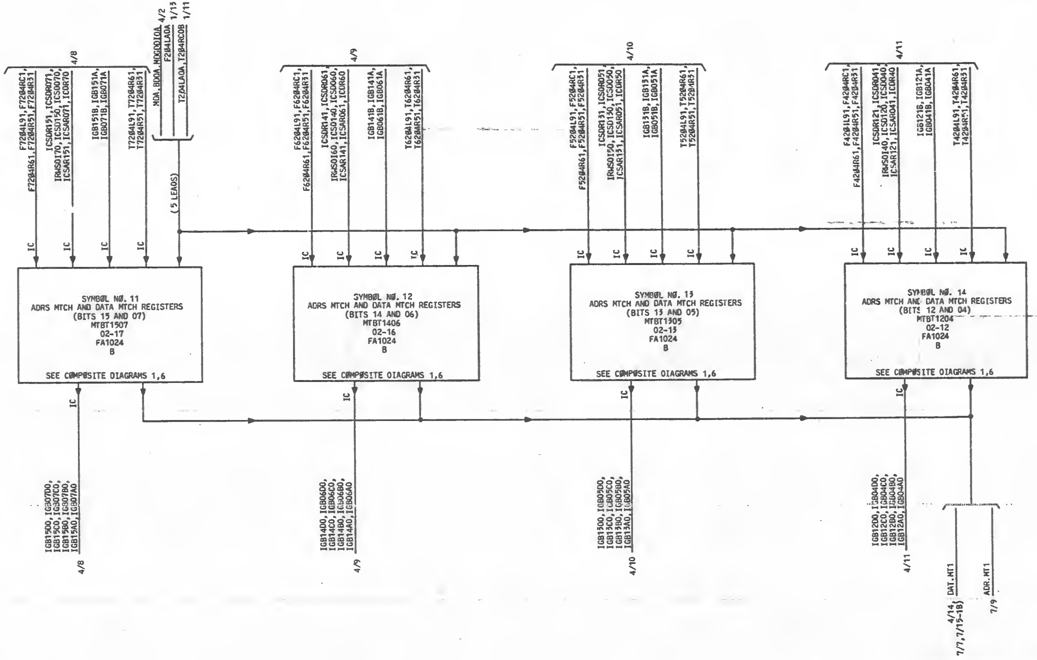
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 7
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 4A

BELL LABORATORIES

SD-1C900-01

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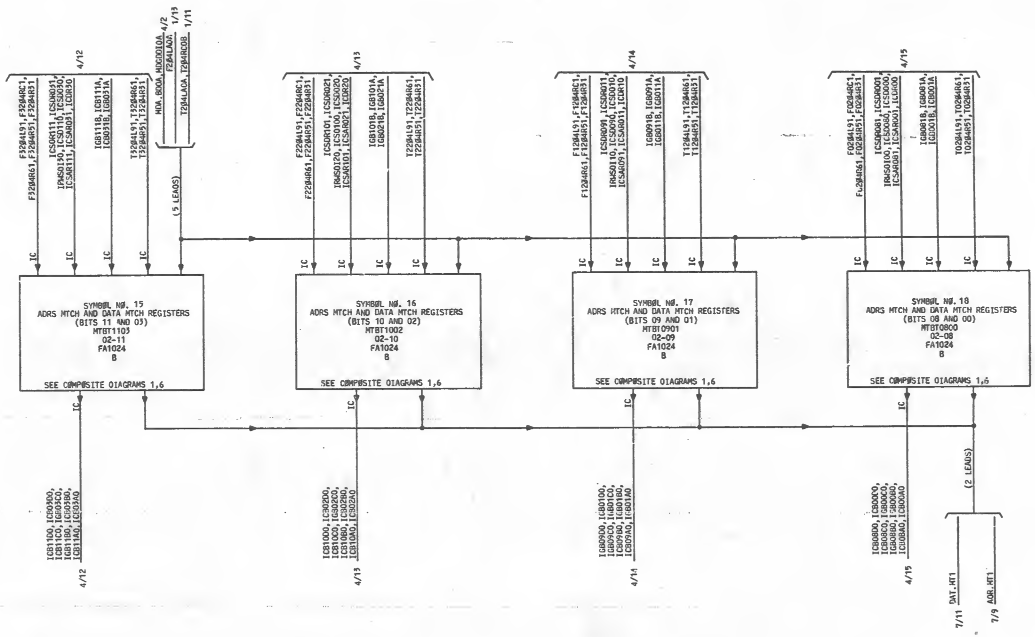
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.


4/12
F3204L91, F3204RC1, F3204R61, F3204R51, F3204R31
ICSDR111, ICSDR031, IPWSOI30, ICSD110, ICSD030, ICSAR111, ICSAR031, ICDR30
IGB111B, ICB111A, ICB031B, IGB031A
T3204L91, T3204R61, T3204R51, T3204R31
MDA, BDOA, MDGDDIOA 4/2
F204LAOA 1/13
T204LAOA, T204RCOB 1/11
(5 LEADS)
IC
SYMBOL NO. 15
ADRS MTCH AND DATA MTCH REGISTERS
(BITS 11 AND 03)
MTBT1103
02-11
FA1024
B
SEE COMPOSITE DIAGRAMS 1,6
ICB11D0, ICB03D0, ICB11C0, IGB03C0, IGB11B0, ICB03B0, ICB11A0, ICB03A0
4/12
4/13
F2204L91, F2204RC1, F2204R61, F2204R51, F2204R31
ICSDR101, ICSDR021, IRWSOI20, ICS0100, ICSD020, ICSAR101, ICSAR021, ICDR20
IGB101B, IGB101A, IGB021B, IGB021A
T2204L91, T2204R61, T2204R51, T2204R31
SYMBOL NO. 16
ADRS MTCH AND DATA MTCH REGISTERS
(BITS 10 AND 02)
MTBT1002
02-10
FA1024
B
SEE COMPOSITE DIAGRAMS 1,6
ICB10D0, IC302D0, ICB10C0, IG302C0, ICB10B0, ICB02B0, ICB10A0, IC902A0
4/13
4/14
F1204L91, F1204RC1, F1204R61, F1204R51, F1204R31
ICSDR091, ICSDR011, IRWSOI10, ICSD090, ICSD010, ICSAR091, ICSAR011, ICDR10
IGB091B, IGB091A, IGB011B, IGB011A
T1204L91, T1204R61, T1204R51, T1204R31
SYMBOL NO. 17
ADRS MTCH AND DATA MTCH REGISTERS
(BITS 09 AND 01)
MTBI0901
02-09
FA1024
B
SEE COMPOSITE DIAGRAMS 1,6
IGB09D0, IGB01D0, IGB09C0, IGB01C0, ICB09B0, IGB01B0, ICB09A0, IGB01A0
4/14
4/15
F0204L91, F0204RC1, F0204R61, F0204R51, F0204R31
ICSDR081, ICSDR001, IRWSOI00, ICSD080, ICSD000, ICSAR081, ICSAR001, ICDR00
IGB081B, IGB081A, IGB001B, ICB001A
T0204L91, T0204R61, T0204R51, T0204R31
SYMBOL NO. 18
ADRS MTCH AND DATA MTCH REGISTERS
(BITS 08 AND 00)
MTBT0800
02-08
FA1024
B
SEE COMPOSITE DIAGRAMS 1,6
ICB08D0, ICB00C0, ICB08C0, IGB00C0, IGB08B0, IGB00B0, ICB08A0, ICB00A0
4/15
(2 LEADS)
DAT.MT1 7/11
ADR.MT1 7/9

PART OF FS 7
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	B7AD

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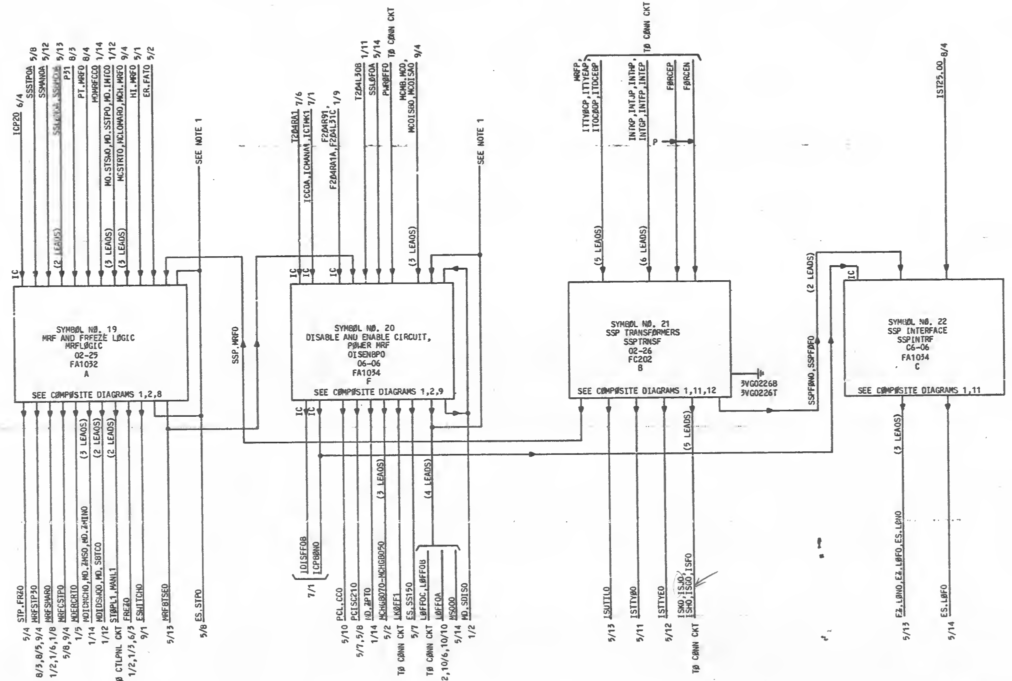
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (ØI). ALL OFF PACE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.
2. FOR TO- AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART OF FS 7
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B7AE

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PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ADR.MT1	ADDRESS MATCH OF MAIN MEMORY (UNSTROBED)
BAEXKO	PANEL BASIC OR EXTENDED KEY
CADRKO	PANEL ADDRESS MATCH KEY
CDAKTO	PANEL DATA MATCH KEY
OAT.MT1	DATA MATCH ON MAIN MEMORY (UNSTROBED)
DBPHLO	PANEL PARITY HIGH OF THE DB LAMP INDICATOR
OBPLLO	PANEL PARITY LOW OF THE DB LAMP INDICATOR
DB00LO-OB19LO	PANEL BITS 0-19 OF THE DB LAMP INDICATORS
OISMKO	PANEL DISPLAY MEMORY KEY
OISRKO	PANEL DISPLAY REGISTER KEY
DROOA	DATA READY FLIP-FLOP (COPY 0)
ELNOP10B	ENABLE LOAD NEW OP CODE (COPY 1)
ENOB.GBO	ENABLE DISPLAY BUFFER TO THE GATING BUS
ENER.GBO	ENABLE ERROR REGISTER TO THE GATING BUS
ENGB.OBO	ENABLE GATING BUS TO THE DB
ENGB.ERO	ENABLE GATING BUS TO THE ER
ER.FATO	FATAL ERROR ("OR" OF BITS 0-9 OF THE ERROR REGISTER)
ES.LOFO	ENABLE SET OF LOCK OFF-LINE FLIP-FLOP (BIT 8 OF THE SS)
ES.LONO	ENABLE SET LOCK ON-LINE FLIP-FLOP (BIT 9 OF THE SS)
ES.SS150	ENABLE SET BIT 15 OF THE SS (SHADOW OF DISABLE FLIP-FLOP)
ES.STPO	ENABLE SET OF STOP FLIP-FLOP (BIT 14 OF THE SS)
ESWITCHO	ENABLE A CENTRAL CONTROL SWITCH VIA MCA
EXECKO	PANEL EXECUTE KEY (LOW ACTIVE)
EXECK1	PANEL EXECUTE KEY (HIGH ACTIVE)
EZ.LOFO	ENABLE ZEROING OF LOCK OFF-LINE FLIP-FLOP
EZ.LONO	ENABLE ZEROING OF LOCK ON-LINE FLIP-FLOP
FORCEN	SYSTEMS STATUS PANEL FORCE (NEGATIVE POLARITY)
FORCEP	SYSTEMS STATUS PANEL FORCE (POSITIVE POLARITY)
FREZO	MAR FREEZE CONTROL LEAD
GBPHO	PARITY HIGH OF THE GATING BUS
GBPLO	PARITY LOW OF THE GATING BUS
GB000-GB190	BITS 0-19 OF THE GATING BUS
HALTKO	PANEL HALT KEY
HI.MRFO	HARDWARE INITIALIZATION ERROR "MRF" (MAINTENANCE RESET FUNCTION)
HILOKO	PANEL HIGH-LOW MEMORY KEY
I.OFF10A	OUTPUT OF THE INSTRUCTION OR DATA FLIP-FLOP (COPY 1)
IADRKO	PANEL INCREMENT ADDRESS KEY

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ICCOA	OUTPUT OF CC FLIP-FLOP [IC]
ICC1	OUTPUT OF CC FLIP-FLOP [IC]
ICDR00-ICDR80	OUTPUT OF CR FLIP-FLOP [IC]
ICMANA1	MANUAL MODE INDICATION [IC]
ICPBONO	POWER ON INITIALIZATION SIGNAL [IC]
ICPZO	CLOCK PHASE PZO [IC]
ICPZOB	CLOCK PHASE PZO [IC]
ICSARPH1	PARITY HIGH, SAR REGISTER [IC]
ICSARPL1	PARITY LOW, SAR REGISTER [IC]
ICSAR001-ICSAR191	BITS 0-19 OF THE SAR REGISTER [IC]
ICSDPHO	PARITY HIGH OF THE MAIN STORE DATA BUS [IC]
ICSOPLO	PARITY LOW OF THE MAIN STORE DATA BUS [IC]
ICSDRPH1	PARITY HIGH OF THE SDRO [IC]
ICSDRPL1	PARITY LOW OF THE SDRO [IC]
ICSDR001-ICSDR151	BITS 0-15 OF THE SDRO [IC]
ICS0000-ICS0150	BITS 0-15 OF THE MAIN STORE DATA BUS [IC]
ICTMK1	PANEL TEST MODE REVERSAL KEY [IC]
IOISFFOB	DISABLE FLIP-FLOP OUTPUT [IC]
IGBPH(A-O)O	INPUTS TO PARITY HIGH OF THE GATING BUS [IC]
IGBPH1	INPUT TO PARITY HIGH OF GATING BUS [IC]
IGBPH1(A,B)	OUTPUTS OF PARITY HIGH OF THE GATING BUS [IC]
IGBPLA0-IGBPLO0	OUTPUTS OF GATING BUS BIT PL [IC]
IGBPL1	INPUTS TO PARITY LOW OF THE GATING BUS [IC]
IGBPL1(A,B)	OUTPUTS FROM PARITY LOW OF THE GATING BUS [IC]
IGB00A0-IGB19A0	INPUTS TO GATING BUS BITS 0-19 [IC]
IGB00B0-IGB15B0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB00C0-IGB15C0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB00D0-IGB15D0	INPUTS TO GATING BUS BITS 0-15 [IC]
IGB001-IGB191	OUTPUTS FROM GATING BUS BITS 0-19 [IC]
IGB001A-IGB191A	OUTPUT OF GATING BUS BITS 0-19 [IC]
IGB001B-IGB151B	OUTPUT OF GATING BUS BITS 0-15 [IC]
IKPHO	PANEL PARITY HIGH INPUT DATA KEY
IKPLO	PANEL PARITY LOW INPUT DATA KEY
IK000-IK190	PANEL BITS 0-19 INPUT DATA KEYS
INTEP	INTERRUPT E INPUT (POSITIVE LEAD)
INT(F-H,J,K)P	SIMILARLY FOR INTERRUPT LEADS F, G, H, J, K
IRWSOI(0-8)O	READ-WRITE CONTROL FOR MY STORE BUS, BITS 0-8 [IC]
IS(F-H,J,K)O	OUTPUTS OF INTERRUPT TRANSFORMERS, F, G, H, J, AND K

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ISPANLO	PANEL INTERRUPT SET INPUT (SETS BIT 13 OF THE IS)
ISPANMTO	PANEL MATCH INTERRUPT INPUT (SETS BIT 3 OF THE IS)
ISTTYEO	EVEN TTY INTERRUPT SET INPUT (SETS BIT 10 OF THE IS)
ISTTYOO	ODD TTY INTERRUPT SET INPUT (SETS BIT 11 OF THE IS)
IST25.00	25-MILLISECOND INTERRUPT SET
ISUTILO	UTILITY INTERRUPT SET INPUT
ITDCEBP	EVEN TOC INTERRUPT (POSITIVE LEAD)
ITDCODP	ODD TOC INTERRUPT (POSITIVE LEAD)
ITTYEAP	EVEN TTY INTERRUPT (POSITIVE LEAD)
ITTYOCP	ODD TTY INTERRUPT (POSITIVE LEAD)
LKOFF1	LOCK OFF-LINE INDICATION (ALLOWS POWER TURNOFF)
LOADKO	PANEL LOAD REGISTER KEY
LOFFO(A-C)	LOCK OFF-LINE OR DISABLE INDICATION (DISABLES IO)
MANKO	PANEL MANUAL KEY
MANL1	PANEL MANUAL LAMP INDICATOR
MCDISAO	MCA CONTROL, DISABLE A
MCDISBO	MCA CONTROL, DISABLE B
MCH.MRFO	MCA INITIALIZATION LEAD TO THE CENTRAL CONTROL
MCHGB050-MCHGB090	BITS 5-9 OF MCA GATING BUS
MCLDMARO	MCA CONTROL, LOAD THE MAR AND SET THE FREEZE FLIP-FLOP
MCMB.MCO	MCA CONTROL, LOAD THE MISCELLANEOUS BIT'S REGISTER INTO THE MCA
MCSTRTO	MCA CONTROL, CLEAR THE FREEZE FLIP-FLOP AND START THE MICROCONTROL
MD.IMTCO	MISC. DECODER, CLEAR THE IMRF.MCH FLIP-FLOP. THIS FLIP-FLOP PREVENTS THE MCH FROM BEING INITIALIZED IF THE MCH ORIGINATES THE MRF.
MD.SBTCO	MISC. DECODER, SET BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)
MD.SOISO	MISC. DECODER, SET DISABLE FLIP-FLOP
MD.SSTPO	MISC. DECODER, SET STOP FLIP-FLOP (BIT 14 OF THE SS)
MD.STSWO	MISC. DECODER, STOP AND SWITCH CENTRAL CONTROL
MD.S1OBO	MISC. DECODER, GATE SWITCH REGISTER 1 TO THE DB
MD.S2DBO	MISC. DECODER, GATE SWITCH REGISTER 2 TO THE DB
MD.S3OBO	MISC. DECODER, GATE SWITCH REGISTER 3 TO THE DB
MD.ZMINO	MISC. DECODER, ZERO THE MICROINTERPRET BIT (BIT 11 OF THE SS)
MD.ZMSO	MISC. DECODER, ZERO THE MAINTENANCE STATE REGISTER
MD.ZPTO	MISC. DECODER, ZERO THE PROGRAM TIMER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MDA.BDO(A,B)	ENABLE GATING OF THE BAD DATA AND THE ADDRESS OF A DOUBLE STORE READ OPERATION TO THE DK AND AK REGISTERS RESPECTIVELY
MDERCRTO	MISCELLANEOUS DECODER RETURN FROM COMPLEMENT CORRECTION MICROSUBROUTINE
MDGDDIOA	ENABLE GATING OF THE GOOD DATA OF THE DOUBLE STORE READ OPERATION TO THE DI REGISTER
MDIDMCHO	MISC. DECODER, IDLE THE MCA
MDIDSWOO	MISC. DECODER, IDLE THE SWITCH SEQUENCER
MDMRFCCO	MISC. DECODER, MAINTENANCE RESET FUNCTION (MRF) TO THE CENTRAL CONTROL
MPKO	PANEL MANUAL PARITY KEY
MPLO	PANEL MANUAL PARITY LAMP INDICATOR
MRFBTSEO	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) SET THE BTC FLIP-FLOP AND CLEAR THE SEMI-ENABLE FLIP-FLOPS FOR THE DISABLE FUNCTION
MRFCSTPO	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) CLEAR STOP FLIP-FLOP
MRFP	MAINTENANCE RESET FUNCTION INPUT FROM SYSTEM STATUS PANEL (POSITIVE LEAD)
MRFSMARO	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) SET MAR TO STARTING INITIALIZATION ADDRESS
MRFSTP30	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) SET CLOCK TO PHASE P3
MS000	BIT 0 OF THE MAINTENANCE STATE REGISTER (OVERRIDE I/O DISABLING)
OFL.OISO	INDICATES CC IN LOCKED OFF-LINE OR DISABLED
ONL1	PANEL LAMP INDICATOR, OUTPUT OF CC FLIP-FLOP INDICATES CC IS IN THE ACTIVE MODE OR ON-LINE (BIT 12 OF THE SS)

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 4A

BELL LABORATORIES

SD-1C900-01

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PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
PCISC210	POWER INITIALIZATION, CLEAR ISC BITS 1 AND 2 (BITS 6 AND 7 OF THE SS)
PCL.CC0	POWER INITIALIZATION, CLEAR CC FLIP-FLOP (BIT 12 OF THE SS)
PT.MRF0	PROGRAM TIMER TIMEOUT, INITIATE A MAINTENANCE RESET FUNCTION
PWRKBB	POWER KEY BB CONTACT (SETS BIT 19 OF SS)
PWROFF0	POWER INITIALIZATION SIGNAL TO THE CENTRAL CONTROL
P31	CLOCK PHASE P3 (POSITIVE ACTIVE)
RESB0	PANEL RESET CIRCUITS FLIP-FLOP OUTPUT
RESK0	PANEL RESET CIRCUITS KEY (LOW ACTIVE)
RESK1	PANEL RESETS CIRCUIT KEY (HIGH ACTIVE)
RS1K0	PANEL REGISTER SELECT (1) KEY
RS2K0	PANEL REGISTER SELECT (2) KEY
RS4K0	PANEL REGISTER SELECT (4) KEY
RS8K0	PANEL REGISTER SELECT (8) KEY
R00L0-R09L0	PANEL REGISTER SELECT LAMP INDICATORS BIT 0-9
R10L0-R15L0	PANEL REGISTER SELECT LAMP INDICATORS BIT 10-15
SGK0	PANEL SPECIAL OR GENERAL REGISTER SELECT KEY
SPLL0	PANEL SPECIAL REGISTER SELECT LAMP INDICATOR
SSAME0A	ADDRESS MATCH ENABLE BIT (BIT 0 OF THE SS)
SSBHC0A	BLOCK HARDWARE CHECK BIT (BIT 1 OF THE SS)
SSCC0A	CENTRAL CONTROL ON-LINE BIT (BIT 12 OF THE SS)
SSDISP0	DISPLAY BIT (BIT 17 OF THE SS)
SSDME0A	DATA MATCH ENABLE BIT (BIT 4 OF THE SS)
SSLOF0A	LOCK OFF-LINE BIT (BIT 8 OF THE SS)
SSLON0A	LOCK ON-LINE BIT (BIT 9 OF THE SS)
SSMAN0A	MANUAL BIT (BIT 10 OF THE SS)
SSP.MRF0	SYSTEM STATUS PANEL MAINTENANCE RESET FUNCTION OF THE CENTRAL CONTROL
SSPF0F0	SYSTEM STATUS PANEL FORCE OFF-LINE FUNCTION
SSPF0N0	SYSTEM STATUS PANEL FORCE ON-LINE FUNCTION
SSSTP0A	STOP FLIP-FLOP BIT (BIT 14 OF THE SS)
STEPK0	PANEL STEP KEY
STOK0	PANEL STORE IN MEMORY KEY
STOPL1	PANEL CENTRAL CONTROL ERROR STOP LAMP INDICATOR
STP.FRZ0	"OR" OF THE STOP FLIP-FLOP AND THE FREEZE FLIP-FLOP
S0ACD0	MY MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL OUTPUT
S0BYI0	MY MAIN STORE BUS STORE BUSY INPUT

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
S0CMI0	MY MAIN STORE BUS STORE COMPLETE SIGNAL INPUT
S0CW00	MY MAIN STORE BUS COMPLEMENT WRITE SIGNAL OUTPUT
TMK0A	PANEL TEST MODE REVERSAL KEY
TSCC0	TEST SET ACCESS, CC FLIP-FLOP OUTPUT
TSI.D0	TEST SET ACCESS, INSTRUCTION OR DATA FLIP-FLOP OUTPUT
TSS0AC0	TEST SET ACCESS POINT AUTOMATIC ERROR CORRECTION SIGNAL
TSS0BY0	TEST SET ACCESS POINT, MY STORE BUSY SIGNAL
TSS0CW0	TEST SET ACCESS POINT AUTOMATIC ERROR CORRECTION SIGNAL
TSS0SCM0	TEST SET ACCESS POINT, MY STORE COMPLETE SIGNAL

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B7AG

PRINTED IN U. S. A.

11/17/75

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL NO. 1

CONTROL PANEL INTERFACE LOGIC

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CPANITRF	06-06	FA1034	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
EXECK0	I	310	TO CTLPNL CKT		EXECKI0	2A5
EXECK1	I	011	TO CTLPNL CKT		EXECKI1	2A5
ICCOA	0	IC	7/20		CCOA	2H1
ICMANA1	0	IC	7/20		MANA1	2H1
ICPBONO	I	IC	7/20		PBONO	2A4
ICTMK1	0	IC	7/20		TMK1	2H1
IDISFF08	I	IC	7/20		DISFF08	2A0
ISPANL0	0	115	5/9		EXEC0	2H6
MANK0	I	314	5/12,7/4 9/3 TO CTLPNL CKT	202	MANK0	2A0
MD.S2DB0	I	205	1/12		GS210	2A7
MDMRFCC0	OT	216	1/14		RESCK0A	2H4
OFL.0IS0	0	106	9/4		CC.DIS0	2H0
DNL1	0	016	TO CTLPNL CKT	202	CC1	2H1
RESB0	0	104	7/5		RESB0	2G7
RESK0	I	111	TO CTLPNL CKT		RESKI0	2A3
RESK1	I	311	TO CTLPNL CKT		RESKI1	2A3
SSCC0A	I	214	5/10		CCI0	2A1
TMK0A	I	114	7/3,7/5 8/4 TO CTLPNL CKT		TMK0A	2A1
3T0588	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V0588	PWR	000		203	+3	
	FWR	119		203	+3	

SYMBOL NO. 2

REGISTER SELECT

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
REG.SEL	02-31	FA1023	C	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
RS1K0	I	112	7/5	202	RS1K0	6A2
RS2K0	I	212	7/5	202	RS2K0	6A2
RS4K0	I	012	7/5	202	RS4K0	6A2
RS8K0	I	010	7/5	202	RS8K0	6A1
R00L0	0	203	TO CTLPNL CKT	202	R0L0	6G6
R01L0	0	006	TO CTLPNL CKT	202	R1L0	6G6
R02L0	0	305	TO CTLPNL CKT	202	R2L0	6G6
R03L0	0	104	TO CTLPNL CKT	202	R3L0	6G5
R04L0	0	204	TO CTLPNL CKT	202	R4L0	6G5
R05L0	0	004	TO CTLPNL CKT	202	R5L0	6G5
R06L0	0	303	TO CTLPNL CKT	202	R6L0	6G4
R07L0	0	103	TO CTLPNL CKT	202	R7L0	6G4
R08L0	0	206	TO CTLPNL CKT	202	R8L0	6G4
R09L0	0	108	TO CTLPNL CKT	202	R9L0	6G3
R10L0	0	208	TO CTLPNL CKT	202	R10L0	6G3
R11L0	0	008	TO CTLPNL CKT	202	R11L0	6G3
R12L0	0	207	TO CTLPNL CKT	202	R12L0	6G2
R13L0	0	007	TO CTLPNL CKT	202	R13L0	6G2

SYMBOL NO. 2 (CONT)

REGISTER SELECT

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
REG.SEL	02-31	FA1023	C	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R14L0	0	306	TO CTLPNL CKT	202	R14L0	6G2
R15L0	0	106	TO CTLPNL CKT	202	R15L0	6G1

SYMBOL NO. 3

CONSOLE AND TEST ACCESS LOGIC

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
C.TA.LOG	02-24	FA1033	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
I.0FF10A	I	217	4/3		I.0I0	10A6
ICC1	I	IC	8/4		CC1	10A6
MCHG8080	OT	304	5/2	202	GPWK0	10G5
MCHG8090	OT	303	5/2	202	GTMK0	10G5
MCMB.MC0	I	012	9/4		GMB.MCH0	10A4
MPK0	I	216	7/5	202	MPK0	10A1
MPL0	0	104	TO CTLPNL CKT	202	MPL0	10G1
PWRK88	I	107	7/5 TO CTLPNL CKT		PWKI0	10A5
SGK0	I	101	7/5	202	RSGSK0	10A0
SPLL0	0	301	TO CTLPNL CKT	202	SPLL0	10G0
SOAC00	I	114	4/2		SOACI0	10A4
SOBYI0	I	017	TO CONN CKT		SOBYI0	10A2
SOCMI0	I	314	4/1		SOCMI0	10A2
SOCW00	I	212	4/2		SOCWI0	10A3
TMK0A	I	307	7/1		TMKI0	10A5
TSCC0	0	103			CC0	10G6
TSI.D0	0	203			I.D0	10G6
TSS0AC0	0	205			S0ACD	10G4
TSS0BY0	0	003			S0BY0	10G2
TSS0CW0	0	005			S0CW0	10G3
TSS0SCM0	0	100			S0CM0	10G2

SYMBOL NO. 4

DISPLAY BUFFERS PH,PL,19-10

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DBHL1910	10-22	FA1028	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
DBPHL0	0	219	TO CTLPNL CKT		DBPH0	3H2
DBPLL0	0	315	TO CTLPNL CKT		DBPL0	3H2
DB10L0	0	214	TO CTLPNL CKT		DB100	4H7
DB11L0	0	014	TO CTLPNL CKT		DB110	4H7
DB12L0	0	215	TO CTLPNL CKT		DB120	4H5
DB13L0	0	114	TO CTLPNL CKT		DB130	4H4
DB14L0	0	218	TO CTLPNL CKT		DB140	4H2
DB15L0	0	018	TO CTLPNL CKT		DB150	4H1
DB16L0	0	113	TO CTLPNL CKT		DB160	3H8
DB17L0	0	115	TO CTLPNL CKT		DB170	3H7
DB18L0	0	019	TO CTLPNL CKT		DB180	3H5
DB19L0	0	318	TO CTLPNL CKT		DB190	3H5
DISMK0	I	111	TO CTLPNL CKT		DISK0	4A6
ENDB.GB0	I	104	7/6		EDB.GBI0	2A4
ENGB.DB0	I	314	7/6		EGB.DBI0	3A0
GBPH0	OT	IC307	2/2		TGB.PH0	3H1
	OI	307	2/2		TGB.PH0	3H1
GBPL0	DT	IC107	2/2		TGB.PL0	3H2
	DI	107	2/2		TGB.PL0	3H3
GB100	OT	IC310	2/3		TGB.100	4G7
	OI	310	2/3		TGB.100	4H7
GB110	OT	IC110	2/3		TGB.110	4G6
	OI	110	2/3		TGB.110	4H6
GB120	OT	IC210	2/3		TGB.120	4G5
	OI	210	2/3		TGB.120	4H5
GB130	OT	IC010	2/3		TGB.130	4G3
	OI	010	2/3		TGB.130	4H4
GB140	OT	IC006	2/3		TGB.140	4G2
	OI	006	2/3		TGB.140	4H2
GB150	OT	IC206	2/3		TGB.150	4G0
	OI	206	2/3		TGB.150	4H1
GB160	OT	IC106	2/2		TGB.160	3G9
	OI	106	2/2		TGB.160	3H8
GB170	OT	IC306	2/2		TGB.170	3H6
	DI	306	2/2		TGB.170	3H7
GB180	OT	IC007	2/2		TGB.180	3H5
	OI	007	2/2		TGB.180	3H5
GB190	OT	IC207	2/2		TGB.190	3H3
	OI	207	2/2		TGB.190	3H4
HILOK0	I	205	TO CTLPNL CKT		HILOK0	4A0
IADRK0	I	112	TO CTLPNL CKT		IADRK0	4A3
IGBPH1	0	IC	5/1		GB.PHI1	2G4
IGBPL1	0	IC	5/1		GB.PLI1	2G4
IGB101	0	IC	5/1		GB.10I1	2G9
IGB111	0	IC	5/1		GB.11I1	2G8
IGB121	0	IC	5/1		GB.12I1	2G8
IGB131	0	IC	5/1		GB.13I1	2G7
IGB141	0	IC	5/1		GB.14I1	2G7
IGB151	0	IC	5/1		GB.15I1	2G7
IGB161	0	IC	5/1		GB.16I1	2G6
IGB171	0	IC	5/1		GB.17I1	2G6
IGB181	0	IC	5/1		GB.18I1	2G5
IGB191	0	IC	5/1		GB.19I1	2G5
IKPH0	I	317	TO CTLPNL CKT		IKPH0	3A1
IKPL0	I	117	TO CTLPNL CKT		IKPL0	3A3
IK100	I	011	TO CTLPNL CKT		IK100	4A8
IK110	I	211	TO CTLPNL CKT		IK110	4A6
IK120	I	311	TO CTLPNL CKT		IK120	4A5
IK130	I	012	TO CTLPNL CKT		IK130	4A4
IK140	I	016	TO CTLPNL CKT		IK140	4A3

SYMBOL NO. 4 (CONT)

DISPLAY BUFFERS PH,PL,19-10

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DBHL1910	10-22	FA1028	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IK150	I	216	TO CTLPNL CKT		IK150	4A1
IK160	I	116	TO CTLPNL CKT		IK160	3A8
IK170	I	316	TO CTLPNL CKT		IK170	3A6
IK180	I	017	TO CTLPNL CKT		IK180	3A6
IK190	I	217	TO CTLPNL CKT		IK190	3A4
MANK0	I	105	7/1	202	MANK0	4A8
MD.S1DB0	I	109	1/12		GS110	2A1
MD.S2DB0	I	209	1/12		GS210	2A2
MD.S3DB0	I	309	1/14		GS310	2A0
STOK0	I	212	TO CTLPNL CKT		STOK0	4A3
3T062C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V062C	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 7
SYMBOL(S) 1 2 3 4

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-0[illegible]

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06/10/77

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL NO. 5

DISPLAY BUFFERS 09-00

OESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DB09-00	10-23	FA1027	A	

FS INFO					CP INFO	
LEAD OESIG	FUNC	TERM.	OESTINATION	NOTE	TERM. MOD	LOC
BAEXKO	I	315	TO CTLPNL CKT		BAEXO	5A5
CADRKO	I	011	TO CTLPNL CKT		CADRKO	4A2
CDAKTO	I	110	TO CTLPNL CKT		CDAKTO	4A5
OB00LO	O	302	TO CTLPNL CKT		OB000	6H4
OB01LO	O	102	TO CTLPNL CKT		OB010	6H4
DB02LO	O	209	TO CTLPNL CKT		OB020	5G7
OB03LO	O	009	TO CTLPNL CKT		OB030	5G6
OB04LO	O	111	TO CTLPNL CKT		OB040	5H3
OB05LO	O	211	TO CTLPNL CKT		OB050	5H2
DB06LO	O	316	TO CTLPNL CKT		OB060	4G7
OB07LO	O	016	TO CTLPNL CKT		OB070	4G7
OB08LO	O	217	TO CTLPNL CKT		OB080	4H4
OB09LO	O	017	TO CTLPNL CKT		OB090	4H3
OISRKO	I	312	TO CTLPNL CKT		OISPKO	5A3
ENOB.GBO	I	014	7/6		EOB.GBIO	4A0
ENGB.DBO	I	115	7/6		EGB.DBIO	6A1
GB000	OT	IC301	2/4		TGB.000	6H4
	OI	301	2/4		TGB.000	6H5
GB010	OT	IC101	2/4		TGB.010	6H3
	OI	101	2/4		TGB.010	6H3
GB020	OT	IC205	2/4		TGB.020	5G7
	OI	205	2/4		TGB.020	5G7
GB030	OT	IC105	2/4		TGB.030	5G5
	OI	105	2/4		TGB.030	5H6
GB040	OT	IC005	2/4		TGB.040	5G2
	OI	005	2/4		TGB.040	5H3
GB050	OT	IC305	2/4		TGB.050	5G1
	OI	305	2/4		TGB.050	5H1
GB060	OT	IC208	2/4		TGB.060	4G7
	OI	208	2/4		TGB.060	4G7
GB070	OT	IC108	2/4		TGB.070	4G6
	OI	108	2/4		TGB.070	4H6
GB080	OT	IC008	2/3		TGB.080	4H4
	OI	008	2/3		TGB.080	4H4
GB090	OT	IC308	2/3		TGB.090	4H2
	OI	308	2/3		TGB.090	4H3
HALTKO	I	304	TO CTLPNL CKT		HALTKO	5A8
IGB001	O	IC	5/2		GB.0011	3G6
IGB011	O	IC	5/2		GB.0111	3G6
IGB021	O	IC	5/2		GB.0211	3G5
IGB031	O	IC	5/2		GB.0311	3G5
IGB041	O	IC	5/2		GB.0411	3G4
IGB051	O	IC	5/2		GB.0511	3G3
IGB061	O	IC	5/2		GB.0611	3G2
IGB071	O	IC	5/2		GB.0711	3G2
IGB081	O	IC	5/2		GB.0811	3G1
IGB091	O	IC	5/2		GB.0911	3G0
IK000	I	100	TO CTLPNL CKT		IK00	6A6
IK010	I	103	TO CTLPNL CKT		IK10	6A3
IK020	I	204	TO CTLPNL CKT		IK20	5A8
IK030	I	311	TO CTLPNL CKT		IK30	5A5
IK040	I	212	TO CTLPNL CKT		IK40	5A4
IK050	I	013	TO CTLPNL CKT		IK50	5A1
IK060	I	113	TO CTLPNL CKT		IK60	4A8
IK070	I	309	TO CTLPNL CKT		IK70	4A6
IK080	I	010	TO CTLPNL CKT		IK80	4A5
IK090	I	310	TO CTLPNL CKT		IK90	4A3
LOADKO	I	213	TO CTLPNL CKT		LOADKO	5A1
MO.S1DBO	I	201	1/12		GS11O	2A1
MO.S2DBO	I	001	1/12		GS21O	2A2

SYMBOL NO. 5 (CONT)

DISPLAY BUFFERS 09-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DB09-00	10-23	FA1027	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	OESTINATION	NOTE	TERM. MOD	LOC
MO.S3DBO	I	300	1/14		GS31O	2A2
MPKO	I	203	7/3 TO CTLPNL CKT	202	MPKO	6A5
PWRK8B	I	314	7/3		PWKO	4A2
RESBO	I	109	7/1		RESCKO	4A8
RS1KO	I	003	7/2 TO CTLPNL CKT	202	RS1KO	6A6
RS2KO	I	303	7/2 TO CTLPNL CKT	202	RS2KO	6A3
RS4KO	I	104	7/2 TO CTLPNL CKT	202	RS4KO	5A8
RS8KO	I	012	7/2 TO CTLPNL CKT	202	RS8KO	5A5
SGKO	I	112	7/3 TO CTLPNL CKT	202	SGKO	5A4
STEPKO	I	004	TO CTLPNL CKT	202	STEPKO	6A2
TMKOA	I	210	7/1		TMKOA	4A6
3T062C	GRO	0GO		203	GRD	
	GRO	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V062C	PWR	000		203	+3	
	PWR	11/		203	+3	

SYMBOL NO. 6

MISC CIRCUIT

DESIG	EQPT LOC	CODE	ELEM IOENT	OPT
MISCKT	06-06	FA1034	E	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ENOB.GBO	OI	008	7/4,7/5		DB.GBO	7H2
ENER.GBO	OI	306	5/1,5/2		ER.GBO	7H2
ENGB.OBO	OI	307	7/4,7/5		TGB.OBO	7H4
ENGB.ERO	OI	208	5/1,5/2		GB.ERO	7H5
F204LA0B	I	309	1/13		F204LAO	7A2
F204RA1A	I	IC	1/9		F204RA1A	7C0
F204R91	I	IC	1/9		F204R91	7C0
SS01SPO	I	206	5/5	202	OISPO	7A3
T204LA0B	I	209	1/11		T204LAO	7A4
T204RA0B	I	308	1/11		T204RAO	7A5
T204RA1	O	IC	7/20		T204RA1	7H5
T204RC0C	I	109	1/11		T204RCO	7A4
T204R90B	I	009	1/11		T204R90	7A4

SYMBOL NO. 7

MATCH ENABLE LOGIC

DESIG	EOPT LOC	CODE	ELEM IOENT	OPT
MTHENLGC	06-06	FA1034	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	I	202	7/9	202	ADRMTI1	3A6
CAT.MT1	I	102	7/11		OAMTI1	3A5
DR00A	I	302	4/1		ORIO	3A4
ELNOP10B	I	304	1/1		LNOPQ	3A2
ICP20B	I	IC	1/9		P20B	2E1
ISPANMTO	O	001	5/11		PMATO	3H3
SSAMEOA	I	003	5/14	202	AMEIO	3A3
SSOMEOA	I	213	5/10		OMEIO	3A3

SYMBOL NO. 8

ADRS MTCH AND OATA MTCH REGISTERS
(6: S PH AND FL)

OESIG	EOPT LOC	COOE	ELEM IOENT	OPT
MTBTPHPL	02-18	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		008			ADR.MT1	10H4
		305			OA.MT1	10H4
FP204L91	I	IC	4/5		F204L91	11F0
FP204RC1	I	IC	4/5		F204RC1	11F0
FP204R31	I	IC	4/5		F204R31	11E0
FP204R51	I	IC	4/5		F204R51	12F0
FP204R61	I	IC	4/5		F204R61	12E0
F204LA0A	I	216	1/13		F204LAO	11A5
ICDR80	I	IC	4/5		DRO	12B0
ICSARPH1	I	IC	4/5		SARB1	10A2
ICSARPL1	I	IC	4/5		SARA1	10A3
ICSDPHO	I	IC	4/5		TSD0B	10A4
ICSOPLO	I	IC	4/5		TSD0A	10A5
ICSORPH1	I	IC017	4/5		SDRB1	10A4
ICSORPL1	I	IC314	4/5		SDRA1	10A5
IGBPHA0	O	IC	4/5		AKBG10	11H2
IGBPHB0	O	IC	4/5		AIBG10	11H6
IGBPHC0	O	IC	4/5		DKBG10	12H2
IGBPHD0	O	IC	4/5		DIBG10	12H5
IGBPH1A	I	IC	4/5		GB.BD1A	11E0
IGBPH1B	I	IC	4/5		GB.BD1B	12E0
IGBPLA0	O	IC	4/5		AKAG10	11H3
IGBPLB0	O	IC	4/5		AIAG10	11H6
IGBPLC0	O	IC	4/5		DKAG10	12H2
IGBPLD0	O	IC	4/5		DIAG10	12H5
IGBPL1A	I	IC	4/5		GB.AD1A	11E0
IGBPL1B	I	IC	4/5		GB.AD1B	12E0
IRWSOI80	I	IC	4/5		R.WSOIO	10A4
MDA.BD0A	I	307	4/2		ER.AKDKO	12A2
MDGDDI0A	I	107	4/2		ERC.DIO	12A6
TP204L91	I	IC	4/5		T204L91	11A2
TP204R31	I	IC	4/5		T204R31	11A5
TP204R51	I	IC	4/5		T204R51	12C0
TP204R61	I	IC	4/5		T204R61	12B0
T204LA0A	I	308	1/11		T204LAO	11A5
T204RC0B	I	209	1/11		T204RCO	11A2

SYMBOL NO. 9

ADRS MTCH REGISTER
(BITS 19 AND 17)

OESIG	EOPT LOC	CODE	ELEM IOENT	OPT
MTBT1917	02-20	FA1030	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	108	7/10,7/11 7/12,7/13 7/14,7/15 7/16,7/17 7/18 4/15,7/7	202	ADR.MT1	5G8
F204LA0B	I	211	1/13		F204LAO	5A0
F204R30C	I	311	1/13		F204R30	5A0
F9204L91	I	IC	4/6		F204L91	5A2
F9204RC1	I	IC	4/6		F204RC1	5A2
F9204R31	O	IC	5/5		F204R31	5H0
ICSAR171	I	IC	4/6		SAR.A1	5A5
ICSAR191	I	IC	4/6		SAR.B1	5A5
IGB17A0	O	IC	4/6		TIGBAA0	5H2
IGB171A	I	IC	4/6		GB.A01	5A2
IGB19A0	O	IC	4/6		TIGBBA0	5H1
IGB191A	I	IC	4/6		GB.B01	5A1
MDA.BD0B	I	107	4/2		ER.SAAKO	5A4
T204LA0B	I	318	1/11		T204LAO	5A1
T204RC0C	I	218	1/11		T204RCO	5A3
T9204L91	I	IC	4/6		T204L91	5A2
T9204R31	I	IC	4/6		T204R31	5A0

PART OF FS 7
SYMBOL(S) 5 6 7 8 9

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	5A

BELL LABORATORIES

SD-1C900-01

B7CB

PRINTED IN U. S. A.

06/10/77

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL NO. 10

ADRS MTCH REGISTER
(BITS 18 AND 16)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1816	02-19	FA1030	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	108	7/9	202	ADR.MT1	5G8
F204LA0B	I	211	1/13		F204LA0	5A0
F204R30C	I	311	1/13		F204R30	5A0
F8204L91	I	IC	4/7		F204L91	5A2
F8204RC1	I	IC	4/7		F204RC1	5A2
F8204R31	O	IC	5/6		F204R31	5H0
ICSAR161	I	IC	4/7		SAR.A1	5A5
ICSAR181	I	IC	4/7		SAR.B1	5A5
IGB16A0	O	IC	4/7		TIGBAA0	5H2
IGB161A	I	IC	4/7		GB.A01	5A2
IGB18A0	O	IC	4/7		TIGBBA0	5H1
IGB181A	I	IC	4/7		GB.B01	5A1
MDA.B00B	I	107	4/2		ER.SAAK0	5A4
T204LA0B	I	318	1/11		T204LA0	5A1
T204RC0C	I	218	1/11		T204RC0	5A3
T8204L91	I	IC	4/7		T204L91	5A2
T8204R31	I	IC	4/7		T204R31	5A0

SYMBOL NO. 11

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1507	02-17	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/12,7/13 7/14,7/15 7/16,7/17 7/18 4/14,7/7		DA.MT1	10H6
F204LA0A	I	216	1/13		F204LA0	11A5
F7204L91	I	IC	4/8		F204L91	11F0
F7204RC1	I	IC	4/8		F204RC1	11F0
F7204R31	I	IC	4/8		F204R31	11E0
F7204R51	I	IC	4/8		F204R51	12F0
F7204R61	I	IC	4/8		F204R61	12E0
ICDR70	I	IC	4/8		DR0	12B0
ICSAR071	I	IC	4/8		SARA1	10A3
ICSAR151	I	IC	4/8		SARB1	10A2
ICSDR071	I	IC314	4/8		SDRA1	10A5
ICSDR151	I	IC017	4/8		SDRB1	10A4
ICSD070	I	IC	4/8		TSD0A	10A5
ICSD150	I	IC	4/8		TSD0B	10A4
IGB07A0	O	IC	4/8		AKAG10	11H3
IGB07B0	O	IC	4/8		AIAG10	11H6
IGB07C0	O	IC	4/8		DKAG10	12H2
IGB07D0	O	IC	4/8		OIAG10	12H5
IGB071A	I	IC	4/8		GB.AD1A	11E0
IGB071B	I	IC	4/8		GB.AD1B	12E0
IGB15A0	O	IC	4/8		AKBG10	11H2
IGB15B0	O	IC	4/8		AIBG10	11H6
IGB15C0	O	IC	4/8		DKBG10	12H2

SYMBOL NO. 11 (CONT)

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 15 AND 07)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1507	02-17	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IGB1500	O	IC	4/8		OIBG10	12H5
IGB151A	I	IC	4/8		GB.BD1A	11E0
IGB151B	I	IC	4/8		GB.BD1B	12E0
IRWS0170	I	IC	4/8		R.WS010	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDD10A	I	107	4/2		ERC.010	12A6
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2
T7204L91	I	IC	4/8		T204L91	11A2
T7204R31	I	IC	4/8		T204R31	11A5
T7204R51	I	IC	4/8		T204R51	12C0
T7204R61	I	IC	4/8		T204R61	12B0

SYMBOL NO. 12

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1406	02-16	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F204LA0A	I	216	1/13		F204LA0	11A5
F6204L91	I	IC	4/9		F204L91	11F0
F6204RC1	I	IC	4/9		F204RC1	11F0
F6204R31	I	IC	4/9		F204R31	11E0
F6204R51	I	IC	4/9		F204R51	12F0
F6204R61	I	IC	4/9		F204R61	12E0
ICDR60	I	IC	4/9		DR0	12B0
ICSAR061	I	IC	4/9		SARA1	10A3
ICSAR141	I	IC	4/9		SARB1	10A2
ICSDR061	I	IC314	4/9		SDRA1	10A5
ICSDR141	I	IC017	4/9		SDRB1	10A4
ICSD060	I	IC	4/9		TSD0A	10A5
ICSD140	I	IC	4/9		TSD0B	10A4
IGB06A0	O	IC	4/9		AKAG10	11H3
IGB06B0	O	IC	4/9		AIAG10	11H6
IGB06C0	O	IC	4/9		DKAG10	12H2
IGB06D0	O	IC	4/9		OIAG10	12H5
IGB061A	I	IC	4/9		GB.AD1A	11E0
IGB061B	I	IC	4/9		GB.AD1B	12E0
IGB14A0	O	IC	4/9		AKBG10	11H2
IGB14B0	O	IC	4/9		AIBG10	11H6
IGB14C0	O	IC	4/9		DKBG10	12H2
IGB14D0	O	IC	4/9		OIBG10	12H5
IGB141A	I	IC	4/9		GB.BD1A	11E0
IGB141B	I	IC	4/9		GB.BD1B	12E0
IRWS0160	I	IC	4/9		R.WS010	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDD10A	I	107	4/2		ERC.D10	12A6
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2
T6204L91	I	IC	4/9		T204L91	11A2

SYMBOL NO. 12 (CONT)

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 14 AND 06)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1406	02-16	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T6204R31	I	IC	4/9		T204R31	11A5
T6204R51	I	IC	4/9		T204R51	12C0
T6204R61	I	IC	4/9		T204R61	12B0

SYMBOL NO. 13

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 13 AND 05)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1305	02-13	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F204LA0A	I	216	1/13		F204LA0	11A5
F5204L91	I	IC	4/10		F204L91	11F0
F5204RC1	I	IC	4/10		F204RC1	11F0
F5204R31	I	IC	4/10		F204R31	11E0
F5204R51	I	IC	4/10		F204R51	12F0
F5204R61	I	IC	4/10		F204R61	12E0
ICDR50	I	IC	4/10		DR0	12B0
ICSAR051	I	IC	4/10		SARA1	10A3
ICSAR131	I	IC	4/10		SARB1	10A2
ICSDR051	I	IC314	4/10		SDRA1	10A5
ICSDR131	I	IC017	4/10		SDRB1	10A4
ICSD050	I	IC	4/10		TSD0A	10A5
ICSD130	I	IC	4/10		TSD0B	10A4
IGB05A0	O	IC	4/10		AKAG10	11H3
IGB05B0	O	IC	4/10		AIAG10	11H6
IGB05C0	O	IC	4/10		DKAG10	12H2
IGB05D0	O	IC	4/10		OIAG10	12H5
IGB051A	I	IC	4/10		GB.AD1A	11E0
IGB051B	I	IC	4/10		GB.AD1B	12E0
IGB13A0	O	IC	4/10		AKBG10	11H2
IGB13B0	O	IC	4/10		AIBG10	11H6
IGB13C0	O	IC	4/10		DKBG10	12H2
IGB13D0	O	IC	4/10		OIBG10	12H5
IGB131A	I	IC	4/10		GB.BD1A	11E0
IGB131B	I	IC	4/10		GB.BD1B	12E0
IRWS0150	I	IC	4/10		R.WS010	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDD10A	I	107	4/2		ERC.010	12A6
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2
T5204L91	I	IC	4/10		T204L91	11A2
T5204R31	I	IC	4/10		T204R31	11A5
T5204R51	I	IC	4/10		T204R51	12C0
T5204R61	I	IC	4/10		T204R61	12B0

SYMBOL NO. 14

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 12 AND 04)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1204	02-12	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F204LA0A	I	216	1/13		F204LA0	11A5
F4204L91	I	IC	4/11		F204L91	11F0
F4204RC1	I	IC	4/11		F204RC1	11F0
F4204R31	I	IC	4/11		F204R31	11E0
F4204R51	I	IC	4/11		F204R51	12F0
F4204R61	I	IC	4/11		F204R61	12E0
ICDR40	I	IC	4/11		DR0	12B0
ICSAR041	I	IC	4/11		SARA1	10A3
ICSAR121	I	IC	4/11		SARB1	10A2
ICSDR041	I	IC314	4/11		SDRA1	10A5
ICSDR121	I	IC017	4/11		SDRB1	10A4
ICSD040	I	IC	4/11		TSD0A	10A5
ICSD120	I	IC	4/11		TSD0B	10A4
IGB04A0	O	IC	4/11		AKAG10	11H3
IGB04B0	O	IC	4/11		AIAG10	11H6
IGB04C0	O	IC	4/11		DKAG10	12H2
IGB04D0	O	IC	4/11		OIAG10	12H5
IGB041A	I	IC	4/11		GB.AD1A	11E0
IGB041B	I	IC	4/11		GB.AD1B	12E0
IGB12A0	O	IC	4/11		AKBG10	11H2
IGB12B0	O	IC	4/11		AIBG10	11H4
IGB12C0	O	IC	4/11		DKBG10	12H2
IGB12D0	O	IC	4/11		OIBG10	12H5
IGB121A	I	IC	4/11		GB.BD1A	11E0
IGB121B	I	IC	4/11		GB.BD1B	12E0
IRWS0140	I	IC	4/11		R.WS010	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDD10A	I	107	4/2		ERC.010	12A6
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2
T4204L91	I	IC	4/11		T204L91	11A2
T4204R31	I	IC	4/11		T204R31	11A5
T4204R51	I	IC	4/11		T204R51	12C0
T4204R61	I	IC	4/11		T204R61	12B0

PART OF FS 7
SYMBOL(S) 10 11 12 13 14

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01		B7CC

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PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL NO. 15

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 11 AND 03)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1103	02-11	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F204LA0A	I	216	1/13		F204LA0	11A5
F3204L91	I	IC	4/12		F204L91	11F0
F3204RC1	I	IC	4/12		F204RC1	11F0
F3204R31	I	IC	4/12		F204R31	11E0
F3204R51	I	IC	4/12		F204R51	12F0
F3204R61	I	IC	4/12		F204R61	12E0
ICDR30	I	IC	4/12		DR0	12B0
ICSAR031	I	IC	4/12		SARA1	10A3
ICSAR111	I	IC	4/12		SARB1	10A2
ICSDR031	I	IC314	4/12		SDRA1	10A5
ICSDR111	I	IC017	4/12		SDRB1	10A4
ICSD030	I	IC	4/12		TSD0A	10A5
ICSD110	I	IC	4/12		TSD0B	10A4
IGB03A0	0	IC	4/12		AKAG10	11H3
IGB03B0	0	IC	4/12		AIAG10	11H6
IGB03C0	0	IC	4/12		DKAG10	12H2
IGB03D0	0	IC	4/12		DIAG10	12H5
IGB031A	I	IC	4/12		GB.AD1A	11E0
IGB031B	I	IC	4/12		GB.AD1B	12E0
IGB11A0	0	IC	4/12		AKBG10	11H2
IGB11B0	0	IC	4/12		AIBG10	11H6
IGB11C0	0	IC	4/12		DKBG10	12H2
IGB11D0	0	IC	4/12		DIBG10	12H5
IGB111A	I	IC	4/12		GB.BD1A	11E0
IGB111B	I	IC	4/12		GB.BD1B	12E0
IRWS0I30	I	IC	4/12		R.WS0I0	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDDI0A	I	107	4/2		ERC.DI0	12A6
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2
T3204L91	I	IC	4/12		T204L91	11A2
T3204R31	I	IC	4/12		T204R31	11A5
T3204R51	I	IC	4/12		T204R51	12C0
T3204R61	I	IC	4/12		T204R61	12B0

SYMBOL NO. 16

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1002	02-10	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F204LA0A	I	216	1/13		F204LA0	11A5
F2204L91	I	IC	4/13		F204L91	11F0
F2204RC1	I	IC	4/13		F204RC1	11F0
F2204R31	I	IC	4/13		F204R31	11E0
F2204R51	I	IC	4/13		F204R51	12F0
F2204R61	I	IC	4/13		F204R61	12E0
ICDR20	I	IC	4/13		DR0	12B0

SYMBOL NO. 16 (CONT)

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 10 AND 02)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT1002	02-10	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ICSAR021	I	IC	4/13		SARA1	10A3
ICSAR101	I	IC	4/13		SARB1	10A2
ICSDR021	I	IC314	4/13		SDRA1	10A5
ICSDR101	I	IC017	4/13		SDRB1	10A4
ICSD020	I	IC	4/13		TSD0A	10A5
ICSD100	I	IC	4/13		TSD0B	10A4
IGB02A0	0	IC	4/13		AKAG10	11H3
IGB02B0	0	IC	4/13		AIAG10	11H6
IGB02C0	0	IC	4/13		DKAG10	12H2
IGB02D0	0	IC	4/13		DIAG10	12H5
IGB021A	I	IC	4/13		GB.AD1A	11E0
IGB021B	I	IC	4/13		GB.AD1B	12E0
IGB10A0	0	IC	4/13		AKBG10	11H2
IGB10B0	0	IC	4/13		AIBG10	11H6
IGB10C0	0	IC	4/13		DKBG10	12H2
IGB10D0	0	IC	4/13		DIBG10	12H5
IGB101A	I	IC	4/13		GB.BD1A	11E0
IGB101B	I	IC	4/13		GB.BD1B	12E0
IRWS0I20	I	IC	4/13		R.WS0I0	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDDI0A	I	107	4/2		ERC.DI0	12A6
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2
T2204L91	I	IC	4/13		T204L91	11A2
T2204R31	I	IC	4/13		T204R31	11A5
T2204R51	I	IC	4/13		T204R51	12C0
T2204R61	I	IC	4/13		T204R61	12B0

SYMBOL NO. 17

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT0901	02-09	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F1204L91	I	IC	4/14		F204L91	11F0
F1204RC1	I	IC	4/14		F204RC1	11F0
F1204R31	I	IC	4/14		F204R31	11E0
F1204R51	I	IC	4/14		F204R51	12F0
F1204R61	I	IC	4/14		F204R61	12E0
F204LA0A	I	216	1/13		F204LA0	11A5
ICDR10	I	IC	4/14		DR0	12B0
ICSAR011	I	IC	4/14		SARA1	10A3
ICSAR091	I	IC	4/14		SARB1	10A2
ICSDR011	I	IC314	4/14		SDRA1	10A5
ICSDR091	I	IC017	4/14		SDRB1	10A4
ICSD010	I	IC	4/14		TSD0A	10A5
ICSD090	I	IC	4/14		TSD0B	10A4
IGB01A0	0	IC	4/14		AKAG10	11H3
IGB01B0	0	IC	4/14		AIAG10	11H6
IGB01C0	0	IC	4/14		DKAG10	12H2

SYMBOL NO. 17 (CONT)

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 09 AND 01)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT0901	02-09	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IGB01D0	0	IC	4/14		DIAG10	12H5
IGB011A	I	IC	4/14		GB.AD1A	11E0
IGB011B	I	IC	4/14		GB.AD1B	12E0
IGB09A0	0	IC	4/14		AKBG10	11H2
IGB09B0	0	IC	4/14		AIBG10	11H6
IGB09C0	0	IC	4/14		DKBG10	12H2
IGB09D0	0	IC	4/14		DIBG10	12H5
IGB091A	I	IC	4/14		GB.BD1A	11E0
IGB091B	I	IC	4/14		GB.BD1B	12E0
IRWS0I10	I	IC	4/14		R.WS0I0	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDDI0A	I	107	4/2		ERC.DI0	12A6
T1204L91	I	IC	4/14		T204L91	11A2
T1204R31	I	IC	4/14		T204R31	11A5
T1204R51	I	IC	4/14		T204R51	12C0
T1204R61	I	IC	4/14		T204R61	12B0
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2

SYMBOL NO. 18

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 08 AND 00)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT0800	02-08	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADR.MT1	OT	008	7/9	202	ADR.MT1	10H4
DAT.MT1	OT	305	7/11		DA.MT1	10H6
F0204L91	I	IC	4/15		F204L91	11F0
F0204RC1	I	IC	4/15		F204RC1	11F0
F0204R31	I	IC	4/15		F204R31	11E0
F0204R51	I	IC	4/15		F204R51	12F0
F0204R61	I	IC	4/15		F204R61	12E0
F204LA0A	I	216	1/13		F204LA0	11A5
ICDR00	I	IC	4/15		DR0	12B0
ICSAR001	I	IC	4/15		SARA1	10A3
ICSAR081	I	IC	4/15		SARB1	10A2
ICSDR001	I	IC314	4/15		SDRA1	10A5
ICSDR081	I	IC017	4/15		SDRB1	10A4
ICSD000	I	IC	4/15		TSD0A	10A5
ICSD080	I	IC	4/15		TSD0B	10A4
IGB00A0	0	IC	4/15		AKAG10	11H3
IGB00B0	0	IC	4/15		AIAG10	11H6
IGB00C0	0	IC	4/15		DKAG10	12H2
IGB00D0	0	IC	4/15		DIAG10	12H5
IGB001A	I	IC	4/15		GB.AD1A	11E0
IGB001B	I	IC	4/15		GB.AD1B	12E0
IGB08A0	0	IC	4/15		AKBG10	11H2
IGB08B0	0	IC	4/15		AIBG10	11H6
IGB08C0	0	IC	4/15		DKBG10	12H2
IGB08D0	0	IC	4/15		DIBG10	12H5
IGB081A	I	IC	4/15		GB.BD1A	11E0
IGB081B	I	IC	4/15		GB.BD1B	12E0

SYMBOL NO. 18 (CONT)

ADRS MTCH AND DATA MTCH REGISTERS
(BITS 08 AND 00)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MTBT0800	02-08	FA1024	B	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IRWS0I00	I	IC	4/15		R.WS0I0	10A4
MDA.BD0A	I	307	4/2		ER.AKDK0	12A2
MDGDDI0A	I	107	4/2		ERC.DI0	12A6
T0204L91	I	IC	4/15		T204L91	11A2
T0204R31	I	IC	4/15		T204R31	11A5
T0204R51	I	IC	4/15		T204R51	12C0
T0204R61	I	IC	4/15		T204R61	12B0
T204LA0A	I	308	1/11		T204LA0	11A5
T204RC0B	I	209	1/11		T204RC0	11A2

PART OF FS 7
SYMBOL(S) 15 16 17 18

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B7CD

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PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

SYMBOL NO. 19

MRF AND FREEZE LOGIC

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MRFLOGIC	02-25	FA1032	A	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		114			ST.FRZA0	3A7
		313			STP.SWI0	3A2
		314			ST.FRZB0	3A6
ER.FAT0	I	208	5/2		ERS0	2A5
ES.STP0	OI	010	5/8		TST.STP0	3H2
ESWITCH0	O	015	9/1		SWITCH0	3H3
FREZ0	O	112	1/2,1/3 6/3		FREEZA0	3H7
HI.MRF0	I	011	5/1		HI.MRFI0	2A4
ICP20	I	IC	6/4		P20	3H4
MANL1	O	303	TO CTLPNL CKT	202	MANL1	2H8
MCH.MRF0	I	311	9/4		MCHMRFI0	2A2
MCLOMAR0	I	214	9/4		ST.FRZI0	3A7
MCSTRT0	I	014	9/4		MSTRTI0	3A8
MD.IMTC0	I	113	1/12		CLMCHMR0	2A1
MD.SBTC0	OT	002	1/12		SET.BTC0	3H6
MD.SSTP0	I	305	1/12		ST.STPI0	3A1
MD.STSW0	I	108	1/12		ER.PTSI0	2A5
MD.ZMIN0	OT	004	1/14		STSTP0I0	3H3
	OT	302	1/14		CLR.INT0	3H6
MD.ZMS0	OT	102	1/14		CLR.MSR0	3H6
MDERCRT0	OT	101	1/5		SET.BHC0	3H5
MDIOMCH0	OT	301	1/14		INTMCH0A	2H2
MDIOSW00	OT	219	1/12		INTMCH0B	3H5
MDMRFCC0	I	213	1/14		COM.RSI0	2A3
MRFBTSE0	O	203	5/13,7/20		CLR.SEN0	2H3
MRFCSTP0	O	005	9/4 5/8		CLR.STP0	2H2
MRFSMAR0	O	202	1/2,1/6 1/8		ST.MARK0	3H7
MRFSTP30	O	107	9/4 8/3,8/5		SET.P30	2H4
PT.MRF0	I	111	8/4		PT.MRFI0	2A3
P31	I	211	8/3		P31	2A7
SSBHC0A	I	017	5/13	202	BHCI0	2A4
SSLON0A	I	316	5/13		LONI0	2A6
SSMAN0A	I	308	5/12	202	MANL0	2A8
SSP.MRF0	I	012	7/21		SSPMRFI0	2A3
SSSTP0A	I	310	5/8		STOPI0	3A8
STOPL1	O	210	TO CTLPNL CKT	202	STOPB1	3H9
STP.FRZ0	OT	212	5/4		TFRZSTP0	3H8
3T054C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054C	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 20

DISABLE AND ENABLE CIRCUIT,
POWER MRF

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
DISENBP0	06-06	FA1034	F	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ES.SS150	O	013	5/7		DISFF0C	9H0
FZ04L31C	I	IC	1/9		FZ04L31C	8A2
FZ04RA1A	I	IC	1/9		FZ04RA1A	8A3
FZ04R91	I	IC	1/9		FZ04R91	8A2
ICC0A	I	IC	7/1		CC0A	9A6
ICMANA1	I	IC	7/1		MANA1	9A6
ICPBON0	O	IC	7/1,7/22		PBON0	9G7
ICTMK1	I	IC	7/1		TMK1	9A7
IDISFF0B	O	IC	7/1		DISFF0B	9H1
LKOFF1	O	315	TO CONN CKT		LNOF1	9H7
LOFF0A	OI	103	10/2,10/6 10/10		DIS.100A	9H5
LOFF0B	OI	203	TO CONN CKT		DIS.100B	9H6
LOFF0C	OI	100	TO CONN CKT		DIS.100C	9H6
MCDISA0	I	305	9/4		DISA0	8A5
MCDISB0	I	313	9/4		DISB0	8A5
MCHGB050	OT	207	5/2	202	SDIS0	9H4
MCHGB060	OT	007	5/2	202	SEN0	9H3
MCHGB070	OT	107	5/2	202	DISFF0A	9H2
MCMB.MC0	I	113	9/4		G.DISBT0	8A6
MD.SDIS0	OT	312	1/12		SET.DIS0	9G9
	I	105	1/12		ST.DISI0	8A2
MD.ZPT0	OT	212	1/14		CLR.PT0	9G8
MRFBTSE0	I	211	7/19		MRFI0	8A4
MS000	OI	300	5/14		LOFF1	9H5
PCISC210	O	012	5/7,5/8		CLR.ISC0	9G9
PCL.CC0	O	112	5/10		CLR.PC0	9G8
PWROFF0	I	015	TO CONN CKT		PBONI0	9A8
SSLOF0A	I	014	5/14	202	LOFF0	9A5
TZ04L30B	I	006	1/11		TZ04L30	8A2
TZ04RA1	I	IC	7/6		TZ04RA1	8A2

SYMBOL NO. 21

SSP TRANSFORMERS

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SSPTRNSF	02-26	FC202	B	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FORCEN	I	210	TO CONN CKT	P/FORCEP	FORCEN	2A5
FORCEP	I	310	TO CONN CKT	P/FORCEN	FORCEP	2A5
INTEP	I	017	TO CONN CKT		INTEP	2A7
INTFP	I	018	TO CONN CKT		INTFP	2A7
INTGP	I	001	TO CONN CKT		INTGP	2A8
INTHP	I	002	TO CONN CKT		INTHP	2A8
INTJP	I	003	TO CONN CKT		INTJP	2A8
INTKP	I	201	TO CONN CKT		INTKP	2A9
ISF0	O	009	TO CONN CKT		ST.ISF0	2G7
ISG0	O	111	TO CONN CKT		ST.ISG0	2G8
ISH0	O	011	TO CONN CKT		ST.ISH0	2G8
ISJ0	O	110	TO CONN CKT		ST.ISJ0	2G8
ISK0	O	212	TO CONN CKT		ST.ISK0	2G9
ISTTYE0	OT	012			ST.ISA0	2G6
	I		5/12			
	OT	112	7/21		ST.ISB0	2G6

SYMBOL NO. 21 (CONT)

SSP TRANSFORMERS

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SSPTRNSF	02-26	FC202	B	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ISTTY00	OT	010			ST.ISC0	2G7
	I		5/11			
ISTTY00	OT	312	7/21		ST.ISD0	2G7
ISUTIL0	O	109	5/13		ST.ISE0	2G7
ITDCEBP	I	014	TO CONN CKT		INTBP	2A6
ITDCODP	I	016	TO CONN CKT		INTDP	2A7
ITTYEAP	I	013	TO CONN CKT		INTAP	2A6
ITTYOCP	I	015	TO CONN CKT		INTCP	2A6
MRFP	I	202	TO CONN CKT		MRFP	2A9
SSP.MRF0	O	213	7/19		MRF0	2G9
SSPF0F0	O	211	7/22		FOR.LOF0	2G5
SSPF0N0	O	311	7/22		FOR.LON0	2G5
3VG0Z26B	I	101	9/1		INTGN	2A8
	I	102	9/1		INTHN	2A8
	I	103	9/1		INTJN	2A8
	I	301	9/1		INTKN	2A9
	I	302	9/1		MRFN	2A9
3VG0Z26T	I	113	9/1		INTAN	2A6
	I	114	9/1		INTBN	2A6
	I	115	9/1		INTCN	2A7
	I	116	9/1		INTDN	2A7
	I	117	9/1		INTEN	2A7
	I	118	9/1		INTFN	2A8

SYMBOL NO. 22

SSP INTERFACE

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SSPINTRF	06-06	FA1034	C	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ES.LOF0	O	303	5/14		TST.LOF0	4H1
ES.LON0	O	004	5/13		TST.LON0	4H1
EZ.LOF0	OT	116	5/13		CLR.LOF0	4H6
EZ.LON0	O	215	5/13		CLR.LON0	4H5
ICPBON0	I	IC	7/20		PBON0	4E6
IST25.00	I	101	8/4		I25.00	4A4
SSPF0F0	I	301	7/21		FORCENI0	4A1
SSPF0N0	I	002	7/21		FORCEPI0	4A1

PART OF FS 7
SYMBOL(S) 19 20 21 22

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	5A

BELL LABORATORIES
SD-1C900-01
B7CE
PRINTED IN U. S. A.
06/10/77

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 1

FUNCTION PARTITIONING OF CONSOLE FUNCTIONS

CIRCUIT OPERATION

FS 7 PROVIDES FOUR MAJOR FUNCTIONS:

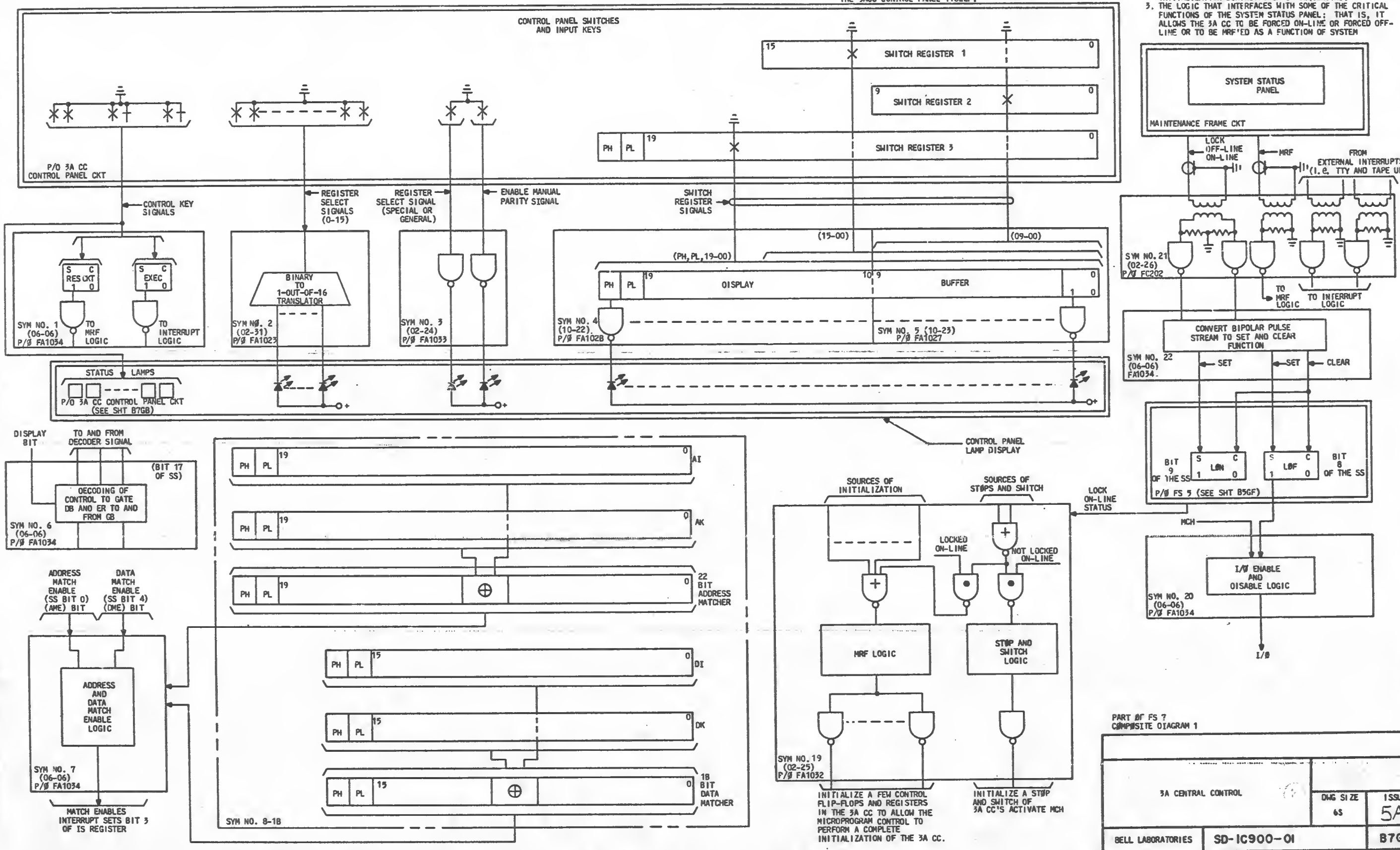
1. THE LOGIC INTERFACES TO RECEIVE CONTROL FROM AND SEND STATUS INFORMATION TO THE 3A CC CONTROL PANEL.
2. THE LOGIC NEEDED TO HARDWARE INITIALIZE THE 3A CC. THIS INCLUDES THE LOGIC NECESSARY TO ENABLE POWER TO BE TURNED ON OR TURNED OFF AND THE APPROPRIATE INITIALIZATION DURING POWER-UP SEQUENCING.
3. THE LOGIC THAT INTERFACES WITH SOME OF THE CRITICAL FUNCTIONS OF THE SYSTEM STATUS PANEL: THAT IS, IT ALLOWS THE 3A CC TO BE FORCED ON-LINE OR FORCED OFF-LINE OR TO BE MRF'ED AS A FUNCTION OF SYSTEM

CIRCUIT OPERATION (CONT)

STATUS PANEL INPUTS.

4. INTERFACE TRANSFORMERS THAT BUFFER INTERRUPTS ENTERING FROM EXTERNAL INPUTS INTO THE 3ACC.

COMPOSITE DIAGRAM 1 INDICATES THE FUNCTIONAL PARTITIONING OF EACH OF THESE FUNCTIONS WITH FS 7. AS CAN BE SEEN, THIS LOGIC IS DISPERSED THROUGH A NUMBER OF CIRCUIT PACKS AS WELL AS THE 3ACC CONTROL PANEL ITSELF.


CONTROL PANEL SWITCHES AND INPUT KEYS
P/O 3A CC CONTROL PANEL CKT
15
SWITCH REGISTER 1
0
9
SWITCH REGISTER 2
0
PH
PL
19
SWITCH REGISTER 3
0
CONTROL KEY SIGNALS
REGISTER SELECT SIGNALS (0-15)
REGISTER SELECT SIGNAL (SPECIAL OR GENERAL)
ENABLE MANUAL PARITY SIGNAL
SWITCH REGISTER SIGNALS
S C RES CKT 1 0
S C EXEC 1 0
TO MRF LOGIC
TO INTERRUPT LOGIC
SYM NO. 1 (06-06) P/Ø FA1034
BINARY TO 1-OUT-OF-16 TRANSLATOR
SYM NØ. 2 (02-31) P/Ø FA1023
SYM NO. 3 (02-24) P/Ø FA1033
(15-00)
(09-00)
(PH,PL,19-00)
PH
PL
19
DISPLAY
10
9
BUFFER
0
1
0
SYM NO. 4 (10-22) P/Ø FA1028
SYM NO. 5 (10-23) P/Ø FA1027
STATUS LAMPS
P/O 3A CC CONTROL PANEL CKT (SEE SHT B7GB)
+
CONTROL PANEL LAMP DISPLAY
SYSTEM STATUS PANEL
MAINTENANCE FRAME CKT
LOCK OFF-LINE ON-LINE
MRF
FROM EXTERNAL INTERRUPTS (I.E. TTY AND TAPE UNIT)
SYM NO. 21 (02-26) P/Ø FC202
TO MRF LOGIC
TO INTERRUPT LOGIC
CONVERT BIPOLAR PULSE STREAM TO SET AND CLEAR FUNCTION
SYM NO. 22 (06-06) FA1034
SET
SET
CLEAR
BIT 9 OF THE SS
S C LØN 1 0
S C LØF 1 0
BIT 8 OF THE SS
P/Ø FS 5 (SEE SHT B5GF)
LOCK ON-LINE STATUS
MCH
I/Ø ENABLE AND DISABLE LOGIC
SYM NO. 20 (06-06) P/Ø FA1034
I/Ø
DISPLAY BIT
TO AND FROM DECODER SIGNAL
(BIT 17 OF SS)
DECODING OF CONTROL TO GATE DB AND ER TO AND FROM GB
SYM NO. 6 (06-06) P/Ø FA1034
PH PL 19 0 AI
PH PL 19 0 AK
PH PL 19 ⊕ 0
22 BIT ADDRESS MATCHER
ADDRESS MATCH ENABLE (SS BIT 0) (AME) BIT
DATA MATCH ENABLE (SS BIT 4) (DME) BIT
ADDRESS AND DATA MATCH ENABLE LOGIC
SYM NO. 7 (06-06) P/Ø FA1034
MATCH ENABLES INTERRUPT SETS BIT 3 OF IS REGISTER
PH PL 15 0 DI
PH PL 15 0 DK
PH PL 15 ⊕ 0
18 BIT DATA MATCHER
SYM NO. 8-18
SOURCES OF INITIALIZATION
SOURCES OF STØPS AND SWITCH
+
LOCKED ON-LINE
NOT LOCKED ON-LINE
MRF LOGIC
STØP AND SWITCH LOGIC
SYM NO. 19 (02-25) P/Ø FA1032
INITIALIZE A FEW CONTROL FLIP-FLOPS AND REGISTERS IN THE 3A CC TO ALLOW THE MICROPROGRAM CONTROL TO PERFORM A COMPLETE INITIALIZATION OF THE 3A CC.
INITIALIZE A STØP AND SWITCH OF 3A CC'S ACTIVATE MCH

PART ØF FS 7
CØMPØSITE DIAGRAM 1

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	5A

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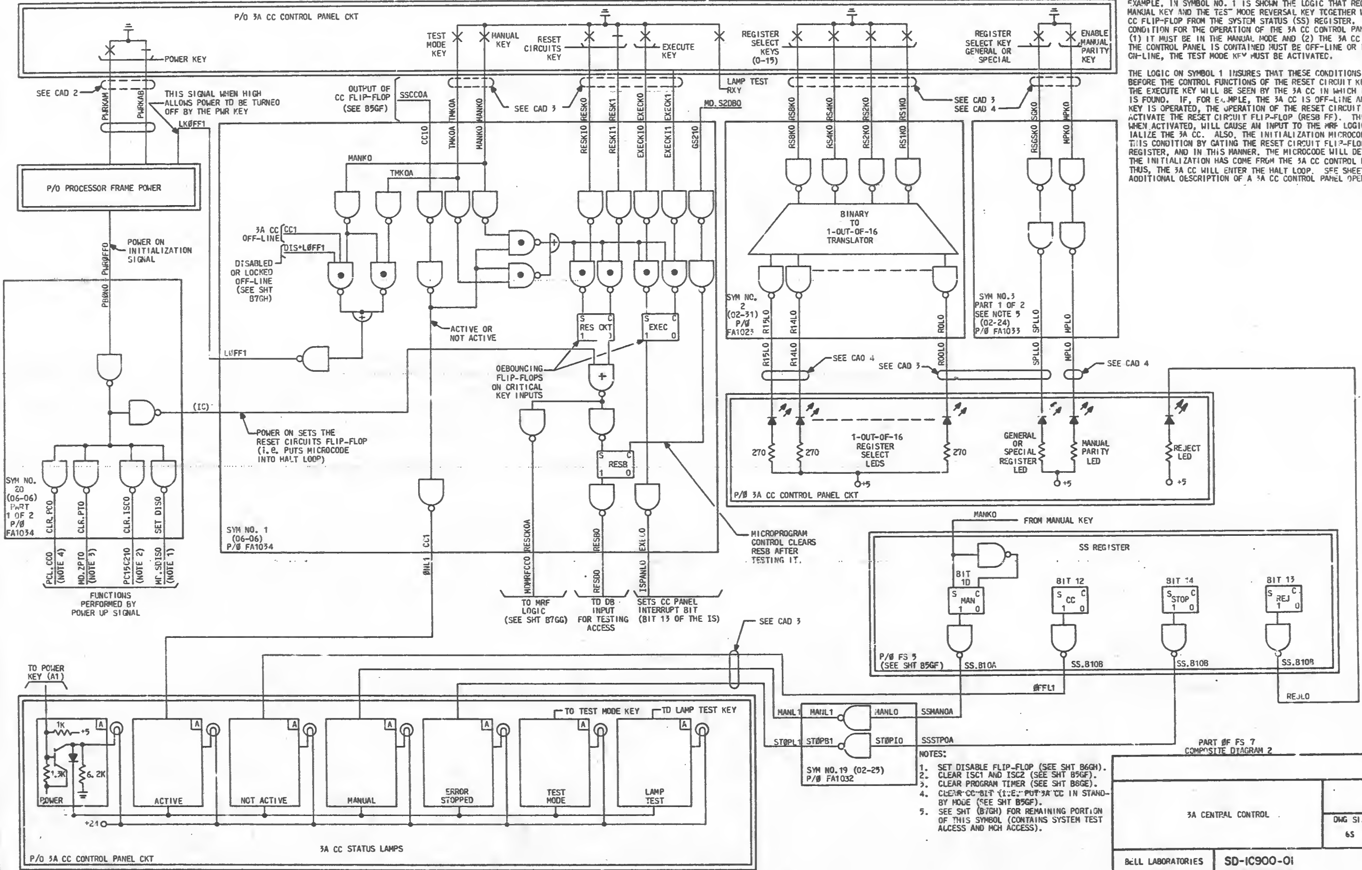
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 2

P/Ø CONTROL PANEL INTERFACE LOGIC



CIRCUIT OPERATION

COMPOSITE DIAGRAM 2 SHOWS THE CONTROL PORTION OF THE 3A CC PANEL FUNCTIONS. AS INDICATED, THERE ARE A NUMBER OF CONTROL KEYS THAT CAN BE OPERATED ON THE 3A CC CONTROL PANEL ITSELF. THESE KEYS, IN TURN, ARE INPUTTED TO COMBINATIONAL LOGIC THAT DETERMINES WHETHER A CONTROL FUNCTION FROM THE 3A CC CONTROL PANEL CAN BE PERFORMED AND/OR MONITORED BY THE 3A CC. FOR EXAMPLE, IN SYMBOL NO. 1 IS SHOWN THE LOGIC THAT RECEIVES THE MANUAL KEY AND THE TEST MODE REVERSAL KEY TOGETHER WITH THE CC FLIP-FLOP FROM THE SYSTEM STATUS (SS) REGISTER. A NECESSARY CONDITION FOR THE OPERATION OF THE 3A CC CONTROL PANEL IS: (1) IT MUST BE IN THE MANUAL MODE AND (2) THE 3A CC IN WHICH THE CONTROL PANEL IS CONTAINED MUST BE OFF-LINE OR IF IT IS ON-LINE, THE TEST MODE KEY MUST BE ACTIVATED.

THE LOGIC ON SYMBOL 1 INSURES THAT THESE CONDITIONS ARE MET BEFORE THE CONTROL FUNCTIONS OF THE RESET CIRCUIT KEY OF THE EXECUTE KEY WILL BE SEEN BY THE 3A CC IN WHICH THIS LOGIC IS FOUND. IF, FOR EXAMPLE, THE 3A CC IS OFF-LINE AND THE MANUAL KEY IS OPERATED, THE OPERATION OF THE RESET CIRCUIT KEY WILL ACTIVATE THE RESET CIRCUIT FLIP-FLOP (RESB FF). THIS SIGNAL, WHEN ACTIVATED, WILL CAUSE AN INPUT TO THE MRF LOGIC TO INITIALIZE THE 3A CC. ALSO, THE INITIALIZATION MICROCODE WILL TEST THIS CONDITION BY GATING THE RESET CIRCUIT FLIP-FLOP TO THE DB REGISTER, AND IN THIS MANNER, THE MICROCODE WILL DETERMINE THAT THE INITIALIZATION HAS COME FROM THE 3A CC CONTROL PANEL AND THUS, THE 3A CC WILL ENTER THE HALT LOOP. SEE SHEET B7GD FOR ADDITIONAL DESCRIPTION OF A 3A CC CONTROL PANEL OPERATION.

NOTES:

1. SET DISABLE FLIP-FLOP (SEE SHT B6GH).
2. CLEAR ISC1 AND ISC2 (SEE SHT B5GF).
3. CLEAR PROGRAM TIMER (SEE SHT B6GE).
4. CLEAR CC BIT (I.E. PUT 3A CC IN STANDBY MODE (SEE SHT B5GF).
5. SEE SHT (B7GH) FOR REMAINING PORTION OF THIS SYMBOL (CONTAINS SYSTEM TEST ACCESS AND MCH ACCESS).

PART ØF FS 7
COMPOSITE DIAGRAM 2

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B7GB

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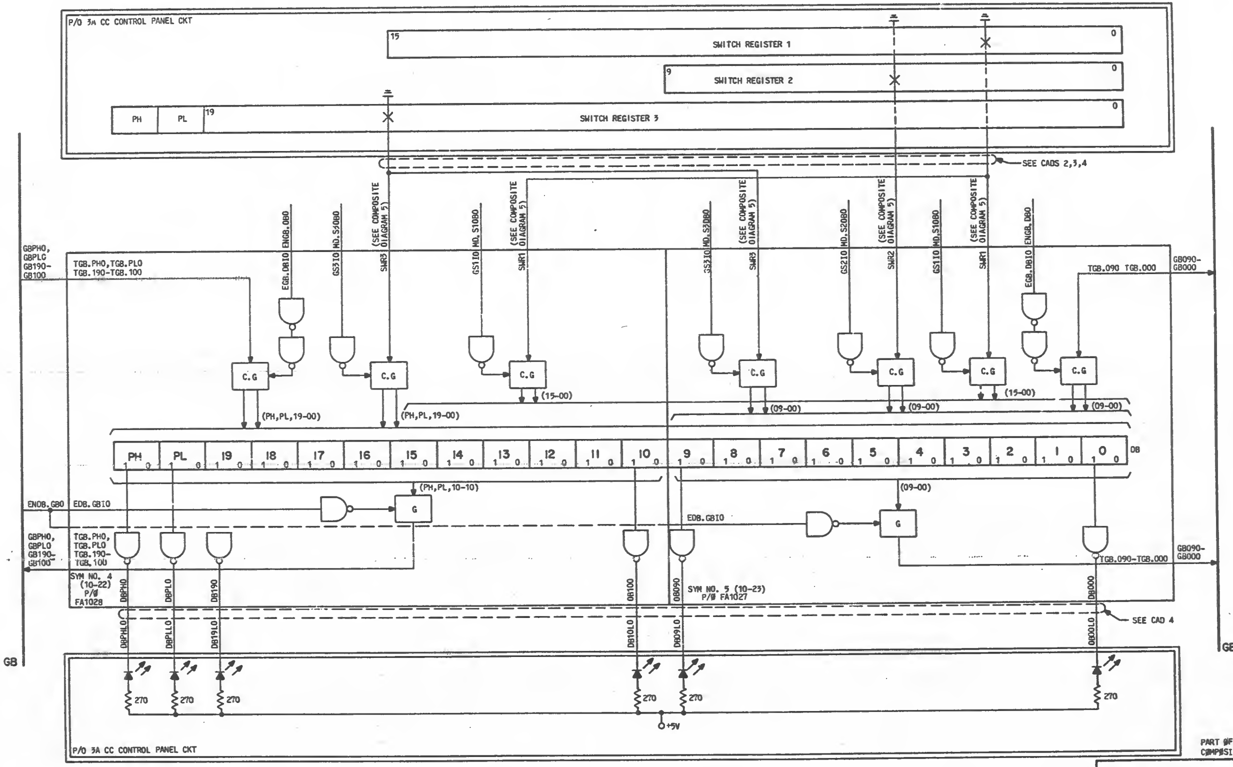
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 3

DISPLAY BUFFER OPERATION

CIRCUIT OPERATION
(SEE SHEET B7GD)



PART OF FS 7
COMPOSITE DIAGRAM 3

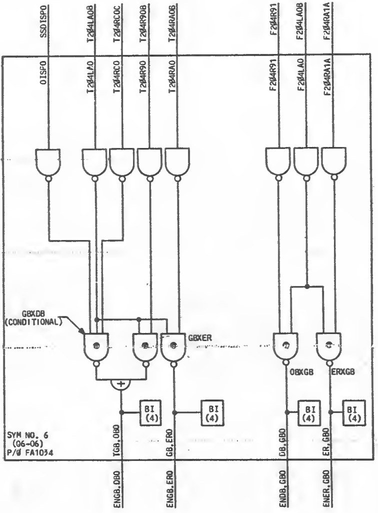
3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B7GC

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 4

DECODING OF THE TO AND FROM FIELD FOR THE DB AND ER REGISTERS



CIRCUIT OPERATION (CONT)

MANUAL AND EITHER 1) TEST MODE OR 2) OFF LINE AND EITHER DISABLED OR LOCKED OFF-LINE TO ALLOW POWER TO BE REMOVED. IF ONE OF THESE CONDITIONS ARE MET, THE NET LKØFF IS HIGH AND THE ACTIVATION OF THE POWER KEY WILL ALLOW POWER TO BE REMOVED FROM THE 3A CC. IF THE,POWER KEY IS ACTIVATED FROM THE "OFF" TO THE "ON" POSITION, SIGNALS FROM THE POWER KEY ACTIVATE THE PROCESSOR FRAME POWER CIRCUIT AND ALLOW POWER TO BE TURNED ON. WHEN POWER IS TURNED ON, POWER IS SEQUENCED. POWER IS FIRST TURNED ON TO A SMALL PORTION OF THE 3A CC THAT CONTAINS SOME INITIALIZATION LOGIC. IN PARTICULAR, POWER IS TURNED ON TO CIRCUIT PACK FA1034 WHICH IS SHOWN IN SYMBOL 1 AND SYMBOL 20 IN COMPOSITE DIAGRAM 2. SIMULTANEOUSLY WITH TURNING POWER ON TO THIS CIRCUIT PACK, A POWER INITIALIZATION SIGNAL IS SENT FROM THE PROCESSOR FRAME POWER CIRCUIT VIA NET PWRØFF WHICH ALLOWS KEY FLIP-FLOPS IN THE 3A CC TO BE INITIALIZED. AS INDICATED, THESE FLIP-FLOPS ARE THE DISABLED FLIP-FLOP, THE ISC FLIP-FLOPS, THE PROGRAM TIMER REGISTER, AND THE CC FLIP-FLOP. THE PURPOSE OF SETTING THE DISABLED FLIP-FLOP IS SO THAT WHEN POWER IS TURNED ON TO THE REMAINING PORTIONS OF THE 3A CC AND IN PARTICULAR THE I/Ø CHANNEL, ANY ERRONEOUS OUTPUTS FROM THE I/Ø CHANNEL WILL BE INHIBITED. THE CC FLIP-FLOP MUST BE PUT IN THE STANDBY MODE, THE PROGRAM TIMER MUST BE CLEARED TO PREVENT A PROGRAM TIMER TIMEOUT AND THE ISC BITS MUST BE CLEARED TO AN INITIAL STATE SO THAT ALL SUBSEQUENT INITIALIZATIONS, POWER OR OTHERWISE, WILL INVOKE THE PROPER MICROCODE INITIALIZATION PROCEDURES. NOTE THAT A POWER INITIALIZATION, IN ADDITION TO PERFORMING THE DESCRIBED OPERATION, INITIATES A MRF INITIALIZATION, THAT TO THE MICROCODE APPEARS LIKE A RESET CIRCUIT MRF AND HENCE, THE PANEL-HALT LOOP WILL BE ENTERED (SEE SHEET B7GB).

COMPOSITE DIAGRAM 4 SHOWS THE FINAL STAGE OF THE DECODING FOR THE TO FIELDS AND FROM FIELDS, FOR THE DB REGISTER, AND THE ER REGISTER. THESE TO-FIELD AND FROM-FIELD CROSSPOINTS OPERATE EXACTLY IN THE SAME MANNER AS OTHER TO-FIELD AND FROM-FIELD CONTROL POINTS IN THE 3A CC, WITH THE ONE EXCEPTION. THERE IS A SPECIAL TO-FIELD CROSSPOINT THAT CONDITIONALLY GATES THE GB TO THE DB REGISTER. THE ACTIVATION OF THIS TO-FIELD CROSSPOINT IS CONDITIONED ON THE DISPLAY BIT, BIT 17 OF THE SS REGISTER. IF THIS BIT IS SET, THE GB IS GATED INTO THE DB. THE PURPOSE OF THIS FUNCTION IS TO ALLOW ALL BRANCH COMMANDS TO GATE THE CONTENTS OF THE PA REGISTER PLUS ONE TO THE DB IF THE DISPLAY BIT IS ACTIVE. THIS PROVIDES A CONVENIENT ONE WORD TRANSFER TRACE FOR PROGRAM DEBUGGING AND A VISUAL INDICATION THAT A 3A CC IS RUNNING.

CIRCUIT OPERATION (CONT)

RESPOND BY LIGHTING THE REJECT LED ON THE 3A CC CONTROL PANEL AND IT WILL ALSO GATE ALL ONES TO THE DB, SO AS TO BRING ATTENTION TO A REJECTED FUNCTION.

WITH THE MICROCODE HAVING DETERMINED THAT A VALID LOAD AND DISPLAY OPERATION HAS BEEN REQUESTED IT WILL THEN GATE SWITCH REGISTER 2 TO THE DB. THE DB NOW CONTAINS THE BINARY REPRESENTATION OF WHICH ONE OF THE 16 REGISTERS IS TO BE GATED TO. IN ADDITION, FORM THE CONTENTS OF SWITCH REGISTER 2 THE MICROCODE WILL DETERMINE WHETHER THESE 16 REGISTERS ARE FROM THE GENERAL REGISTER CLASS OR FROM THE SPECIAL REGISTER CLASS. THE MICROCODE WILL TYPICALLY GATE THE BINARY NUMBER REPRESENTING THE REGISTER SELECTED TO THE IB REGISTER. ONCE IN THE IB REGISTER THAT IS DESCRIBED IN FS 1. THE MICROCONTROL CAN EASILY SELECT THE APPROPRIATE TO AND FROM FIELD ASSOCIATED WITH THE REGISTER SELECTED.

THE THIRD SEGMENT OF THE REGISTER OPERATION IS TO OBTAIN THE DATA FROM THE INPUT DATA KEYS ON 3A CC CONTROL PANEL. THESE KEYS ARE OBTAINED BY GATING SWITCH REGISTER 3 TO DB. NOTE ALSO THAT THERE IS AN AUTOMATIC PARITY GENERATION OPTION ON THESE KEYS AND THIS OPTION IS DETERMINED BY ANOTHER BIT IN SWITCH REGISTER 1. THEREFORE, IF NECESSARY MICROCODE WILL GENERATE PARITY ON THE 20-BIT DATA INPUT REGISTER KEYS BY GATING THIS INPUT DATA TO THE DML LOGIC. IN ORDER TO GATE POTENTIALLY BAD PARITY DATA TO THE DML FROM THE DB THE GB PARITY CHECKER, AS DESCRIBED IN FS 6, MUST BE MOMENTARILY INHIBITED TO PREVENT A GB PARITY CHECK ERROR. ONCE PARITY HAS BEEN COMPUTED IN THE DML, THE INPUT KEY DATA CAN BE FREELY GATED AROUND THE 3A CC WITHOUT CAUSING PARITY PROBLEMS. IN THIS PARTICULAR EXAMPLE, THE DATA INPUT KEYS WILL BE LOADED INTO THE DEFINED DESTINATION REGISTER. THEN ON A SUBSEQUENT MICROCYCLE, THE OUTPUT OF THAT REGISTER WILL BE GATED BACK ONTO THE GB AND PLACED IN THE DB REGISTER SINCE THE REGISTER DISPLAY KEY WAS ALSO ACTIVATED. ONCE PLACED IN THE DISPLAY BUFFER THE MICROCODE WILL RETURN TO THE PANEL-HALT LOOP AND THE CONTENTS OF THE DB WILL BE VISIBLE ON THE LED'S ON THE 3A CC PANEL. AS INDICATED IN COMPOSITE DIAGRAM 3, THERE IS A SET OF LED'S ATTACHED DIRECTLY TO THE OUTPUT OF THE DB REGISTER, AND THEREFORE IN THIS INSTANCE, THE DATA THAT ORIGINATED FROM THE INPUT KEYS WILL RESIDE IN THE DB REGISTER AND CAN BE READ OUT VISUALLY. NOTE THAT THE REGISTER SELECT KEYS HAVE A HARDWIRED TRANSLATOR TO CONVERT THE BINARY TO A 1-OUT-OF-6 TRANSLATION TO LIGHT THE LED'S ON THE PANEL ITSELF. SIMILARLY, THE GENERAL OR SPECIAL REGISTER SELECT KEY, AS WELL AS THE ENABLE-MANUAL-PARITY KEYS ARE HARDWIRED TO LED'S (SEE COMPOSITE DIAGRAM 2).

ALSO SHOWN ON COMPOSITE DIAGRAM 2 IS THE STATUS LAMPS ON THE 3A CC CONTROL PANEL. EACH STATUS LAMP BASICALLY DEFINES THE MODE OR STATE OF THE GIVEN 3A CC IN WHICH THEY RESIDE. THERE IS A LAMP THAT INDICATES WHETHER POWER IS ON OR OFF. A LAMP THAT INDICATES THE ACTIVE OR NOT ACTIVE STATUS, A LAMP INDICATING WHETHER THE MANUAL KEY IS ACTIVE, AND HENCE, WHETHER THE MACHINE IS IN A MANUAL MODE. AN ERROR-STOP LAMP WHICH INDICATES WHETHER THE 3A CC HAS BEEN ERROR STOPPED. A TEST-MODE LAMP WHICH INDICATES WHETHER THE TEST-MODE KEY IS ACTIVATED, AND A LAMP-TEST KEY TO TEST THE LAMP CONDITIONS. NOTE THAT THE STOP LAMP, THE ACTIVE OR STANDBY LAMP, AS WELL AS THE MANUAL LAMP ARE DRIVEN DIRECTLY FROM THE SYSTEM STATUS (SS) REGISTER. THE REJECT STATE IS ALSO ANOTHER BIT IN THE SS REGISTER, INDICATING AN INVALID COMBINATION OF CONTROL KEYS ON THE 3A CC CONTROL PANEL.

SYMBOL 1 ALSO CONTAINS LOGIC THAT DETERMINES WHETHER POWER CAN BE TURNED OFF ON A GIVEN 3A CC. THAT IS, THE 3A CC MUST BE IN A PREDETERMINED STATE TO HAVE ITS POWER TURNED OFF. THE 3A CC MUST BE IN

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 2-5

MOST 3A CC CONTROL PANEL FUNCTIONS ARE EXECUTED OUT OF PANEL-HALT LOOP. THE PANEL-HALT LOOP IS SPECIAL MICROCODED LOOP THAT CONTINUOUSLY INTERROGATES THE STATE OF THE INTERRUPT LEVEL THAT IS ASSIGNED TO PANEL FUNCTIONS. THIS INTERRUPT LEVEL IS 13 AND HENCE, CORRESPONDS TO BIT 13 OF THE IS REGISTER. ONCE A 3A CC HAS BEEN INITIALIZED AND IS IN THE PANEL-HALT LOOP, PANEL FUNCTIONS CAN BE PERFORMED. IT SHOULD BE NOTED THAT IT MAY NOT ALWAYS BE NECESSARY TO ACTIVATE THE RESET-CIRCUIT KEY TO GAIN ACCESS TO THE 3A CC CONTROL PANEL. THAT IS, THERE ARE METHODS OTHER THAN INITIALIZATION TO PUT A 3A CC IN THE PANEL-HALT LOOP. THE ACTIVATION OF THE RESET-CIRCUIT KEY IS THE MOST STRAIGHTFORWARD AND WILL GUARANTEE THE MICROCONTROL WILL TRANSFER TO THE PANEL-HALT LOOP IF THE 3A CC IS THE APPROPRIATE STATE. ONCE CONTROL IS AVAILABLE BY THE VIRTUE OF BEING IN THE PANEL-HALT LOOP ADDITIONAL CONTROL FUNCTIONS CAN BE PERFORMED VIA THE 3A CC CONTROL PANEL. THESE FUNCTIONS BASICALLY CONSIST OF LOADING OR DISPLAYING REGISTERS OR THE MAIN STORE, SINGLE STEPPING THROUGH MACROLEVEL INSTRUCTIONS OR GENERATING MATCH FUNCTION ON MAIN STORE ADDRESSES OR DATA. THE OPERATION OF THESE FUNCTIONS IS PERFORMED BY A SINGLE OR MULTIPLE STEP PROCEDURE WHERE A SINGLE STEP CONSISTS OF SETTING-UP THE DESIRED FUNCTION ON THE CONTROL AND DATA KEYS AND THEN OPERATING THE EXECUTE FUNCTION. THE EXECUTE WILL IN TURN GENERATE A PANEL INTERRUPT WHICH WILL INTERROGATE THE STATE OF THE PANEL KEYS AND PERFORM THE DESIRED FUNCTION. IF THE FUNCTION REQUESTED IS AN INVALID ONE, THE PANEL MICROCODE WILL LIGHT THE REJECT LED. IN ALL CASES, EXCEPT IF THE HALT KEY IS NOT ACTIVE, THE MICROPROGRAM CONTROL WILL COMPLETE A PANEL STEP OPERATION BY SETTING THE PANEL HALT LED AND RETURN TO THE PANEL-HALT LOOP WAITING FOR THE NEXT PANEL FUNCTION. IF THE PANEL-HALT KEY IS NOT ACTIVE AND AN EXECUTE IS GIVEN, THE LOCATION IN THE PA REGISTER WILL BE LOADED INTO THE SAR AND MACROLEVEL INSTRUCTION EXECUTION WILL BE INITIATED AT THIS LOCATION.

AN EXAMPLE OF A PANEL FUNCTION IS A REGISTER LOAD AND DISPLAY FUNCTION. FIRST A REGISTER IS SELECTED VIA THE REGISTER SELECT KEYS. ONE OF 16 REGISTERS OF EITHER THE GENERAL OR THE SPECIAL CLASS IS CHOSEN WITH THE APPROPRIATE KEYS. THE ONLY ADDITIONAL CONTROL REQUIRED IS TO ACTIVATE THE LOAD AND DISPLAY FUNCTION KEYS FOR REGISTERS. THEN THE EXECUTE KEY IS ACTIVATED. THE EXECUTE KEY, SIMILAR TO THE RESET CIRCUIT KEY, IS FIRST BUFFERED THROUGH A FLIP-FLOP TO REMOVE ANY BOUNCE ON THE KEY, AND THEN IT INPUTS DIRECTLY INTO THE SET SIDE OF BIT 13 OR THE IS REGISTER. WHEN THE INTERRUPT CODE IS ENTERED. IT WILL INTERPRET THE STATE OF THE KEYS THAT ARE ACTIVATED ON THE 3A CC CONTROL PANEL, AND IN THIS PARTICULAR CASE, THE MICROCODE WILL DETERMINE THAT A LOAD AND DISPLAY FUNCTION OF A GIVEN REGISTER HAS BEEN REQUESTED. NOTE THAT THE STATE OF THE REGISTER SELECT KEYS IS ACCESSED BY USING MISCELLANEOUS DECODER CROSSPOINT CONTROL SIGNALS TO GATE THE STATE OF THE SWITCHES INTO THE DB REGISTER. SEE COMPOSITE DIAGRAM 3. FOR CONVENIENCE IN ACCESSING THE SWITCHES ON THE 3A CC PANEL, THE SWITCHES HAVE BEEN GROUPED INTO THREE REGISTERS. THE ASSIGNMENT OF THESE SWITCHES AND THEIR FUNCTIONS IS DETAILED IN COMPOSITE DIAGRAM 5. NOTE THAT THE REGISTER SELECT KEYS ARE IN SWITCH REGISTER 2, MOST OF THE BASIC CONTROL KEYS ARE IN SWITCH REGISTER 1, AND THE DATA INPUT KEYS ARE IN SWITCH REGISTER 3. THEREFORE, FOR THE REGISTER LOAD AND DISPLAY FUNCTION, THE MICROCODE WILL GATE SWITCH REGISTER 1 TO THE DB, AND THEN GATE THE DB TO THE DML LOGIC TO TEST THE RESPECTIVE BITS OF SWITCH REGISTER 1 TO DETERMINE WHAT FUNCTION HAS BEEN REQUESTED. IN THIS INSTANCE, IT WILL DETERMINE THAT A LOAD AND DISPLAY FUNCTION HAS BEEN REQUESTED AND IT WILL ALSO CHECK TO MAKE SURE THAT NO OTHER FUNCTION WAS REQUESTED SO AS TO ASSERTAIN WHETHER AN INVALID REQUEST HAS BEEN MADE. IF AN INVALID REQUEST HAS BEEN SET UP, THE MICROCODE WILL

COMPOSITE DIAGRAM 5

SWITCH REGISTER ASSIGNMENT INTO THE DB REGISTER

SWITCH REGISTER 1 (SWR1)						SWITCH REGISTER 2 (SWR2)					SWITCH REGISTER 3 (SWR3)				
DISPLAY BUFFER BIT	TERM MØD	NETNAME (PIN NØ.)			FUNCTION	TERM MØD	NETNAME (PIN NØ.)			FUNCTION	TERM MØD	NETNAME (PIN NØ.)			FUNCTION
00	MPKO	MPKO	(10-23) FA1027	(216)	MAN PTY KEY	RS1KO	RS1KO	(10-23) FA1027	(003)	REG SELECT KEY	IK00	IK000	(10-23) FA1027	(100)	DATA INPUT KEY
01	STEPKO	STEPKO		(004)	STEP KEY	RS2KO	RS2KO		(303)	REG SELECT KEY	IK10	IK010		(103)	
02	HALTKO	HALTKO		(304)	HALT KEY	RS4KO	RS4KO		(104)	REG SELECT KEY	IK20	IK020		(204)	
03	BAEXKO	BAEXKO		(315)	BASIC OR EXTENDED KEY	RS8KO	RS8KO		(012)	REG SELECT KEY	IK30	IK030		(311)	
04	DISRKO	DISRKO		(312)	DISPLAY REG KEY	SGKO	SGKO		(112)	GENERAL OR SPECIAL	IK40	IK040		(212)	
05	LOADKO	LOADKO		(213)	LOAD KEY						IK50	IK050		(013)	
06	RESCKO	RESBO		(109)	RESET CKT (S) FF ØP						IK60	IK060		(113)	
07	TMKOA	TMKOA		(210)	TST MODE REVERSAL KEY						IK70	IK070		(309)	
08	CDAKTO	CDAKTO		(110)	DATA MATCH KEY						IK80	IK080		(010)	
09	CADRKO	CADRKO		(011)	ADRS MATCH KEY	PWRKBB	PWKO		(314)	PWR KEY (BB CONT) ON-OFF	IK90	IK090		(310)	
10	MANKO	MANKO	(10-22) FA1028	(105)	MANUAL KEY			(10-22) FA1028			IK100	IK100	(10-22) FA1028	(011)	
11											IK110	IK110		(211)	
12	DISMKO	DISMKO		(111)	DISPLAY MEM KEY						IK120	IK120		(311)	
13	STØKO	STØKO		(212)	STORE IN MEM KEY						IK130	IK130		(012)	
14	IADRKO	IADRKO		(112)	INCREMENT ADRS KEY						IK140	IK140		(016)	
15	HILØKO	HILØKO		(205)	HIGH-LOW MEM KEY						IK150	IK150		(216)	
16											IK160	IK160		(116)	
17											IK170	IK170		(316)	
18											IK180	IK180		(017)	
19											IK190	IK190		(217)	DATA INPUT KEY
PL											IKPLO	IKPLO		(117)	PNL PTY LOW IN. DA KEY
PH											IKPHO	IKPHO		(317)	PNL PTY HIGH IN. DA KEY

PART ØF FS 7
COMPOSITE DIAGRAM 4,5

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	5A

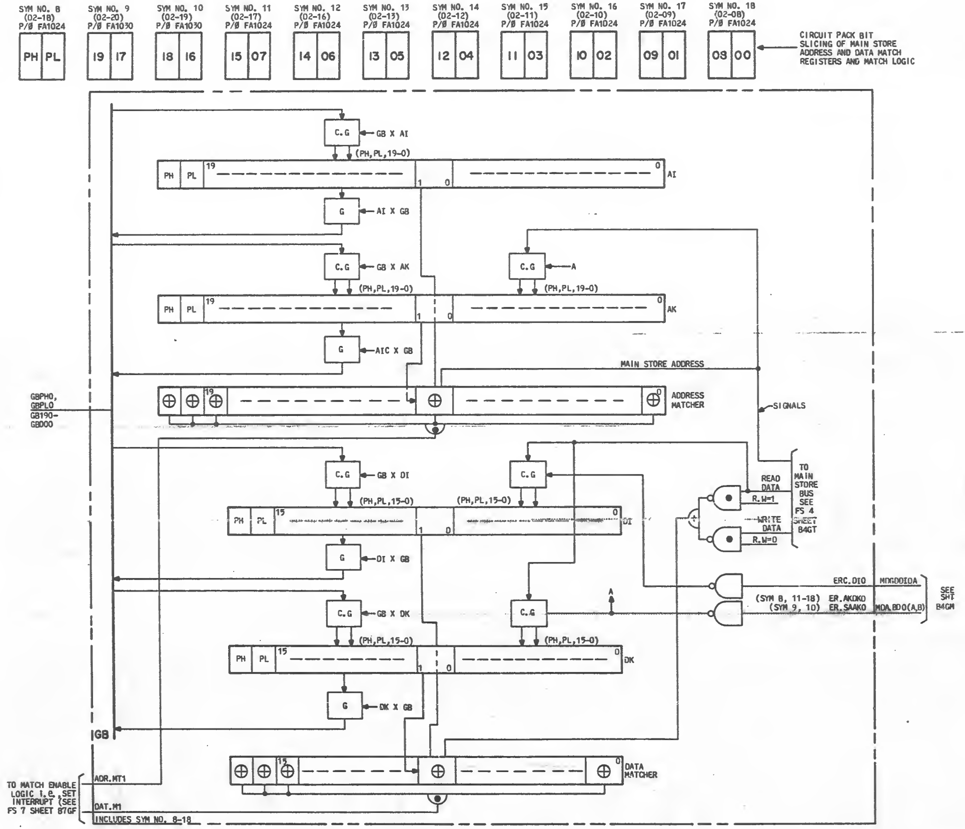
BELL LABORATORIES | SD-1C900-01 | B7GD

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 6

MAIN STORE ADDRESS AND DATA MATCH LOGIC



CIRCUIT OPERATION

THE MAIN STORE (MAS) ADDRESS AND DATA MATCH LOGIC IS NORMALLY USED IN CONJUNCTION WITH THE OPERATION OF THE 3A CC CONTROL PANEL. THIS LOGIC ALLOWS A SINGLE ADDRESS MATCH, TOGETHER WITH A SINGLE DATA MATCH, TO BE PERFORMED ON ANY GIVEN MEMORY CYCLE. THE ADDRESS THAT IS MATCHED IS THE ACTUAL 20-BIT ADDRESS THAT IS PLACED ON THE MAIN STORE BUS (MASB) FOR A GIVEN MEMORY OPERATION. THE DATA THAT IS MATCHED IS THE DATA THAT IS ON THE MASB FOR A GIVEN MEMORY CYCLE. NOTE THAT SINCE IT IS POSSIBLE TO PERFORM A MAS FUNCTION WITH EITHER "MY" MAS OR THE "OTHER" MAS THE ADDRESS MATCHER AND DATA MATCHER MAKE NO DISTINCTION. THE TYPICAL MODE OF OPERATION TO PERFORM AN ADDRESS MATCH FUNCTION IS TO LOAD THE ADDRESS INPUT (AI) REGISTER WITH THE ADDRESS THAT IS TO BE MATCHED. THIS IS PERFORMED BY A LOAD AND DISPLAY FUNCTION OF THE AI REGISTER VIA NORMAL PANEL FUNCTION AS DESCRIBED ON SHEET B7GD. SIMILARLY, THE ADDRESS MASK (AK) REGISTER IS LOADED WITH THE DESIRED MASK. IF THE AK IS SET TO ALL ZEROS, NO BITS OF THE ADDRESS ARE MASKED OFF FOR THE MATCH TO BE PERFORMED. NOTE THAT THE PARITY BITS ARE INCLUDED IN THE MATCHER, BUT SINCE THE AK REGISTER IS TYPICALLY LOADED WITH ALL ZEROS TO MAINTAIN GOOD PARITY, THE PL BIT AND PH BIT OF THE AK ARE SET TO ONE AND, THEREFORE, THE PARITY BITS DO EFFECT THE MATCH FUNCTION.

THE DATA MATCH INPUT (DI) REGISTER, AND THE DATA MASK (DK) REGISTER, OPERATE IN EXACTLY THE SAME MANNER AS THE AI AND AK EXCEPT THAT THE DI AND DK ARE 16-BIT REGISTER, AND THE AI AND THE AK ARE 20-BIT REGISTERS WITH THEIR RESPECTIVE PARITY BITS. ONCE THE ADDRESS MATCH AND/OR THE DATA MATCH REGISTERS ARE SET UP, THE MATCH FUNCTION IS ENABLED BY SETTING THE APPROPRIATE BITS IN THE SYSTEM STATUS REGISTER (SEE SHEET B7GF FOR DESCRIPTION OF THE MATCH ENABLE LOGIC).

AN AUXILIARY FUNCTION OF THE AK, THE DI, AND THE DK REGISTER IS SHOWN IN THIS COMPOSITE DIAGRAM. THESE REGISTERS ARE USED IN CONJUNCTION WITH THE DOUBLE STORE CIRCUITRY. THAT IS, WHEN A STORE ERROR C SIGNAL IS RECEIVED FROM THE MAS, A SPECIAL HARDWARE SIGNAL GENERATED BY THE PROCESSOR BUS CONTROLLER LOGIC, AS DESCRIBED ON SHEET B4GM, WILL ENABLE THE GATING OF THE ADDRESS PRESENTLY ON THE MASB INTO THE AK REGISTER. THE DATA PRESENTLY ON THE MAIN STORE BUS IS GATED INTO THE DK REGISTER. THIS ADDRESS AND DATA CORRESPONDS TO THE ADDRESS AT WHICH A READ PARITY ERROR OCCURS AND THE DATA CORRESPONDS TO THE DATA THAT IS ACTUALLY READ OUT OF THE STORE INCORRECTLY. THEN ON A MEMORY CYCLE IMMEDIATELY FOLLOWING THE RECEPTION OF A STORE ERROR C, THE READ OF THE "OTHER" MAS IS PERFORMED AND THAT DATA IS RETURNED TO THE PROCESSOR. THIS DATA, IN ADDITION TO BEING GATED TO THE STORE INSTRUCTION REGISTER OR THE STORE DATA REGISTER, IS ALSO GATED TO THE DI REGISTER. UNLESS THIS REREAD WAS UNSUCCESSFUL, WHICH WOULD NORMALLY BE VERY UNLIKELY, THE DI CONTAINS THE GOOD DATA. THE DK CONTAINS THE BAD DATA WORD, AND THE AK CONTAINS THE ADDRESS AT WHICH BOTH OF THESE WORDS ARE LOCATED IN THE MAS. IN THIS WAY THE HARDWARE AIDS IN THE COLLECTION OF DATA FOR A LATER ANALYSIS BY SOFTWARE.

TABLE A

TO-AND-FROM-FIELD DECODER								
SPECIAL REGISTER	GBX SPECIAL REGISTER TO-FIELD PAIR				SPECIAL REGISTER GBX FROM-FIELD PAIR			
	NETNAME	(PIN N0.)			NETNAME	(PIN N0.)		
AI	T204LADA	(308)	T204R30B	(010)	F204LA0A	(216)	F204R30B	(213)
*	T204LA0B	(318)	T204R30C	(118)	F204LA0B	(211)	F204R30C	(311)
AK	T204L90A	(009)	T204RC0B	(209)	F204L90A	(016)	F204RC0B	(113)
*	T204L90B	(316)	T204RC0C	(218)	F204L90B	(111)	F204RC0C	(014)
DI	T204LA0A	(308)	T204R60B	(109)	F204LA0A	(216)	F204R60B	(315)
DK	T204LA0A	(308)	T204R50B	(309)	F204LA0A	(216)	F204R50B	(115)

* APPLY TO SYM NO. 9 AND 10

PART 0F FS 7
C0MP0SITE DIAGRAM 6

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	5A

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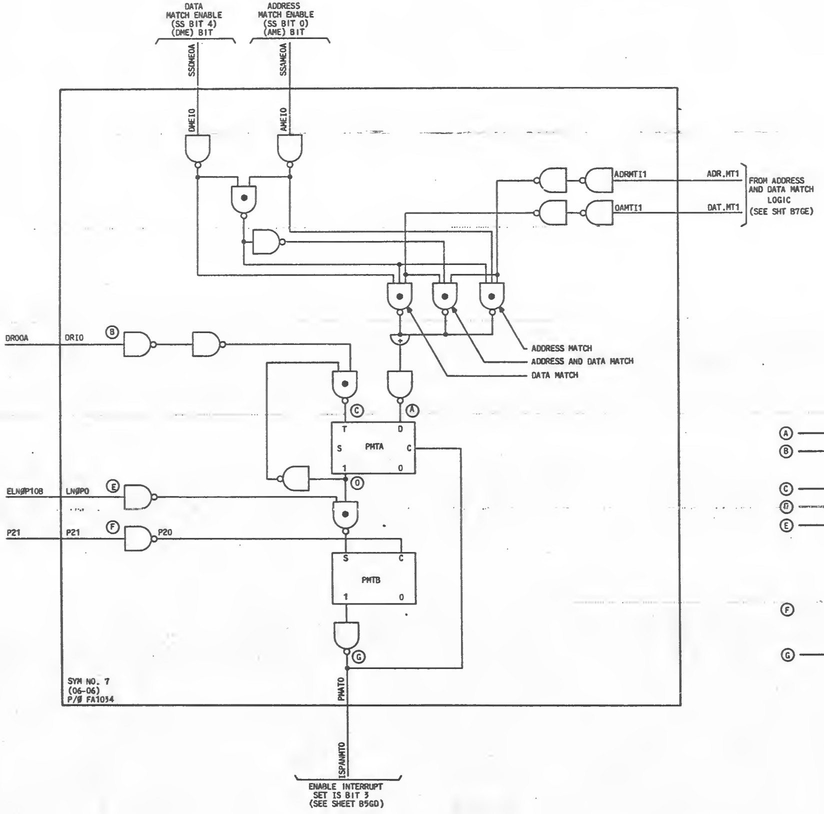
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 7

3A CC PANEL ADDRESS AND DATA MATCH
ENABLE LOGIC

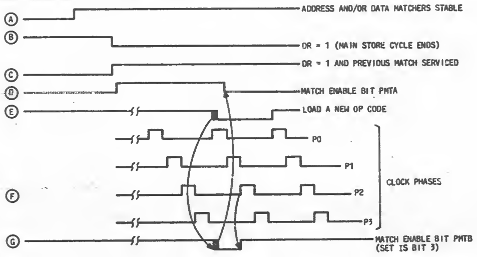


CIRCUIT OPERATION

THE MATCH ENABLE LOGIC IS USED IN CONJUNCTION WITH THE ADDRESS AND DATA MATCH REGISTERS AND THE 3A CC CONTROL PANEL LOGIC TO ALLOW ADDRESS AND DATA MATCHES TO BE PERFORMED. FIRST THE OPERATION OF AN ADDRESS MATCH FUNCTION WILL BE DESCRIBED. AN ADDRESS MATCH IS INITIATED BY LOADING THE AI AND THE AK REGISTERS FROM THE 3A CC PANEL. THEN THE ADDRESS MATCH ENABLE KEY IS OPERATED FROM THE 3A CC PANEL. THE STATE OF THIS KEY IS THEN GATED TO BIT 0 (ADDRESS MATCH ENABLE [AME]) OF THE SS REGISTER VIA MICROCODE ONCE THE PANEL EXECUTE KEY IS OPERATED. AS SHOWN ON COMPOSITE DIAGRAM 7, THIS BIT ENABLES AN ADDRESS MATCH GATE SHOWN IN SYMBOL 7. THIS GATE WILL FIRE IF AN ADDRESS MATCH OCCURS. IF THIS GATE FIRES, POINT A WILL BECOME ACTIVE THEN WHEN THE DR FLIP-FLOP GETS SET OR, IN OTHER WORDS, AT THE END OF A MAIN STORE CYCLE THE STATE OF POINT A WILL BE GATED INTO THE PMTA FLIP-FLOP. THIS IN TURN WILL ACTIVATE THE PMTA FLIP-FLOP BY CAUSING A HIGH-LEVEL SIGNAL AT POINT D. ONCE POINT D IS ACTIVATED, IT IS FED BACK TO THE INPUT OF THE PMAT TO PREVENT ANY SUBSEQUENT MEMORY CYCLES FROM CLEARING THE PMTA FLIP-FLOP. NOTE THAT THIS IS NECESSARY BECAUSE THE ORDER OF OBTAINING WORDS FROM THE MAS MAY NOT BE THE ORDER IN WHICH THEY ARE PROCESSED BY THE 3A CC. THEREFORE, IF THE ADDRESS MATCH FUNCTION HAS BEEN ACTIVATED AND HENCE THE PMTA FLIP-FLOP IS SET, IT IS IMPORTANT NOT TO CLEAR IT ON A SUBSEQUENT MEMORY CYCLE UNTIL THE MATCH FUNCTION HAS BEEN SERVICED. NOTE THAT THE MATCH FUNCTION INITIATES AN INTERRUPT TO ACTUALLY SERVICE IT OR, IN OTHER WORDS, COMPLETE ITS OPERATION. THE OUTPUT OF THE PMTA FLIP-FLOP IS THEN GATED BY THE LOAD NEW OP CODE (LNØP) SIGNAL INTO THE PMTB FLIP-FLOP. THIS GATING GUARANTEES THAT AN ADDRESS MATCH FUNCTION WILL NOT BE SERVICED UNTIL THE INSTRUCTION AT THAT ADDRESS HAS COMPLETED ITS EXECUTION. THIS IS NECESSARY SO THAT WHEN 3A CC CONTROL PANEL OPERATION HAS COMPLETED AND THE PROGRAM RETURNS TO NORMAL EXECUTION FLOW, IT WILL NOT BE "IMMEDIATELY" INTERRUPTED BY THE SAME ADDRESS LOCATION. THIS WOULD BE THE CASE IF THE MATCH FUNCTION WAS SERVED BEFORE THE INSTRUCTION AT THAT LOCATION WAS EXECUTED. WITH THE LNØP FUNCTION STROBING THE OUTPUT OF THE PMTA FLIP-FLOP INTO THE PMTB FLIP-FLOP A PULSE IS GENERATED ON THE OUTPUT GATE SHOWN AS POINT G. THEN THE PMTB FLIP-FLOP IS CLEARED AT CLOCK PHASE P2. NOTE THAT THE OUTPUT OF POINT G INPUTS TO THE PANEL INTERRUPT BIT 3 OF THE IS REGISTER. IN THIS WAY THE 3A CC PANEL MATCH GENERATES AN INTERRUPT. THIS INTERRUPT IS LIKE ALL OTHER INTERRUPTS AND IN ORDER TO BE SERVICED THE CORRESPONDING MASK BIT IN THE IM REGISTER MUST BE CLEARED TO ALLOW THE PANEL MATCH INTERRUPT TO OCCUR. THE TYPICAL OPERATION OF THE PANEL MATCH MICROCODE IS TO DETERMINE WHETHER THE 3A CC PANEL IS IN A VALID MODE TO ALLOW THE MICROPROGRAM CONTROL TO TRANSFER TO THE PANEL-HALT LOOP. IF THE 3A CC CONTROL PANEL IS IN A VALID STATE, THAT IS, IN THE MANUAL MODE AND IN STANDBY OR ACTIVE AND IN TEST MODE, THEN CONTROL IS TRANSFERRED TO THE PANEL-HALT LOOP. OTHERWISE, THE MICROCODE TRANSFERS CONTROL TO A MAS LOCATION THAT INITIATES A SEQUENCE OF MACROLEVEL CODE THAT WILL PERFORM THE ADDRESS MATCHING SERVICING FUNCTION VIA A SOFTWARE UTILITY OPERATION. IN THIS MANNER SOFTWARE CAN SET UP ALL OF THE CONDITIONS AS DESCRIBED ABOVE, AND HENCE, GENERATE AN ADDRESS MATCH WITH THE CONTROL BEING TRANSFERRED TO THE UTILITY PROGRAM IF THE ADDRESS MATCH OCCURS.

THE DATA MATCH FUNCTION OPERATES IN EXACTLY THE SAME MANNER WITH BIT 4 (DATA MATCH ENABLE DME) OF THE SS REGISTER SET AND THE DATA MATCH ENABLE KEY OPERATED ON THE 3A CC PANEL. NOTE THAT IF BOTH THE ADDRESS MATCH AND THE DATA MATCH ENABLE KEYS ARE OPERATED, THEN A MATCH IS NOT GENERATED UNLESS AN ADDRESS AND DATA MATCH OCCUR SIMULTANEOUSLY ON THE SAME MAS CYCLE.

TIMING DIAGRAM FOR THE PANEL MATCH ENABLE FUNCTION



PART ØF FS 7
CØMPØSITE DIAGRAM 7

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B7GF

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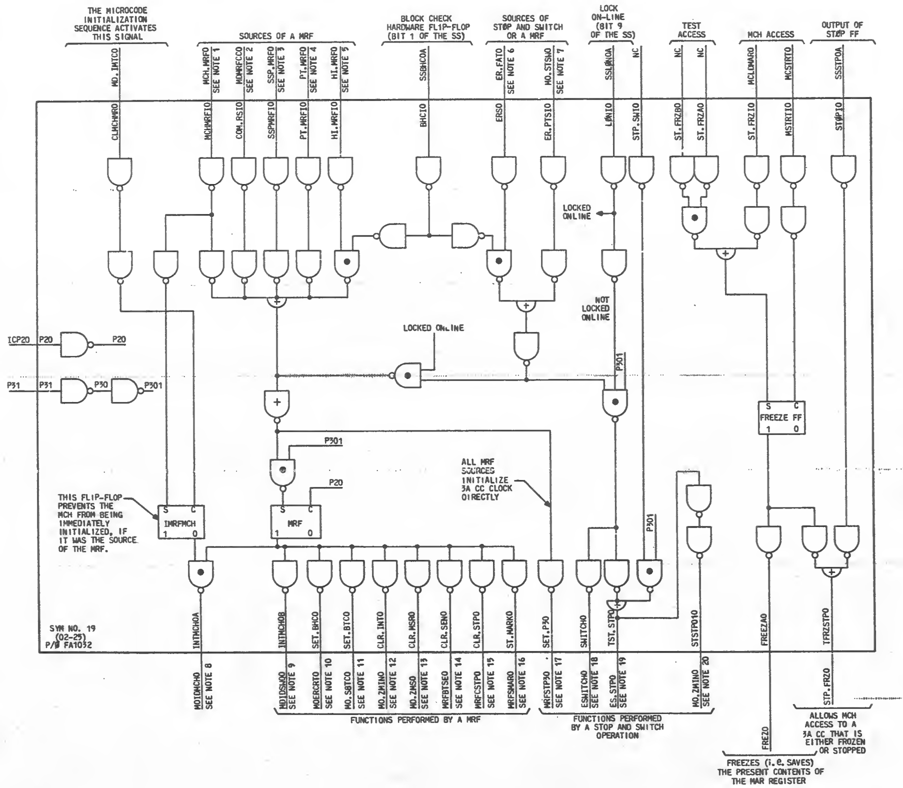
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 8

POWER INITIALIZATION AND MAINTENANCE
RESET FUNCTIONS (MRF) CIRCUITRY



NOTES:

FUNCTION INPUTS THAT CAN CAUSE A MRF

1. MCH MRF (SEE SHT B9GJ).
2. RESET CIRCUITS FUNCTION FROM CC PANEL (SEE SHT 87GB).
3. SYSTEM STATUS PANEL MRF (SEE SHT 87GJ).
4. PROGRAM TIMER TIMEOUT 1ST OR 2ND (SEE SHT B8GE).
5. HARDWARE MRF ERROR, BA ERROR, WRITE PROTECT ERROR OR MY STORE FAST TIMEOUT ERROR (SEE SHT B5GB).

THESE FUNCTIONS EITHER CAUSE A STØP AND A SWITCH FROM ONE 3A CC TO ANOTHER OR THEY MRF THE 3A CC IN WHICH THE FUNCTION ORIGINATED DEPENDING UPON THE LOCK ON-LINE FLIP-FLOP

6. HARDWARE FATAL ERROR (ALL MAJOR 3A CC AND MAIN STORE ERRORS ARE IN THIS CATAGORY (SEE SHT B5GE).
7. STOP AND SWITCH MICROINSTRUCTION.
8. IDLE MCH (SEE SHT B9GJ).

FUNCTIONS PERFORMED BY THE MRF LOGIC

9. CLEAR MCH SWITCH SEQUENCER (SEE SHT B9GN).
10. SET BLOCK HARDWARE CHECK BIT (SEE SHT B5GF).
11. SET BLOCK TIMER CHECK BIT (SEE SHT B5GF).
12. CLEAR THE MICROINTERPRET BIT (SEE SHT B5GF).
13. CLEAR THE MAINTENANCE STATE REGISTER (SEE SHT B5GD).
14. INITIALIZE I/Ø ENABLE LOGIC (SEE SHT B7GH).
15. CLEAR THE STOP FLIP-FLOP (SEE SHT B5GF).
16. LOAD THE MAR 10 THE START OF INITIALIZATION MICROCODE (SEE SHT B1GO).
17. INITIALIZATION 3A CC CLOCK-TO-CLOCK PHASE P3 (SEE SHT B8GD).

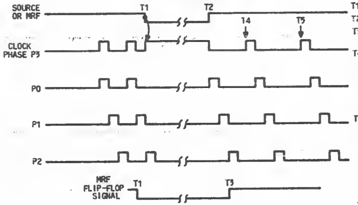
FUNCTIONS PERFORMED BY A STØP AND SWITCH OPERATION

18. INITIATE A SWITCH MESSAGE TO THE MCH.
19. SET THE STOP FLIP-FLOP.
20. CLEAR THE MICROINTERPRET FLIP-FLOP.

CIRCUIT OPERATION

(SEE SHEET B7CH)

TIMING DIAGRAM FOR MRF SEQUENCE



T1 - MRF OCCURS
T2-T1 - DURATION OF MRF SOURCE
T3-T1 - INTERVAL DURING WHICH MRF FUNCTIONS ARE PERFORMED
T4 - START OF MICROCYCLE THAT WILL ACCESS STARTING LOCATION OF MICROCODE INITIALIZATION SEQUENCE. FROM THIS POINT ON MICRO-PROGRAM CONTROL FINISHES INITIALIZATION.
T5 - FIRST MICROINSTRUCTION OF INITIALIZATION SEQUENCE IS EXECUTED

PART ØF FS 7
CØMPØSITE DIAGRAM B

3A CENTRAL CONTROL ②

DWG SIZE 6S
ISSUE 5A
BELL LABORATORIES
SD-1C900-01
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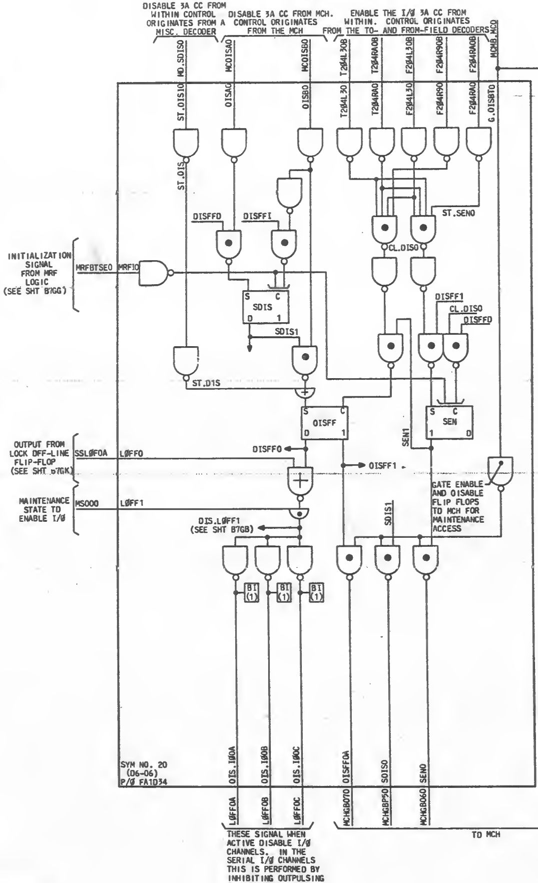
PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 9

I/O ENABLE AND DISABLE LOGIC

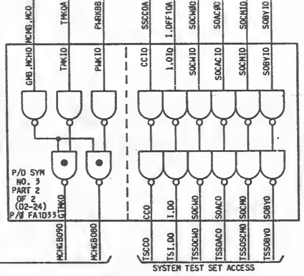

DISABLE 3A CC FROM WITHIN CONTROL ORIGINATES FROM A MISC. DECODER
DISABLE 3A CC FROM MCH. CONTROL ORIGINATES FROM THE MCH
ENABLE THE I/O 3A CC FROM WITHIN. CONTROL ORIGINATES FROM THE TO- AND FROM-FIELD DECODERS
MD.SDISO
MCOISAO
MCOISBO
T204L30B
T204RA0B
F204L30B
F204R90B
F204RA0B
MCMB.MCO
ST.OIS10
OISAO
OISBO
T204L30
T204RA0
F204L30
F204R90
F204RA0
G.OISBT0
ST.OIS
DISFFD
DISFFI
ST.SENO
CL.DISO
INITIALIZATION SIGNAL FROM MRF LOGIC (SEE SHT B7GG)
MRFBTSEO
MRFIO
S C SDIS D 1
SDIS1
DISFF1
CL.DISO
DISFFD
ST.DIS
S C OISFF D 1
S C SEN 1 D
SEN1
DISFF0
OISFF1
OUTPUT FROM LOCK OFF-LINE FLIP-FLOP (SEE SHT B7GK)
SSLOFOA
LOFF0
MAINTENANCE STATE TO ENABLE I/O
MS000
LOFF1
DIS.LOFF1 (SEE SHT B7GB)
GATE ENABLE AND DISABLE FLIP FLOPS TO MCH FOR MAINTENANCE ACCESS
SDIS1
BI (1)
BI (1)
BI (1)
SYM NO. 20 (D6-06) P/O FA1D34
OIS.I00A
OIS.I00B
OIS.I00C
OISFF0A
SOIS0
SEN0
LOFF0A
LOFF0B
LOFF0C
MCHGB070
MCHGBP50
MCHGB060
THESE SIGNAL WHEN ACTIVE DISABLE I/O CHANNELS. IN THE SERIAL I/O CHANNELS THIS IS PERFORMED BY INHIBITING OUTPULSING ON THE SERIAL LINK.
TO MCH

CIRCUIT OPERATION (CONT)

PART OF COMPOSITE DIAGRAM 10 SHOWS A SIMILAR FUNCTION OF GATING MAINTENANCE ACCESS INFORMATION TO THE MCH FOR THE TEST MODE KEY AND THE POWER KEY. THE OTHER PORTION OF COMPOSITE DIAGRAM 10 IS MERELY USED FOR BUFFERING SIGNALS THAT ARE SENT TO THE SYSTEM TEST SET. THIS PREVENTS ANY FAULT IN THE SYSTEM TEST SET FROM INADVERTENTLY CAUSING A 3A CC TO MALFUNCTION.

COMPOSITE DIAGRAM 10

MCH ACCESS LOGIC AND TEST SET ACCESS LOGIC



CIRCUIT OPERATION (CONT)

ON-LINE 3A CC. THE CLEARING OF THE MINT FLIP-FLOP PERFORMS A SIMILAR FUNCTION TO THE SETTING OF THE STOP FLIP-FLOP. THAT IS, BY CLEARING MINT FLIP-FLOP, ACCESS IS OBTAINED TO THE MACHINE THAT HAS BEEN STOPPED BY INHIBITING THE OUTPUT OF THE STORE INSTRUCTION REGISTER ONTO THE OUTPUT OF THE MICROSTORE. THUS, BY BEING IN THE STOP STATE AND NOT IN THE MICROINTERPRET MODE, THE OUTPUT OF THE MICROSTORE IS HELD TO THE ALL ZEROS. THEREFORE, THE MCH CAN ACCESS THE STOPPED 3A CC BY BRING ONTO THE CONTENTS OF THE MICROPROGRAM STORE OUTPUT. IN THIS MANNER, THE MCH CAN PERFORM MICROINSTRUCTIONS THAT WILL ENABLE THE VARIOUS REGISTERS OF THIS 3A CC TO BE GATED TO THE MCH.

THE FREEZE FLIP-FLOP IS RESET TO PERMIT THE CONTENTS OF THE MAR REGISTER TO BE HELD OR FROZEN IN THEIR PRESENT STATE. THIS FLIP-FLOP PERMITS THE MCH TO LOAD AN ARBITRARY ADDRESS INTO THE MAR AND FREEZE IT THERE. THEN ON A SUBSEQUENT MICROCYCLE, THE MAINTENANCE CHANNEL CAN READ THE CONTENTS OF THAT MICROPROGRAM ADDRESS AND HENCE, VERIFY THE CONTENTS OF ANY ARBITRARY LOCATION OF THE MICROPROGRAM STORE. THE FREEZE FLIP-FLOP PERFORMS ITS FUNCTION BY INHIBITING THE CLOCKING INTO THE MAR REGISTER (SEE SHEET B1GB). NOTE THAT FOR TEST PURPOSES TWO INPUTS CAN BE ADDED TOGETHER AND USED TO SET THE FREEZE FLIP-FLOP. THIS IS SOMETIMES USEFUL TO FREEZE A 3A CC MACHINE UNDER CERTAIN ERROR CONDITIONS.

ONE ADDITIONAL FUNCTION SHOWN IN COMPOSITE DIAGRAM 8 IS THE ORING OF THE STOP FLIP-FLOP TOGHETHER WITH THE FREEZE FLIP-FLOP. THIS SENDS A DC CONDITION TO THE MCH. THE OR OF THESE TWO STATES IS USED TO INDICATE TO THE MCH THAT IT CAN GAIN ACCESS TO A 3A CC THAT IS IN THIS STATE. OTHERWISE, THE MAINTENANCE CHANNEL CANNOT INTERPRET THE PROCESSING IN A 3A CC IF THESE CONDITIONS ARE NOT MET.

COMPOSITE DIAGRAM 9 SHOWS THE OPERATION OF THE I/O ENABLE AND DISABLE LOGIC. THIS LOGIC ALLOWS THE I/O CHANNELS TO EITHER BE ENABLED OR DISABLED FROM EITHER THE ON-LINE OR THE OFF-LINE 3A CC. THIS DISABLING OF AN I/O CHANNEL IS ACTUALLY PERFORMED BY THE DISABLE FLIP-FLOP WHICH INHIBITS THE CLOCKING TO ANY EQUIPPED I/O CHANNEL. NOTE THAT THE OUTPUT OF THE DISABLED FLIP-FLOP IS ACTUALLY ORED WITH THE LOCK OFF-LINE FLIP-FLOP BECAUSE BOTH OF THESE STATES PERFORM THE IDENTICAL OPERATION. NOTE THAT FOR MAINTENANCE PURPOSES A MAINTENANCE STATE SIGNAL PROVIDES THE ABILITY TO OVERRIDE THE PURPOSE OF THE LOCK OFF-LINE FLIP-FLOP OR DISABLE FLIP-FLOP SO THAT DIAGNOSTICS CAN BE PERFORMED ON A 3A CC THAT HAS BEEN DISABLED OR LOCKED OFF-LINE.

IT SHOULD FIRST BE NOTED THAT THE DISABLE FUNCTION IS CRITICAL IN ITS OPERATION. THEREFORE, IT IS IMPERATIVE THAT AN EXTERNAL SOURCE SUCH AS THE OTHER 3A CC NOT BE ABLE TO INADVERTENTLY DISABLE THE ON-LINE 3A CC. IN ORDER TO PREVENT THIS, THE STATE KNOWN AS THE "SEMI-DISABLE" STATE MUST BE SEQUENCED THROUGH BEFORE THE DISABLE FLIP-FLOP CAN BE SET. THEREFORE, IN ORDER TO DISABLE A 3A CC VIA THE MAINTENANCE CHANNEL, IT TAKES A 2-STEP OPERATION. THE SEMI-DISABLE FLIP-FLOP MUST BE SET WITH THE CONTROL LEAD MCDISA0. THEN ON A SUBSEQUENT MCH ORDER THE CONTROL FUNCTION CALLED MCDISB0 MUST BE EXECUTED BEFORE THE DISABLE FLIP-FLOP CAN BE SET. THE LEAD MD.SDISO PERMITS A 3A CC TO DISABLE ITSELF WITHOUT GOING THROUGH THIS TWO STEP SEQUENCE.

SIMILARLY, ONCE THE DISABLE FLIP-FLOP HAS BEEN SET, A SEQUENCE OF CONTROL OPERATIONS MUST BE PERFORMED TO CLEAR THE DISABLE FUNCTION. THIS PREVENTS AN INOPERATIVE 3A CC FROM ENABLING ITS OWN I/O INADVERTENTLY. THIS FUNCTION IS PERFORMED BY FIRST THE SETTING OF A "SEMI-ENABLE" FLIP-FLOP VIA A MISCELLANEOUS DECODER CROSSPOINT. THEN ON A SUBSEQUENT MICROCYCLE A MISCELLANEOUS DECODER CROSSPOINT THAT CLEARS THE DISABLE FLIP-FLOP WILL BE PERMITTED IF THE "SEMI-ENABLE" FLIP-FLOP HAS BEEN SET.

IN ORDER TO PROVIDE MAINTENANCE ACCESS TO TEST THE I/O ENABLE AND DISABLE LOGIC, A CONTROL SIGNAL IS PROVIDED FROM THE MCH THAT GATES THE STATE OF THE THREE FLIP-FLOPS INVOLVED IN THE MCH.

CIRCUIT OPERATION FOR COMPOSITE DIAGRAMS 8-10

COMPOSITE DIAGRAM 8 SHOWS THE LOGIC REQUIRED TO HARDWARE INITIALIZE THE 3A CC IN THE EVENT OF A MAINTENANCE RESET FUNCTION (MRF). THE SOURCES OF MRF'S AS WELL AS THE FUNCTIONS THAT ARE PERFORMED WHEN AN MRF OCCURS ARE DESCRIBED BY THE INDIVIDUAL NOTES ATTACHED TO EACH OF THE LOGICAL GATES SHOWN IN COMPOSITE DIAGRAM B. NOTE THAT ALL MRF'S WITH THE EXCEPTION OF ONE DO ESSENTIALLY THE SAME FUNCTIONAL OPERATION. THEY SET THE MRF FLIP-FLOP, AND THE MRF FLIP-FLOP IN TURN INITIALIZES A NUMBER OF KEY FLIP-FLOPS IN A 3A CC. IN ADDITION, THE SIGNAL THAT INITIATES THE MRF, AND HENCE, SETS THE MRF FLIP-FLOP, IS USED TO DIRECTLY INITIALIZE THE 3A CC CLOCK TO CLOCK PHASE P3. WHEN THE SOURCE OF THE MRF BECOMES INACTIVE, THE CLOCK IS ALLOWED TO START. THUS STARTING AT P3, THE CLOCK WILL GO THROUGH CLOCK PHASES P0, P1, AND P2 BEFORE THE MFR FLIP-FLOP IS CLEARED. AT THAT POINT IN TIME THE 3A CC IS "HARDWARE INITIALIZED" AND A SEQUENCE OF MICROCODE WILL TAKE OVER TO CONTINUE INITIALIZATION. THE STARTING ADDRESS OF THIS SEQUENCE OF MICROCODE IS JAMMED INTO THE MAR BY ONE OF THE OUTPUTS OF THE MRF FLIP-FLOP. THIS STARTING MICROCODE ADDRESS FOR THE MRF INITIALIZATION IS 0 (0277).

THE MRF INPUT FROM THE MAINTENANCE CHANNEL (MCH) PERFORMS ONE ADDITIONAL FUNCTION. IT SETS A FLIP-FLOP CALLED IMRFMCH. THE PURPOSE OF THIS FLIP-FLOP IS TO PREVENT A MRF ORIGINATED FROM THE THE MAINTENANCE CHANNEL FROM BEING RETURNED IMMEDIATELY TO THE MAINTENANCE CHANNEL, AND HENCE, INITIALIZING THE SOURCE OF THE MRF. NOTE THAT THE IMRFMCH FLIP-FLOP WILL BE CLEARED BY A MISCELLANEOUS DECODER CROSSPOINT SIGNAL ACTIVATED WITHIN THE MICROCODE INITIALIZATION SEQUENCE.

ANOTHER COMMENT ABOUT THE SOURCES OF AN MRF IS THAT THE MRF ORIGINATING FROM THE RESET-CIRCUIT KEY OF THE 3A CC CONTROL PANEL, ALTHOUGH IT PERFORMS THE SAME INITIALIZATION HARDWARE SEQUENCE, IS HANDLED SLIGHTLY DIFFERENT BY THE MICROCODE INITIALIZATION. THAT IS, WHEN A RESET-CIRCUIT FUNCTION OCCURS, IT SETS THE RESET-CIRCUITS FLIP-FLOP AS SHOWN ON COMPOSITE DIAGRAM 2. THE FLIP-FLOP IS TESTED BY THE MICROCODE DURING ITS INITIALIZATION SEQUENCE. IF IT IS FOUND TO BE SET THE MICROPROGRAM CONTROL, TRANSFERS TO THE PANEL-HALT LOOP GIVING CONTROL TO THE 3A CC PANEL FUNCTIONS. ALL OTHER MRF'S BYPASS THIS PANEL-HALT LOOP. THEY WILL USUALLY TEST THE ISC BITS IN THE SYSTEM STATUS (SS) REGISTER TO DETERMINE WHAT TYPE OF INITIALIZATION IS TO TAKE PLACE. THAT IS, 1) WHETHER THE 3A CC INITIALIZING IS TO BE PUT ON-LINE, OR 2) TO STOP-AND SWITCH IN AN ATTEMPT TO HAVE THE OTHER 3A CC GO ON-LINE, OR 3) TO TRANSFER TO AN IPL (INITIALIZATION PROGRAM LOAD) SEQUENCE THAT WILL RELOAD THE CONTENTS THE MAS IN AN ATTEMPT TO ESTABLISH A GOOD PROGRAM STORE FROM WHICH TO EXECUTE CODE.

THIS DECISION, WHETHER TO INITIALIZE THE ON-LINE 3A CC OR TO STOP-AND-SWITCH TO THE OFF-LINE, IS PERFORMED BY MICROCODE IN THE INITIALIZATION SEQUENCE OF THE MRF FUNCTION. HOWEVER, THERE ARE OTHER CASES WHERE THE HARDWARE ITSELF DETERMINES THAT A STOP-AND-SWITCH FUNCTION IS THE ONLY VIABLE METHOD OF RECOVERING THE SYSTEM. THIS FUNCTION IS ACTIVATED WHENEVER BITS 0 THROUGH 9 OF THE ERROR REGISTER (ER) ARE SET AND THE BLOCK HARDWARE CHECK BIT IS NOT SET. THESE ERRORS ARE KNOWN AS FATAL ERRORS AND WILL INITIATE A STOP-AND-SWITCH FUNCTION. SIMILARLY, IF THE PROGRAM TIMER HAS REACHED THE FIRST TIME-OUT COUNT (BIT 14 OF TI=1) A STOP-AND-SWITCH FUNCTION WILL OCCUR. AS SHOWN, BOTH OF THESE FUNCTIONS THAT STOP-AND-SWITCH ARE ORED TOGETHER AND WILL ALWAYS CAUSE A STOP-AND-SWITCH TO OCCUR UNLESS A GIVEN 3A CC IS LOCKED ON-LINE. IN THIS CASE, THE ONLY ALTERNATIVE IS TO INITIALIZE THE ON-LINE MACHINE. NOTE ALSO THAT THE SOFTWARE IS GIVEN THE CAPABILITY OF PERFORMING THIS STOP-AND-SWITCH FUNCTION IF IT HAS DETERMINED THAT AN INVALID SYSTEM STATE HAS OCCURED, AND THEREFORE, A STOP-AND-SWITCH IS REQUIRED. THIS STOP-AND-SWITCH FUNCTION IS INPUTTED ON THE SAME NET AS THE FIRST PROGRAM TIMER TIMEOUT ON THE NET MD.STSW0 (SEE NOTE 7). AS INDICATED IN COMPOSITE DIAGRAM B, WHEN A STOP-AND-SWITCH FUNCTION OCCURS THREE MAJOR OPERATIONS OCCUR: 1) THE SWITCH SIGNAL IS SENT TO THE MAINTENANCE CHANNEL; 2) THE STOP FLIP-FLOP IS SET: AND 3) THE MICROINTERPRET (MINT) FLIP-FLOP IS CLEARED. THE SETTING OF THE STOP FLIP-FLOP IS USED TO KEEP THE 3A CC, THAT HAS JUST TERMINATED INSTRUCTION EXECUTION, IN A STATE WHERE IT CAN BE EASILY INTERROGATED BY THE NEWLY

PART OF FS 7
COMPOSITE DIAGRAM 9,10

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B7GH

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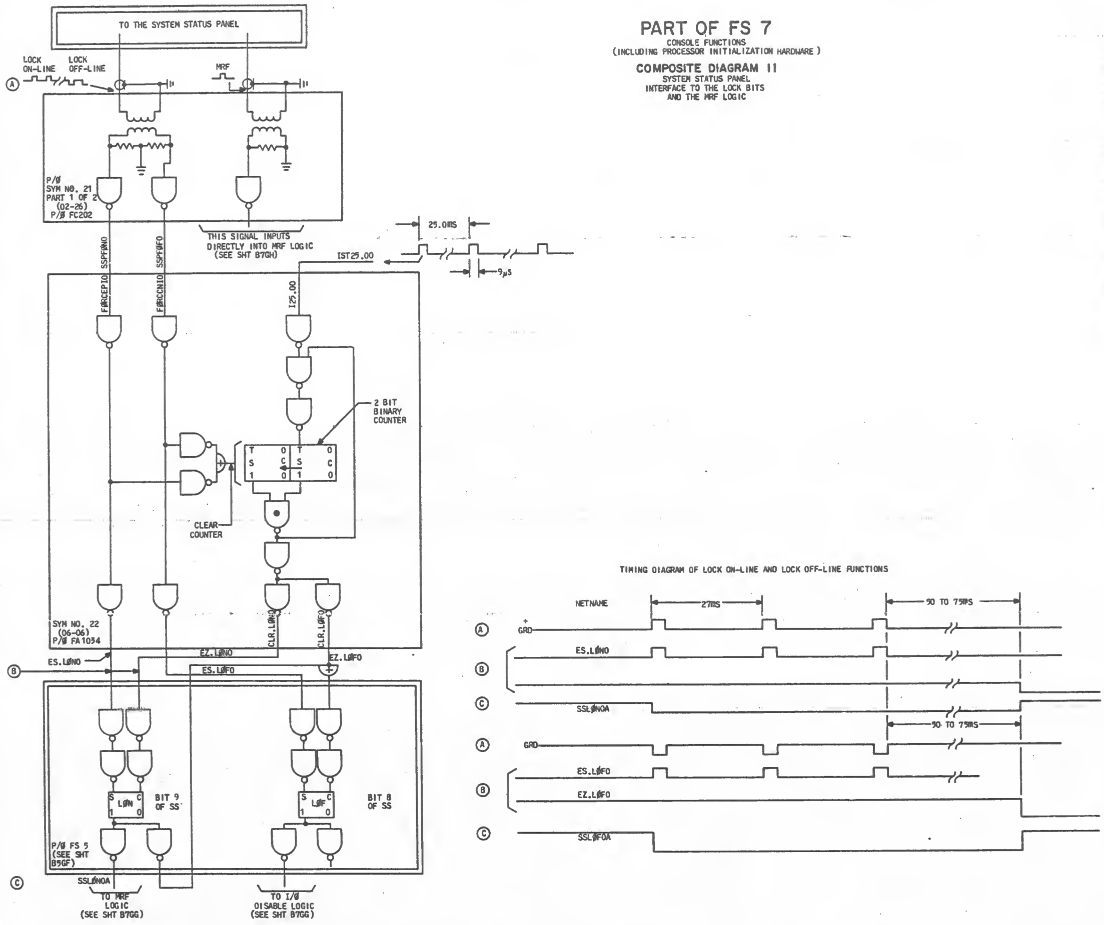
E-7021 (12-73)

PART OF FS 7

CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 11

SYSTEM STATUS PANEL
INTERFACE TO THE LOCK BITS
AND THE MRF LOGIC



TIMING DIAGRAM OF LOCK ON-LINE AND LOCK OFF-LINE FUNCTIONS

CIRCUIT OPERATION

COMPOSITE DIAGRAM 11 SHOWS THE SYSTEM STATUS PANEL INTERFACE FOR THE LOCK FUNCTIONS AND THE MRF FUNCTION. ALL OTHER COMMUNICATION WITH THE SYSTEM STATUS PANEL IS PERFORMED OVER A STANDARD I/Ø SERIAL CHANNEL. IF A MRF IS INITIATED BY THE SYSTEM STATUS PANEL, A SINGLE PULSE ENTERS VIA THE TRANSFORMER SHOWN ON SYMBOL 21, AND THIS IN TURN, PULSES THE INPUT TO THE MRF LOGIC AS SHOWN IN COMPOSITE DIAGRAM 8 AND AS SUCH OPERATES THE SAME AS ALL OTHER MRF SOURCES.

IF THE SYSTEM STATUS PANEL IS TO LOCK A 3A CC ON-LINE, IT PULSES WITH A POSITIVE POLARITY PULSE AS SHOWN ON THE TRANSFORMER INPUT ON SYMBOL 21. THIS POSITIVE PULSE, IN TURN, RESULTS IN THE NET SSPFØNO TO BE ACTIVE AND THE OTHER NET SSPFØFO TO BE INACTIVE. THE SSPFØNO SIGNAL IS JUST DOUBLE INVERTED THROUGH SYMBOL 22 AND PERFORMS A DIRECT SET FUNCTION ON THE LOCK ON-LINE FLIP-FLOP IN THE SS REGISTER. NOTE THAT THE LOCK ON-LINE FUNCTION THAT INPUTS INTO THE TRANSFORMERS IS PROVIDED BY A STEADY STREAM OF PULSE INPUTS. IF THIS STREAM OF INPUT PULSING TERMINATES, THE 2-BIT BINARY COUNTER IN SYMBOL 22 STOPS BEING HELD CLEAR BY THE LOCK ON-LINE FUNCTION. THIS TIMER WILL TIME-OUT IN APPROXIMATELY 50 TO 75ms AND WILL THEN CLEAR THE LOCK ON-LINE FUNCTION. THE LOCK OFF-LINE FUNCTION WORKS IN A SIMILAR MANNER EXCEPT THAT A NEGATIVE POLARITY PULSE TRAIN IS REQUIRED TO THE INPUT OF THE TRANSFORMER IN SYMBOL 21. THIS IN TURN CAUSES THE NET SSPFØFO TO BE ACTIVE AND THE NET SSPFØNO TO BE INACTIVE. THE RESULT IS TO SET THE LOCK OFF-LINE FLIP-FLOP. SIMILARLY, IF THE NEGATIVE PULSING ON THE LOCK OFF-LINE INPUT TO THE TRANSFORMER STOPS, THE 2-BIT BINARY COUNTER IN SYMBOL 22 WILL TIME OUT AND CLEAR THE LOCK OFF-LINE FUNCTION. TO GUARANTEE THAT LOCK ON-LINE AND LOCK OFF-LINE CANNOT OCCUR SIMULTANEOUSLY, THE OUTPUT OF THE LOCK OFF-LINE FLIP-FLOP IS USED TO CLEAR THE LOCK OFF-LINE FLIP-FLOP WITH THE CONTROL NET EZ.LØFO.

PART ØF FS 7
CØMPØSITE DIAGRAM 11

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
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PART OF FS 7

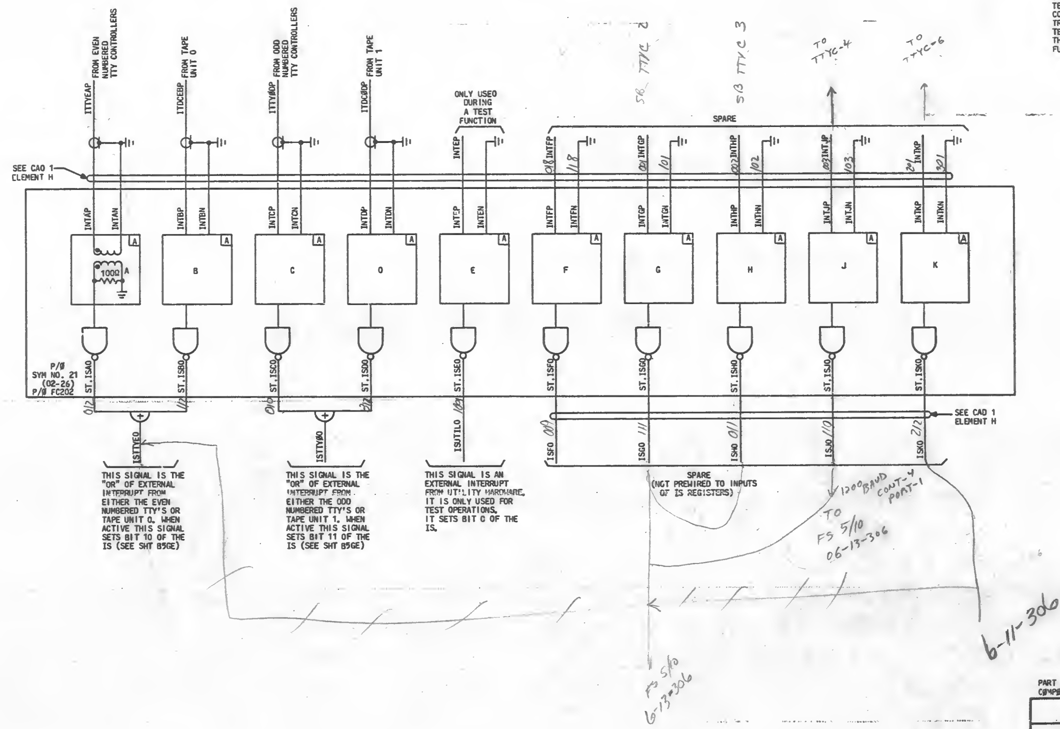
CONSOLE FUNCTIONS
(INCLUDING PROCESSOR INITIALIZATION HARDWARE)

COMPOSITE DIAGRAM 12

TRANSFORMER INSULATION ON EXTERNAL INTERRUPTS

CIRCUIT OPERATION

COMPOSITE OIAGRAM 12 SHOWS THE TRANSFORMERS THAT ARE USED TO ISOLATE EXTERNAL INTERRUPT INPUTS FROM THE INTERRUPT SET REGISTER INPUTS. NOTE THAT THE INPUT TRANSFORMERS A THROUGH E ARE PRESENTLY USED AND F THROUGH K ARE SPARE ANO AVAILABLE FOR GROWTH. ALSO TRANSFORMERS A AND B HAVE THEIR OUTPUTS TIED TOGETHER TO SET THE SAME BIT OF THE IS REGISTER. AS INDICATEO, THIS RESULTS IN HAVING THE EVEN NUMBERED TTY CONTROLLERS AND THE INTERRUPT FROM TAPE UNIT 0 TO SET BIT 10 OF THE IS REGISTER. SIMILARLY, THE INTERRUPT FROM THE ODD NUMBERED TTY CONTROLLERS AND TAPE UNIT 1 SET INTERRUPT BIT 11. INTERRUPT TRANSFORMER E IS USED ONLY FOR TEST PURPOSES AND SETS INTERRUPT BIT 0. IT IS USUALLY USED FOR TEST SET CONNECTIONS THAT SET THE HIGHEST LEVEL INTERRUPT TO PERFORM UTILITY FUNCTIONS VIA AN INTERRUPT MOOE.



THIS SIGNAL IS THE "OR" OF EXTERNAL INTERRUPT FROM EITHER THE EVEN NUMBERED TTY'S OR TAPE UNIT 0. WHEN ACTIVE THIS SIGNAL SETS BIT 10 OF THE IS (SEE SHT B5GE)

THIS SIGNAL IS THE "OR" OF EXTERNAL INTERRUPT FROM EITHER THE ODD NUMBERED TTY'S OR TAPE UNIT 1. WHEN ACTIVE THIS SIGNAL SETS BIT 11 OF THE IS (SEE SHT B5GE)

THIS SIGNAL IS AN EXTERNAL INTERRUPT FROM UTILITY HARDWARE. IT IS ONLY USED FOR TEST OPERATIONS. IT SETS BIT 0 OF THE IS.

SPARE
(NOT PREWIRED TO INPUTS OF IS REGISTERS)

PART ØF FS 7
CØMPØSITE OIAGRAM 12

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B7GK

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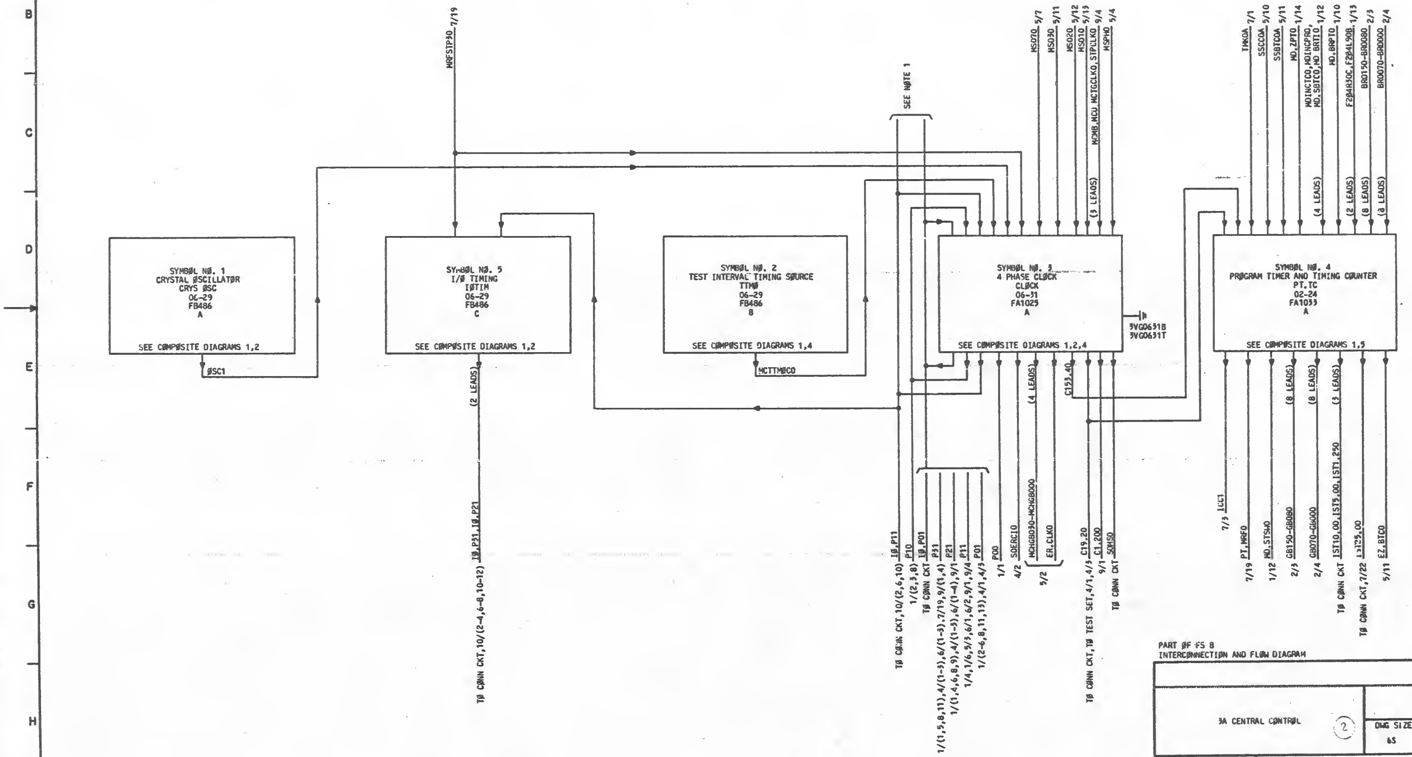
PART OF FS 8

CLØCK, PRØGRAM TIMER AND TIMING CØUNTER
INTERCØNNECTIØN AND FLØW DIAGRAM

NOTES:

1. LEADS SHØWN CØULD FUNCTIØN AS EITHER ØUTPUTS ØR INPUTS (ØI). ALL ØFF-PAGE REFERENCING WILL BE SHØWN ØN ØUTPUT LEAD.
2. FØR TO-AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.



PART ØF FS 8
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B8AA

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E-7821 (12-73)

PART OF FS 8

CLOCK, PROGRAM TIMER AND TIMING COUNTER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
BR0000-BR0150	BITS 0-15 OF THE BR REGISTER (COPY 0)
C1.200	CLOCK PULSE OF 1.2 USEC
C153.40	CLOCK PULSE OF 153.4 USEC
C19.20	CLOCK PULSE OF 19.20 USEC
ER.CLK0	CLOCK ERROR
EZ.BTC0	ENABLE ZEROING OF BLOCK TIMER CHECK FLIP-FLOP
GB000-GB150	BITS 0-15 OF THE GATING BUS
ICC1	OUTPUT OF CC FLIP-FLOP [ICI
IO.P01	P0 CLOCK TO THE IO CHANNELS
IO.P11	P1 CLOCK TO THE IO CHANNELS
IO.P21	P2 CLOCK TO THE IO CHANNELS
IO.P31	P3 CLOCK TO THE IO CHANNELS
IST1.250	1.25 MILLISECOND INTERRUPT SET INPUT
IST10.00	10-MILLISECOND INTERRUPT SET
IST25.00	25-MILLISECOND INTERRUPT SET
IST5.00	5-MILLISECOND INTERRUPT SET
MCHGB000-MCHGB030	GATED OUTPUTS OF CLOCK PHASES P0-P3 TO MAINTENANCE CHANNEL SHIFT REGISTER (MCHTR) (SEE MCMB.MCO BELOW.)
MCMB.MC0	MCA CONTROL, LOAD THE MISC. BITS REGISTER INTO THE MCA SHIFT REGISTER (MCHTR)
MCTGCLK0	TOGGLE THE CLOCK SIGNAL
MCTTMOC0	TEST MODE CONTROL FOR CRYSTAL OSCILLATOR
MD.BRPT0	MISC. DECODER CONTROL, GATE THE BR(8-15) TO THE PT REGISTER (BITS 8-15 OF TI)
MD.BRTI0	MISC. DECODER, GATE BR REGISTER TO THE TIMING REGISTER
MD.SBTC0	MISC. DECODER, SET BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)
MD.STSW0	MISC. DECODER CONTROL, STOP 3A CC AND SWITCH TO THE OTHER 3A CC
MD.ZPT0	MISC. DECODER, ZERO THE PROGRAM TIMER
MDINCPR0	MISC. DECODER, INCREMENT THE PRE-SCALER
MDINCTC0	MISC. DECODER, INCREMENT THE TC
MRFSTP30	CENTRAL CONTROL MAINTENANCE RESET FUNCTION (MRF) SET CLOCK TO PHASE P3
MSPH0	PARITY HIGH OF MAINTENANCE STATE REGISTER
MS010	BIT 1 OF MAINTENANCE STATE REGISTER (CLOCK TEST)
MS020	BIT 2 MAINTENANCE STATE REGISTER (CLOCK TEST)
MS030	BIT 3 MAINTENANCE STATE REGISTER (CLOCK TEST)
MS070	BIT 7 MAINTENANCE STATE REGISTER (ACTIVATE MY STORE)
OSC1	OUTPUT OF CRYSTAL OSCILLATOR
PT.MRF0	PROGRAM TIMER TIMEOUT, INITIATE A MAINTENANCE RESET FUNCTION

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
P00	CLOCK PHASE P0 (GROUND ACTIVE)
P01	CLOCK PHASE P1 (POSITIVE ACTIVE)
P10	CLOCK PHASE P1 (GROUND ACTIVE)
P11	CLOCK PHASE P1 (POSITIVE ACTIVE)
P21	CLOCK PHASE P2 (POSITIVE ACTIVE)
P31	CLOCK PHASE P3 (POSITIVE ACTIVE)
SSBTC0A	BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)
SSCC0A	CENTRAL CONTROL BIT (BIT 12 OF THE SS)
STPCLK0	STOP CLOCK CONTROL
S0ERCI0	MY MAIN STORE BUS ERROR SIGNAL C INPUT
S0MS0	MAINTENANCE STATE (PH OF MS) TO MY STORE (ENABLE I/O CHANNEL FROM OTHER CC)
TMK0A	PANEL TEST MODE REVERSAL KEY

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 4A

BELL LABORATORIES

B8AB

09/02/76

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PART OF FS 8

CLOCK,PROGRAM TIMER AND TIMING COUNTER

SYMBOL NO. 1

CRYSTAL OSCILLATOR

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CRYS OSC	06-29	FB486	A	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
OSC1	0	013	8/3		OSC1	2G5
3T058F	GRD	200		203	GRD	2G1
	GRD	2GD		203		
	GRD	0GD		203		
	GRD	219		203	GRD	2G1
3V058F	PWR	019		203		
	PWR	000		203	+3	2G1
5V061A	PWR	210		203		2G5
	PWR	010		203		2G4

SYMBOL NO. 2

TEST INTERVAL TIMING SOURCE

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TTMO	06-29	FB486	B	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MCTTMOCO	0	214	8/3		TTMOCO	2G4

SYMBOL NO. 3

4 PHASE CLOCK

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CLOCK	06-31	FA1025	A	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		309			MT10	7A5
		108			INVA1	6H6
		203			CTR70	7H4
		003			CTR80	7H2
		109			P30	3H8
		308			P20	3H6
		208			INVAI0	6A6
C1.200	0	305	9/1		CTR20	8H4
C153.40	0	302	8/4		CTR90	7H1
C19.20	0	103	4/1,4/3		CTR60	7H6
			8/4			
			TO CONN CKT			
ER.CLKO	0	107	5/2		CLERO	4H7
IO.P01	OI	218	TO CONN CKT		P0B1	3H1
IO.P11	OI	010	8/5,10/2		P1B1	3H4
			10/6,10/10			
			TO CONN CKT			
MCHGB000	OT	005	5/2	202	GP00	5H0
MCHGB010	OT	304	5/2	202	GP10	5H1

SYMBOL NO. 3 (CONT)

4 PHASE CLOCK

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CLOCK	06-31	FA1025	A	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MCHGB020	OT	104	5/2	202	GP20	5H1
MCHGB030	OT	204	5/2	202	GP30	5H2
MCMB.MCO	I	007	9/4		CM30	5A0
MCTGCLKO	I	001	9/4		CM40	2A5
MCTTMOCO	I	002	8/2		TTMOCO	6A4
MRFSTP30	I	008	7/19		CCTO	8A5
	I	202			INITO	2A3
MSPHO	I	206	5/4	202	INVBIO	6A8
MS010	I	301	5/13		CM00	5A3
MS020	I	101	5/12		CM10	5A5
MS030	I	201	5/11		CM20	5A4
MS070	I	106	5/7		RESO	6A7
OSC1	I	219	8/1		OSCIO	2A4
P00	0	209	1/1		P00	3H2
P01	OI	318	1/2,1/3		P0A1	3H0
			1/4,1/5			
			1/6,1/8			
			1/11,1/13			
			4/1,4/3			
P10	0	009	1/2,1/3		P10	3H4
			1/8			
	I	207			TCT1	8A1
P11	OI	111	1/4,1/6		P1A1	3H3
			5/3,6/1			
			6/2,9/1			
			9/4			
P21	OI	018	1/1,1/4		P2A1	3H5
			1/6,1/8			
			1/9,4/1			
			4/2,4/3			
			6/1,6/2			
			6/3,6/4			
			9/1			
P31	OI	211	1/1,1/5		P3A1	3H7
			1/8,1/11			
			4/1,4/2			
			4/3,6/1			
			6/2,6/3			
			7/19,9/1			
			9/4			
STPCLKO	I	300	9/4		STPCLKO	2A1
SOERCI0	0	006	4/2		RESIO	6H7
SOMSO	0	306	TO CONN CKT		INVB00	6H8
3T058F	GRD	0GD		203	GRD	
	GRD	319		203	GRD	
	GRD	200		203	GRD	
	GRD	2GD		203	GRD	
3VG0631B	GRD	102			GRD102	2H1
	GRD	205			GRD205	2H1
	GRD	200			GRD	
	GRD	307			GRD307	2H0
3VG0631T	GRD	217			GRD217	2H0
	GRD	212			GRD212	2H0
	GRD	319			GRD	
	GRD	017			GRD017	2H1
	GRD	012			GRD012	2H1
	GRD	114			GRD114	2H1
	GRD	314			GRD314	2H0
3V058F	PWR	119		203	+3	
	PWR	000		203	+3	

SYMBOL NO. 4

PROGRAM TIMER AND TIMING COUNTER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PT.TC	02-24	FA1033	A	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		102			GRD102	2H6
		300			CLR.C100	7A7
		302			TC250	7H5
		002			T125	7H0
BR0000	I	010	2/4	202	BR000	5A6
BR0010	I	210	2/4	202	BR010	5A5
BR0020	I	110	2/4	202	BR020	5A3
BR0030	I	310	2/4	202	BR030	5A2
BR0040	I	011	2/4	202	BR040	4A6
BR0050	I	211	2/4	202	BR050	4A4
BR0060	I	111	2/4	202	BR060	4A3
BR0070	I	311	2/4	202	BR070	4A1
BR0080	I	112	2/3	202	BR080	3A6
BR0090	I	312	2/3	202	BR090	3A5
BR0100	I	013	2/3	202	BR100	3A3
BR0110	I	213	2/3	202	BR110	3A2
BR0120	I	117	2/3	202	BR120	2A8
BR0130	I	317	2/3	202	BR130	2A6
BR0140	I	018	2/3	202	BR140	2A5
BR0150	I	218	2/3	202	BR150	2A4
C153.40	I	009	8/3		C15410	9A7
C19.20	I	309	8/3		C1910	6F1
E2.BTCO	0	202	5/11		CLR.BTCO	8G5
F204L90B	I	318	1/13		F204L90	2A3
F204R30C	I	118	1/13		F204R30	2A3
GB000	OT	105	2/4		TC.GB000	5G6
GB010	OT	207	2/4		TC.GB010	5G5
GB020	OT	007	2/4		TC.GB020	5G3
GB030	OT	306	2/4		TC.GB030	5G2
GB040	OT	106	2/4		TC.GB040	4H6
GB050	OT	206	2/4		TC.GB050	4H4
GB060	OT	006	2/4		TC.GB060	4H3
GB070	OT	305	2/4		TC.GB070	4H1
GB080	OT	315	2/3		PT.GB080	3G6
GB090	OT	115	2/3		PT.GB090	3G5
GB100	OT	215	2/3		PT.GB100	3G3
GB110	OT	015	2/3		PT.GB110	3G2
GB120	OT	214	2/3		PT.GB120	2H8
GB130	OT	014	2/3		PT.GB130	2H7
GB140	OT	313	2/3		PT.GB140	2H5
GB150	OT	113	2/3		PT.GB150	2H4
ICC1	0	IC	7/3		CC1	2H1
IST1.250	0	004	TO CONN CKT		I1.250	7H2
IST10.00	0	201	TO CONN CKT		I10.00	7H6
IST25.00	0	204	7/22		I25.00	7H4
			TO CONN CKT			
IST5.00	0	308	TO CONN CKT		I5.00	7H5
MO.BRPTO	I	001	1/10		BR.PTIO	6C1
MO.BRTIO	I	116	1/12		BR.TIIO	6C1
MO.SBTCO	I	209	1/12		CL.TTOIO	8A2
MO.STSWO	OT	008	1/12		STP.SWO	2H5
MO.ZPTO	I	016	1/14		CLR.PTIO	2A4
MOINCPRO	I	109	1/12		INCPSCIO	6F1
MOINCTCO	I	316	1/12		INCTCIO	5A7
PT.MRFO	0	208	7/19		THD.INTO	2H4
SSBTCOA	I	019	5/11	202	BTCIO	2A2
SSCCOA	I	219	5/10		CCIO	2A1
TMKOA	I	106	7/1		INHPTIO	2A2

SYMBOL NO. 4 (CONT)

PROGRAM TIMER AND TIMING COUNTER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PT.TC	02-24	FA1033	A	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T054C	GRD	2GD		203	GRD	
3T054C	GRD	0GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3V054C	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 5

I/O TIMING

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOTIM	06-29	FB486	C	

---------------------- FS INFO ---------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		001			IOP31B	2G7
		004			IOP21B	2G6
IO.P11	I	209	8/3		P1B1	2A6
IO.P21	0	207	10/2,10/3		IOP21A	2G6
			10/4,10/6			
			10/7,10/8			
			10/10,10/11			
			10/12			
			TO CONN CKT			
IO.P31	0	205	10/2,10/3		IOP31A	2G7
			10/4,10/6			
			10/7,10/8			
			10/10,10/11			
			10/12			
			TO CONN CKT			
MRFSTP30	I	002	7/19		INITO	2A6

PART OF FS 8
SYMBOL(S) 1 2 3 4 5

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	B8CA

PRINTED IN U. S. A.

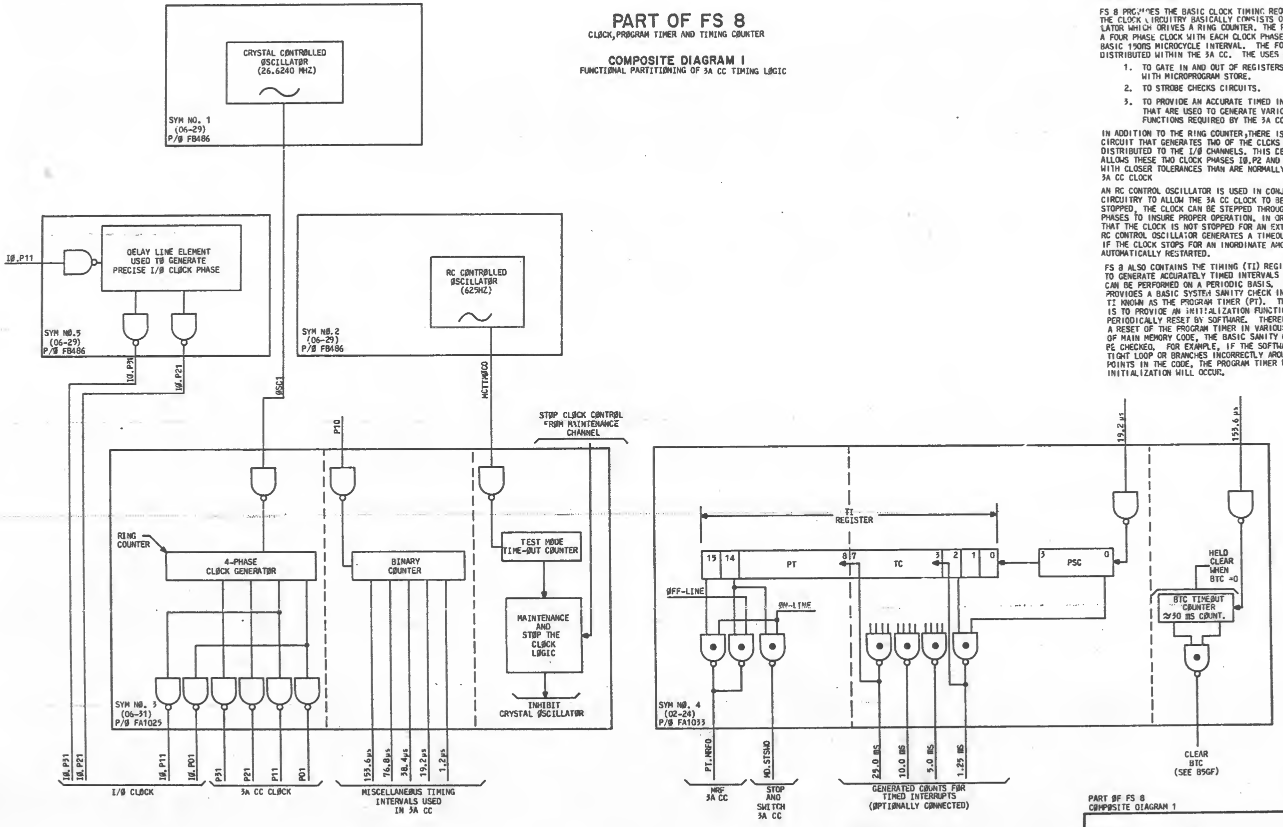
12/13/76

PART OF FS 8

CLOCK, PROGRAM TIMER AND TIMING COUNTER

COMPOSITE DIAGRAM I

FUNCTIONAL PARTITIONING OF 3A CC TIMING LOGIC



CRYSTAL CONTROLLED OSCILLATOR (26.6240 MHZ)
SYM NO. 1 (06-29) P/O FB486
IO.P11
DELAY LINE ELEMENT USED TO GENERATE PRECISE I/O CLOCK PHASE
SYM NO.5 (06-29) P/O FB486
RC CONTROLLED OSCILLATOR (625HZ)
SYM NO.2 (06-29) P/O FB486
IO.P31
IO.P21
OSC1
MCTTMOCO
P10
STOP CLOCK CONTROL FROM MAINTENANCE CHANNEL
RING COUNTER
4-PHASE CLOCK GENERATOR
BINARY COUNTER
TEST MODE TIME-OUT COUNTER
MAINTENANCE AND STOP THE CLOCK LOGIC
INHIBIT CRYSTAL OSCILLATOR
SYM NO. 3 (06-31) P/O FA1025
IO.P31
IO.P21
IO.P11
IO.P01
P31
P21
P11
P01
I/O CLOCK
3A CC CLOCK
153.6μs
76.8μs
38.4μs
19.2μs
1.2μs
MISCELLANEOUS TIMING INTERVALS USED IN 3A CC
TI REGISTER
15
14
PT
8
7
TC
3
2
1
0
3
PSC
0
OFF-LINE
ON-LINE
19.2 μs
153.6 μs
HELD CLEAR WHEN BTC =0
BTC TIMEOUT COUNTER ≈30 mS COUNT.
SYM NO. 4 (02-24) P/O FA1033
PT.NRFO
MO.STSMO
25.0 MS
10.0 MS
5.0 MS
1.25 MS
NRF 3A CC
STOP AND SWITCH 3A CC
GENERATED COUNTS FOR TIMED INTERRUPTS (OPTIONALLY CONNECTED)
CLEAR BTC (SEE B5GF)

CIRCUIT OPERATION

FS 8 PROVIDES THE BASIC CLOCK TIMING REQUIRED FOR THE 3A CC THE CLOCK CIRCUITRY BASICALLY CONSISTS OF A CRYATAL OSCILLATOR WHICH DRIVES A RING COUNTER. THE RING COUNTER GENERATES A FOUR PHASE CLOCK WITH EACH CLOCK PHASE ONE- QUARTER OF THE BASIC 150nS MICROCYCLE INTERVAL. THE FOUR CLOCK PHASES ARE DISTRIBUTED WITHIN THE 3A CC. THE USES OF THE CLOCK ARE:

1. TO GATE IN AND OUT OF REGISTERS ASSOCIATED WITH MICROPROGRAM STORE.
2. TO STROBE CHECKS CIRCUITS.
3. TO PROVIDE AN ACCURATE TIMED INPUT TO COUNTERS THAT ARE USED TO GENERATE VARIOUS TIMED INTERVAL FUNCTIONS REQUIRED BY THE 3A CC.

IN ADDITION TO THE RING COUNTER, THERE IS ALSO A DELAY LINE CIRCUIT THAT GENERATES TWO OF THE CLCKS PHASES THAT ARE DISTRIBUTED TO THE I/O CHANNELS. THIS DELAY LINE ELEMENT ALLOWS THESE TWO CLOCK PHASES IO.P2 AND IO.P3 TO BE GENERATED WITH CLOSER TOLERANCES THAN ARE NORMALLY REQUIRED FOR THE 3A CC CLOCK

AN RC CONTROL OSCILLATOR IS USED IN CONJUNCTION WITH TEST CIRCUITRY TO ALLOW THE 3A CC CLOCK TO BE STOPPED. WHEN STOPPED, THE CLOCK CAN BE STEPPED THROUGH ITS VARIOUS CLOCK PHASES TO INSURE PROPER OPERATION. IN ORDER TO GUARANTEE THAT THE CLOCK IS NOT STOPPED FOR AN EXTENDED PERIOD, THE RC CONTROL OSCILLATOR GENERATES A TIMEOUT INTERVAL, SO THAT IF THE CLOCK STOPS FOR AN INORDINATE AMOUNT OF TIME IT WILL AUTOMATICALLY RESTARTED.

FS 8 ALSO CONTAINS THE TIMING (TI) REGISTER WHICH IS USED TO GENERATE ACCURATELY TIMED INTERVALS SO THAT FUNCTIONS CAN BE PERFORMED ON A PERIODIC BASIS. IN ADDITION, THE TI PROVIDES A BASIC SYSTEM SANITY CHECK IN THE PORTION OF A TI KNOWN AS THE PROGRAM TIMER (PT). THE PURPOSE OF THE PT IS TO PROVIDE AN INITIALIZATION FUNCTION IF IT IS NOT PERIODICALLY RESET BY SOFTWARE. THEREFORE, BY INSERTING A RESET OF THE PROGRAM TIMER IN VARIOUS STRATEGIC POINTS OF MAIN MEMORY CODE, THE BASIC SANITY OF THE SOFTWARE CAN BE CHECKED. FOR EXAMPLE, IF THE SOFTWARE REMAINS IN A TIGHT LOOP OR BRANCHES INCORRECTLY AROUND ONE OF THESE POINTS IN THE CODE, THE PROGRAM TIMER WILL TIME OUT AND AN INITIALIZATION WILL OCCUR.

PART OF FS 8
COMPOSITE DIAGRAM 1

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B8GA

PART OF FS 8

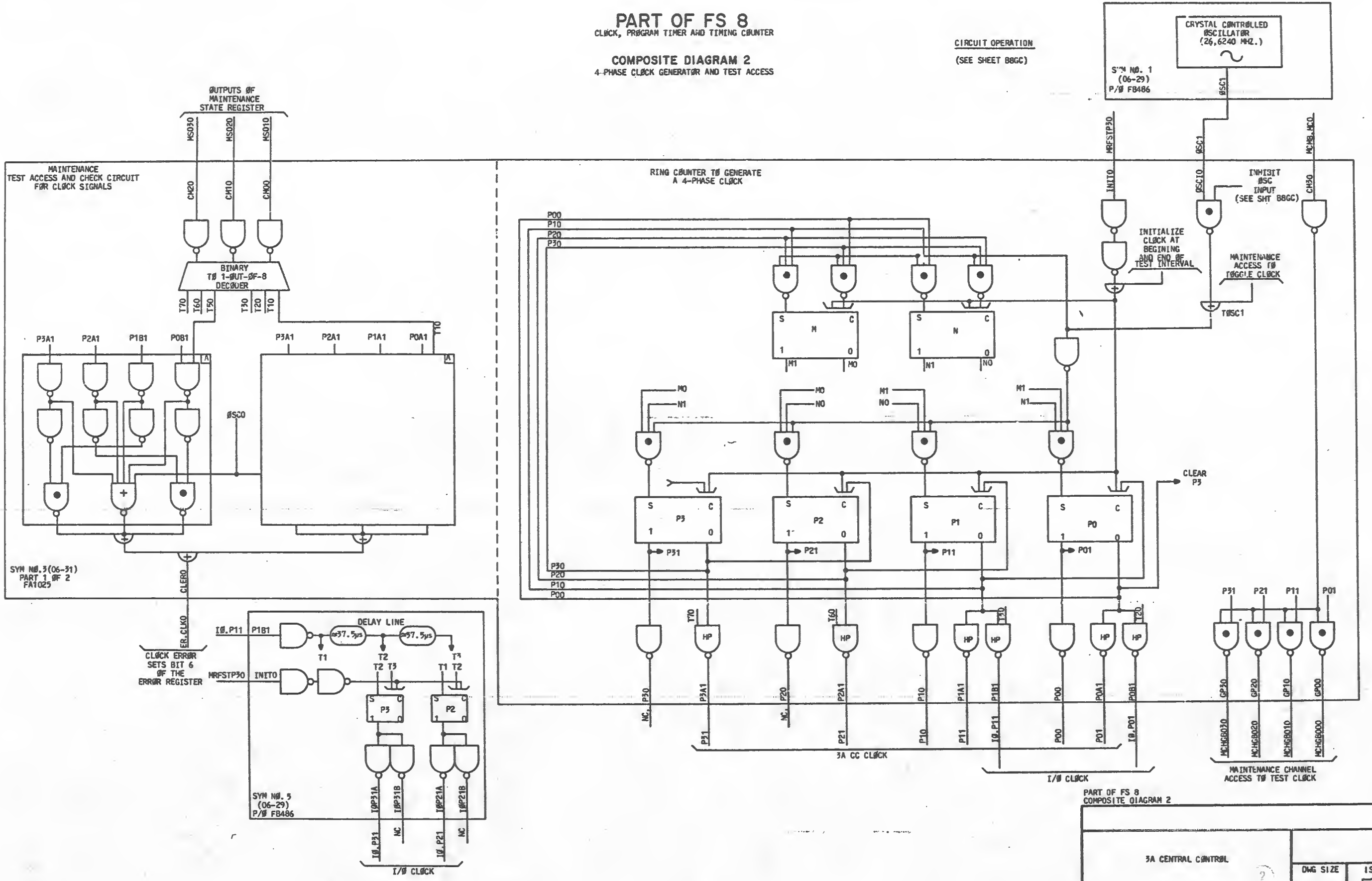
CLOCK, PROGRAM TIMER AND TIMING COUNTER

COMPOSITE DIAGRAM 2

4-PHASE CLOCK GENERATOR AND TEST ACCESS

CIRCUIT OPERATION

(SEE SHEET B8GC)


CRYSTAL CONTROLLED OSCILLATOR (26,6240 MHZ.)
SYM NO. 1 (06-29) P/O FB486
OSC1
MRFSTP30
MCHB.MCO
INITO
OSC10
INHIBIT OSC INPUT (SEE SHT B8GC)
CH30
INITIALIZE CLOCK AT BEGINING AND END OF TEST INTERVAL
MAINTENANCE ACCESS TO TOGGLE CLOCK
TOSC1
OUTPUTS OF MAINTENANCE STATE REGISTER
MSO30
MSO20
MSO10
MAINTENANCE TEST ACCESS AND CHECK CIRCUIT FOR CLOCK SIGNALS
CH20
CH10
CH00
BINARY TO 1-OUT-OF-8 DECODER
T70
T60
T50
T30
T20
T10
P3A1
P2A1
P1B1
P0B1
P3A1
P2A1
P1A1
P0A1
A
OSCO
SYM NO.3(06-31) PART 1 OF 2 FA1025
CLERO
ER.CLKO
CLOCK ERROR SETS BIT 6 OF THE ERROR REGISTER
RING COUNTER TO GENERATE A 4-PHASE CLOCK
P00
P10
P20
P30
M
N
S
C
1
0
M1
M0
N1
N0
P3
P2
P1
P0
P31
P21
P11
P01
CLEAR P3
HP
NC, P30
P3A1
P31
NC, P20
P2A1
P21
P10
P1A1
P1B1
P11
IO.P11
P00
P0A1
P0B1
P01
IO.P01
3A CC CLOCK
I/O CLOCK
GP30
GP20
GP10
GP00
MCHGB030
MCHGB020
MCHGB010
MCHGB000
MAINTENANCE CHANNEL ACCESS TO TEST CLOCK
IO.P11
P1B1
DELAY LINE
37.5μs
37.5μs
T1
T2
T3
MRFSTP30
INITO
T2 T3
T1 T2
P3
P2
SYM NO. 5 (06-29) P/O FB486
IOP31A
IOP31B
IOP21A
IOP21B
IO.P31
NC
IO.P21
NC
I/O CLOCK

PART OF FS 8
COMPOSITE DIAGRAM 2

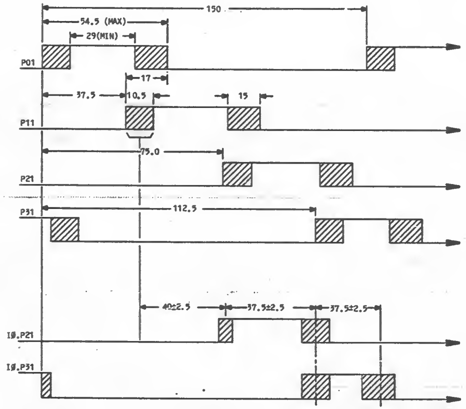
3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B8GB

PART OF FS 8

CLOCK, PROGRAM TIMER AND TIMING COUNTER

COMPOSITE DIAGRAM 3

3A CC CLOCK PHASE TIMING DIAGRAM



NOTES:

1. ALL TIMES GIVEN ARE IN ns.
2. THE TYPICAL CLOCK PULSE WIDTH FOR P01,P11,P21 AND P31 IS 47±5 ns AND THE TYPICAL CLOCK PULSE OVERLAP BETWEEN ADJACENT CLOCK PHASES IS 15±2 ns.
3. CLOCK PHASES P01,P11,P21 AND P31 ARE DRIVEN BY A 1A HIGH POWER GATE AND AS A RESULT HAVE ABOUT A 2 VOLT AMPLITUDE.
4. CLOCK PHASES P00 AND P10 OCCUR ONE GATE DELAY (3-9 ns) BEFORE CLOCK PHASE P01 AND P11. THEY ARE ALSO OF THE OPPOSITE SIGNAL POLARITY. THEY ARE DRIVEN BY A LOW POWER GATE AND HENCE HAVE ABOUT 1-VOLT AMPLITUDE.
5. IO.P01 AND IO.P11 HAVE THE SAME TIMING AS SHOWN FOR P01 AND P11.
6. CLOCK PHASES IO.P01,IO.P11,IO.P21, AND IO.P31 ARE DEDICATED TO THE I/O CHANNELS.
7. IO.P21 AND IO.P31 ARE GENERATED SPECIALY TO PROVIDE MORE ACCURATE WIDTH PULSES VIA A DELAY LINE CIRCUIT TO PROVIDE IMPROVED MARGINS WHEN OUTPULSING ON THE SERIAL I/O CHANNEL.

CIRCUIT OPERATION

THE CRYSTAL OSCILLATOR OUTPUT FROM SYMBOL NO. 1 INPUTS INTO THE RING COUNTER TO GENERATE FOUR BINARY STATES PRODUCED BY FLIP-FLOPS M AND N. THESE FOUR STATES ARE THEN USED TO SET THE FOUR CLOCK PHASE FLIP-FLOPS P0 THROUGH P3. THE OUTPUT OF THESE FLIP-FLOPS ARE BUFFERED THROUGH A SINGLE GATE AND DISTRIBUTED WITHIN THE 3A CC. BOTH POSITIVE AND NEGATIVE POLARITY PHASES ARE AVAILABLE ON THE BACKPLANE. THE POSITIVE POLARITY CLOCK PHASES P01, P11. P21, AND P31 ARE THE MOST COMMONLY USED IN THE 3A CC. FOR THIS REASON, A HIGH POWER GATE IS USED FOR THE OUTPUT GATE IN ORDER TO PROVIDE THE NEEDED FANOUT. THE TIMING FOR THESE CLOCK PHASES IS SHOWN IN COMPOSITE DIAGRAM 3. CLOCK PHASES P00 AND P10, WHICH ARE THE ONLY NEGATIVE POLARITY CLOCK PHASES USED, ARE USED ONLY FOR A COUPLE OF UNIQUE FUNCTIONS. P00 CONTROLS THE GATING INTO THE RAR AND P10 CONTROLS THE GATING INTO THE MAR (SEE FS 1).

THERE ARE ALSO FOUR POSITIVE POLARITY CLOCKS SENT TO THE I/O CHANNELS. THESE CLOCK PHASES ARE DESIGNATED I/O.P01, IO.P11, IO.P21 AND IO.P31. THE FIRST TWO OF THESE CLOCK PHASES IO.P01 AND IO.P11 ARE JUST NORMAL FANOUT PHASES OF THE REGULAR P0 AND P1 CLOCK PHASES USED IN A 3A CC. THE OTHER TWO CLOCK PHASES IO.P21 AND IO.P31 ARE SPECIALLY GENERATED BY A DELAY LINE CIRCUIT AS SHOWN IN SYMBOL NO. 2. THIS DELAY LINE CIRCUIT PROVIDES IMPROVED TOLERANCES ON THE CLOCK PHASES PULSE WIDTH FOR THESE TWO CLOCK PHASES. THE PRIMARY USE OF THE CLOCK PHASES IO.P21 AND IO.P31 IS TO GENERATE CONTROL TIMING FOR THE OUTPUTTING OF THE BIPOLAR SERIAL DATA STREAM USED IN THE SERIAL I/O CHANNELS IN THE 3A CC.

THE REMAINING CIRCUITRY IN COMPOSITE DIAGRAM 2 IS USED TO CHECK THE PROPER OPERATION OF THE 4-PHASE CLOCK. SYMBOL NO. 3 (F9) SHOWS THE ACCESS PROVIDED FOR THE MAINTENANCE CHANNEL TO READ THE STATE OF THE FOUR CLOCK PHASES. SYMBOL NO. 3 (D1) SHOWS THE CHECK CIRCUIT THAT ENSURES THE PROPER OPERATION OF THE FOUR CLOCK PHASES. IN ADDITION, MAINTENANCE STATE INPUTS ARE PROVIDED FROM THE MS REGISTER TO SET UP TEST CONDITIONS TO CHECK FOR THOSE STATES THAT CANNOT BE ADEQUATELY CHECKED BY THE CLOCK CHECK CIRCUIT UNDER NORMAL OPERATION. THE OUTPUT OF THE CHECK CIRCUIT IS SENT DIRECTLY TO THE 3A CC ERROR REGISTER. IF A CLOCK ERROR OCCURS, IT WILL SET BIT 6 OF THE ERROR REGISTER.

PART OF FS 8
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B8GC

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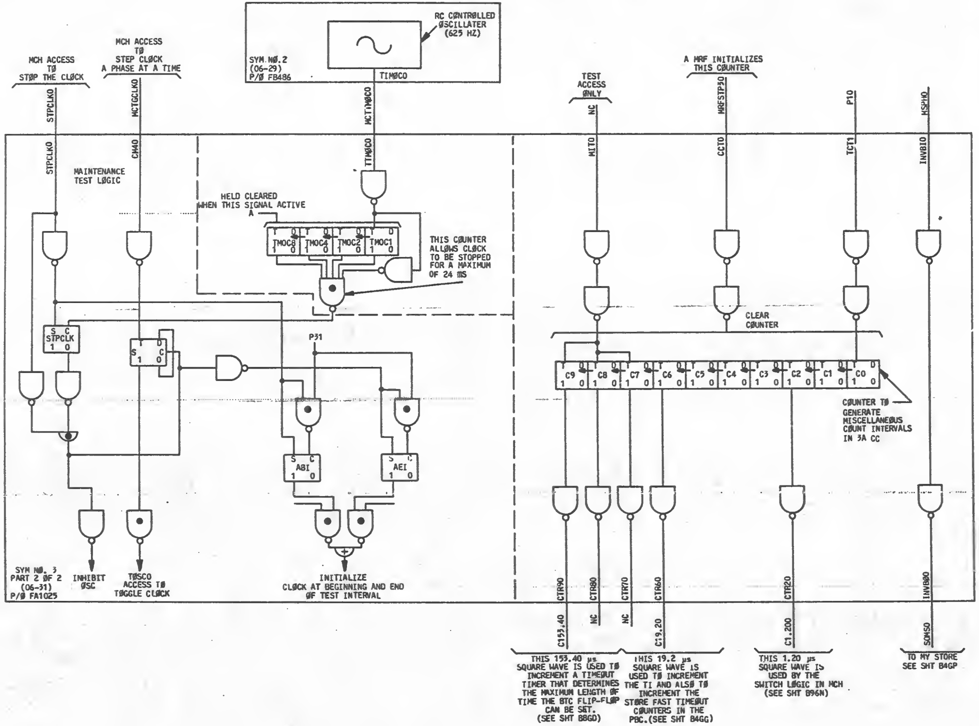
PART OF FS 8
CLOCK, PROGRAM TIMER AND TIMING COUNTER

COMPOSITE DIAGRAM 4
MCH TEST ACCESS AND MISCELLANEOUS FUNCTION TIMER


MCH ACCESS TO STOP THE CLOCK
STPCLKO
MCH ACCESS TO STEP CLOCK A PHASE AT A TIME
MCTGCLKO
RC CONTROLLED OSCILLATER (625 HZ)
SYM.NO.2 (06-29) P/O FB486
TIMOCO
MCTIMOCO
STPCLKO
CM40
TIMOCO
MAINTENANCE TEST LOGIC
HELD CLEARED WHEN THIS SIGNAL ACTIVE
A
T 0 TMOC8 1 0
T 0 TMOC4 1 0
T 0 TMOC2 1 0
T 0 TMOC1 1 0
THIS COUNTER ALLOWS CLOCK TO BE STOPPED FOR A MAXIMUM OF 24 ms
S C STPCLK 1 0
T D S C 1 0
P31
S C ABI 1 0
S C AEI 1 0
SYM NO. 3 PART 2 OF 2 (06-31) P/O FA1025
INHIBIT OSC
TOSCO ACCESS TO TOGGLE CLOCK
INITIALIZE CLOCK AT BEGINNING AND END OF TEST INTERVAL
TEST ACCESS ONLY
NC
MITO
A MRF INITIALIZES THIS COUNTER
MRFSTP30
CCTO
P10
TCT1
HSPHO
INVBIO
CLEAR COUNTER
C9 C8 C7 C6 C5 C4 C3 C2 C1 C0
COUNTER TO GENERATE MISCELLANEOUS COUNT INTERVALS IN 3A CC
CTR90
CTR80
CTR70
CTR60
CTR20
INVB00
C153.40
NC
NC
C19.20
C1.200
SOMSO
THIS 153.40 μs SQUARE WAVE IS USED TO INCREMENT A TIMEOUT TIMER THAT DETERMINES THE MAXIMUM LENGTH OF TIME THE BTC FLIP-FLOP CAN BE SET. (SEE SHT B8GD)
THIS 19.2 μs SQUARE WAVE IS USED TO INCREMENT THE TI AND ALSO TO INCREMENT THE STORE FAST TIMEOUT COUNTERS IN THE PBC.(SEE SHT B4GG)
THIS 1.20 μs SQUARE WAVE IS USED BY THE SWITCH LOGIC IN MCH (SEE SHT B96N)
TO MY STORE SEE SHT B4GP

CIRCUIT OPERATION

COMPOSITE DIAGRAM 4 (LEFT SIDE) SHOWS ADDITIONAL TEST ACCESS CIRCUITRY FOR THE 3A CC 4-PHASE CLOCK. IN ORDER TO COMPLETELY CHECK PROPER OPERATION OF THE CLOCK. IT IS NECESSARY FOR THE 3A CC TO STOP THE CLOCK IN THE OFF-LINE 3A CC. THIS IS PERFORMED BY A MAINTENANCE CHANNEL (MCH) ACCESS TO THE OFF-LINE CLOCK WITH THE CONTROL LEAD STPCLKO. WITH THIS LEAD ACTIVE THE CLOCK PULSING IS COMPLETELY STOPPED. THEN WITH ANOTHER CONTROL LEAD MCTGCLKO, THE MCH IS ABLE TO ADVANCE THE CLOCK A PHASE AT A TIME. EACH TIME A CLOCK PHASE IS STEPPED, THE ABILITY TO DETERMINE ITS OUTPUT IS PROVIDED BY THE ACCESS SHOWN IN COMPOSITE DIAGRAM 2.

BECAUSE OF THE CRITICAL NATURE OF THE CLOCK, AN INDEPENDENT TIMING SOURCE IS PROVIDED TO INSURE THAT THE CLOCK IS NOT STOPPED FOR AN INORDINATE AMOUNT OF TIME. THEREFORE, AN RC CONTROLLED OSCILLATOR (SHOWN IN SYMBOL NO. 2) IS USED TO INPUT TO A BINARY COUNTER THAT PERMITS THE CLOCK TO BE STOPPED FOR A MAXIMUM OF 24 ms. IF THE CLOCK HAS BEEN STOPPED FOR GREATER THAN 24ms THIS CIRCUITRY WILL RESTART THE CLOCK AUTOMATICALLY.

ALSO SHOWN IN COMPOSITE DIAGRAM 4 IS A BINARY COUNTER USED TO GENERATE A NUMBER OF MISCELLANEOUS CLOCK INTERVALS. EACH OF THESE INTERVALS ARE SQUARE WAVES WITH A PERIOD INDICATED ON THE SIGNAL NAMED.

PART OF FS 8
COMPOSITE DIAGRAM 4

3A CENTRAL CONTROL ②
DWG SIZE 6S
ISSUE 5A
BELL LABORATORIES
SD-1C900-01
B8GD

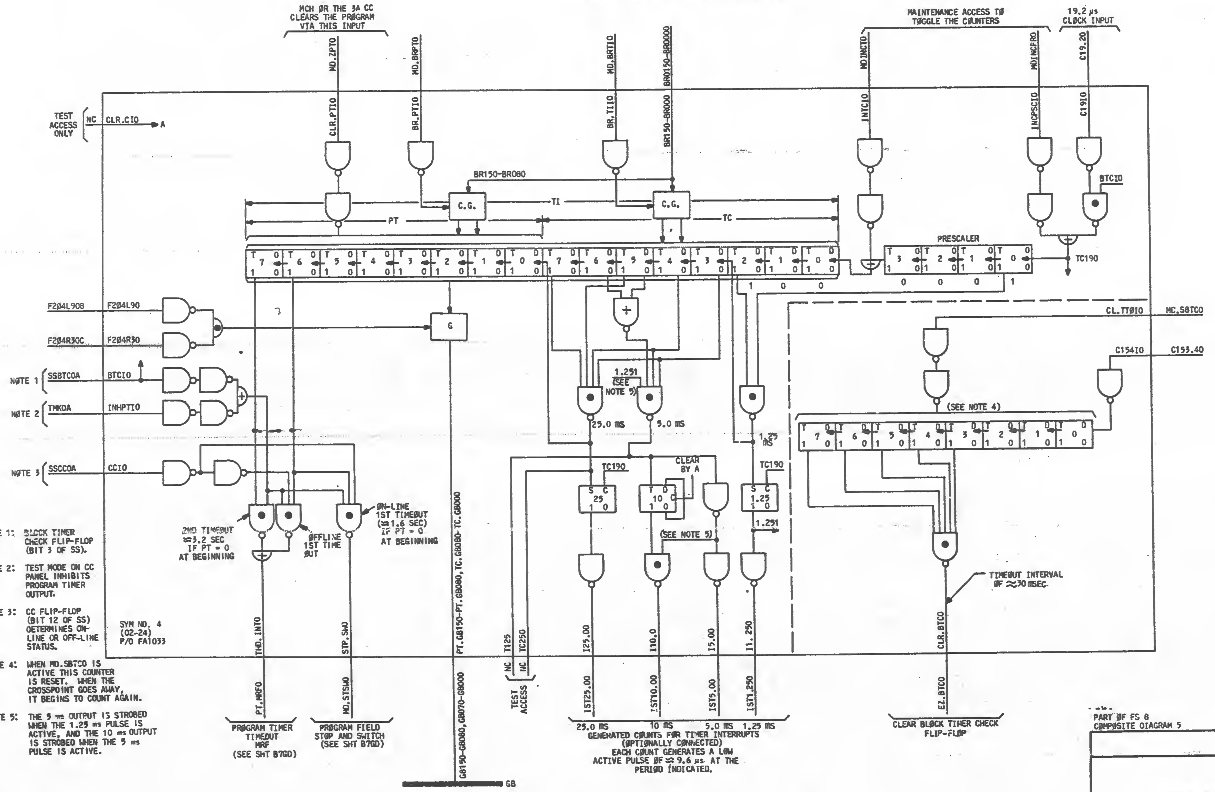
PART OF FS 8

CLØCK, PRØGRAM TIMER AND TIMING CØUNTER

COMPOSITE DIAGRAM 5

PRØGRAM TIMER AND TIMING CØUNTER ØPERATIØN

CIRCUIT OPERATION
(SEE SHT B8GF)



GENERATED CØUNTS FØR TIMER INTERRUPTS (ØPTIØNALLY CØNNECTED) EACH CØUNT GENERATES A LØW ACTIVE PULSE ØF ≈ 9.6 µs AT THE PERIØD INDICATED.

NOTE 1: BLOCK TIMER CHECK FLIP-FLOP (BIT 3 OF SS).

NOTE 2: TEST MODE ON CC PANEL INHIBITS PROGRAM TIMER OUTPUT.

NOTE 3: CC FLIP-FLOP (BIT 12 OF SS) DETERMINES ON-LINE OR OFF-LINE STATUS.

NOTE 4: WHEN MD.SBTCO IS ACTIVE THIS COUNTER IS RESET. WHEN THE CROSSPOINT GOES AWAY, IT BEGINS TO COUNT AGAIN.

NOTE 5: THE 5 ms OUTPUT IS STROBED WHEN THE 1.25 ms PULSE IS ACTIVE, AND THE 10 ms OUTPUT IS STROBED WHEN THE 5 ms PULSE IS ACTIVE.

PART ØF FS 8
CØMPØSITE DIAGRAM 5

3A CENTRAL CØNTRØL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B8GE

PRINTED IN U.S.A.

PART OF FS 8

CLOCK, PROGRAM TIMER AND TIMING COUNTER

CIRCUIT OPERATION FOR COMPOSITE DIAGRAM 5

COMPOSITE DIAGRAM 5 SHOWS THE OPERATION OF THE PROGRAM TIMER (PT) AND THE TIMING COUNTER (TC). THESE TWO TIMERS ARE CONTAINED IN THE REGISTER CALLED THE TI REGISTER.

TIMING COUNTER

THE TC PORTION OF THE TI GENERATES ACCURATELY CONTROLLED TIMED INTERRUPTS. THERE ARE FOUR TIMED INTERRUPTS. EACH ONE OF THESE TIME INTERRUPTS GENERATES A 9.6μS PULSE WITH AN APPROXIMATE PERIOD OF 1.25mS, 5.0mS, 10.0mS, AND 25.0mS. SINCE THE 5, 10, AND 25mS INTERVALS ARE INTEGER MULTIPLES OF THE 1.25m COUNT, IT IS ONLY NECESSARY TO GENERATE THE 1.25mS ACCURATELY. THE OTHER THREE CAN BE GENERATED BY DOING A BINARY COUNT OF THE 1.25mS COUNT. FOR THIS REASON, THE OUTPUT OF THE 1.25mS COUNT IS INPUTTED INTO BIT 3 OF THE TC. THEN BITS 3-7 OF THE TC DO A BINARY COUNT OF THE 1.25mS PULSE AND THEREFORE, THE 5mS OUTPUT CAN BE GENERATED AS THE COUNTER COUNTS UP FROM 0 THROUGH 4, THROUGH 8, THROUGH 12, THROUGH 16, AND FINALLY 20. 20 TIMES 1.25mS GENERATES THE 25mS COUNT. WHEN THIS HAPPENS, THE ENTTIRE TC IS CLEARED AND THE PROCESS REPEATS ITSELF. THE 10mS COUNT IS GENERATED BY A TOGGLE FLIP-FLOP ATTACHED TO THE OUTPUT OF THE 5mS OUTPUT.

THE 1.25ms COUNT IS GENERATED BY ATTACHING A PRESCALER TO THE FRONT END OF THE TC. THE PURPOSE OF THE PRESCALER IS TO PROVIDE A SMALL ENOUGH GRANULARITY IN THE COUNTING SCHEME TO GENERATE AN ACCURATE 1.25ms COUNT. NOTE THAT THE CLOCK INPUT TO THE PRESCALER IS A 19.2us SQUARE WAVE. THIS SQUARE WAVE IS GENERATED BY THE 3A CC CLOCK ITSELF AS SHOWN IN COMPOSITE DIAGRAM 4. THE 4 BITS OF THE PRESCALER AND THE LOW 3 BITS OF THE TC FORM A BINARY COUNTER THAT COUNTS UP TO THE BINARY COUNT 1000001. THIS CORRESPONDS TO DECIMAL COUNT OF 65 (65 X 19.2≃1.25msec). ACTUALLY THE CLOCK INPUT IS 19.1963. THIS ALLOWS THE GENERATION OF AN EXACTLY 1.250mS COUNT WHICH IS GOOD TO THE ACCURACY OF THE CRYSTAL ITSELF. THAT IS. THE CRYSTAL ACCURACY HAS A PERCENT TOLERANCE OF .001. THEREFORE, THE 1.25mS PULSE WILL TRACK THIS. WHEN THE PRESCALER AND THE LOW 3 BITS OF THE TC HAVE REACHED THE DECIMAL COUNT OF 65, THE 1.25ms COUNT IS GENERATED AND THEN THE LOW 3 BITS OF THE TC AND THE PRESCALER ARE CLEARED AND THE PROCESS IS REPEATED.

IN ORDER TO PROVIDE TEST ACCESS TO CHECK THE PROPER OPERATION OF THE TC, AN INHIBIT INPUT IS PROVIDED FROM THE BLOCK TIMER CHECKED (BTC) FLIP-FLOP IN THE SS REGISTER. AS SHOWN, THIS ALLOWS THE CLOCK INPUT TO THE PRESCALER TO BE SHUT OFF. THEN A MISCELLANEOUS DECODER CONTROL IS PROVIDED TO ALLOW THE INPUT TO THE PRESCALER TO BE TOGGLED A COUNT AT A TIME. IN ADDITION, THE INPUT TO THE TC IS PROVIDED WITH A SEPARATE TOGGLE TO MORE EFFICIENTLY TOGGLE THROUGH VARIOUS STATES OF THE TC.

BECAUSE OF THE IMPORTANCE OF THE TI AND IN PARTICULAR THE PT WHICH DERIVES ITS TIMING INPUTS FROM THE TC, A TIME-OUT COUNTER IS PROVIDED TO INSURE THAT THE TIMING SIGNALS GENERATED BY THE TC ARE NOT INHIBITED FOR AN INORDINATE AMOUNT OF TIME. WHEN THE BTC FLIP-FLOP IS SET, THIS TIMER BEGINS TO COUNT. THIS COUNTER WILL ACTIVATE A SIGNAL THAT WILL CLEAR THE BTC 30ms AFTER IT HAS BEEN SET. THEREFORE, IF THE TIMING COUNTER IS TO BE INHIBITED FOR AN EXTENDED PERIOD. i.e., GREATER THAN 30ms, THE BTC FLIP-FLOP MUST BE SET REPEATEDLY.

PROGRAM TIMER

THE OTHER PART OF THE PROGRAM TIMER TI REGISTER IS THE PT. THE PT PROVIDES A BASIC SANITY CHECK ON THE OPERATION OF THE 3A CC. IN ORDER TO PREVENT THE PROGRAM TIMER FROM TIMING OUT AND INITIALIZING THE 3A CC, IT IS NECESSARY FOR SOFTWARE TO ROUTINELY RESET THE PT. NOTE THAT THIS IS DONE BY PLACING A RESET OF THE PROGRAM TIMER IN VARIOUS STRATEGIC SPOTS IN THE MAIN MEMORY CODE. THEREFORE, IF THE SYSTEM GOES INTO A TIGHT LOOP OR THE CODE INADVERTENTLY BYPASSES A PROGRAM TIMER RESET FUNCTION, THE 3A CC WILL INITIALIZE.

NOTE THAT THE INPUT TO THE PT IS THE OUTPUT OF THE 25ms COUNT. THE PT DOES A STRAIGHT BINARY COUNT OF THIS 25ms. THEREFORE, IF THE PT STARTS IN THE ALL-ZERO STATE, IT TAKES APPROXIMATELY 1.6 SECONDS BEFORE BIT 6 OF THE PT IS SET, AND 3.2 SECONDS BEFORE BIT 7 IS SET. AS INDICATED IN COMPOSITE DIAGRAM 5, IF BIT 6 GETS SET AND THE 3A CC IN WHICH THE PROGRAM TIMER RESIDES IS ON-LINE, A STOP-AND-SWITCH MESSAGE IS GENERATED WHICH WILL INITIALIZE THE OFF-LINE 3A CC. NOTE THAT PT CONTINUES TO COUNT AFTER THE STOP-AND-SWITCH HAS BEEN GIVEN. IF THE MACHINE TO WHICH THE SWITCH MESSAGE HAS BEEN GIVEN DOES NOT COME ON-LINE AND HENCE RESET THE PT, THE PT WILL SET BIT 7 APPROXIMATELY 1.6 SECONDS LATER AND ANOTHER INITIALIZATION SIGNAL WILL BE GENERATED. IN THIS CASE, AN INITIALIZATION TO THE 3A CC IN WHICH THE PT IS CONTAINED WILL RESULT. IT WILL ATTEMPT TO INTIALIZE ITSELF IN ORDER TO ACHIEVE AN OPERATING STATE.

IF THE PT IS LOCATED IN THE OFF-LINE MACHINE, AND THE FIRST TIME-OUT OCCURS, THAT IS, BIT 6 GETS SET, AN INITIALIZATION

CIRCUIT OPERATION (CONT)

OF THE OFF-LINE 3A CC WILL OCCUR. NOTE THAT THIS INFERS THAT ON-LINE 3A CC IS NORMALLY EXPECTED TO SEND A PERIODIC MCH ORDER TO THE PT LOCATED IN THE OFF-LINE MACHINE TO PREVENT IT TIMING OUT. IN THIS WAY IF THE ON-LINE MACHINE BECOMES COMPLETELY INOPERATIVE, THE PT IN THE OFF-LINE 3A CC WILL INITIALIZE THE SYSTEM WITHOUT REQUIRING AN INDICATION FROM THE ONLINE 3A CC AS TO ITS INSANITY.

THE ON-LINE PT IS TYPICALLY SET (LOADED BY SOFTWARE WITH AN APPROPRIATE CONSTANT) TO TIME-OUT AHEAD OF THE OFF-LINE PT. FOR EXAMPLE, 300 TO 400mS IS A TYPICAL TIME-OUT FOR THE ON-LINE 3A CC. THE OFF-LINE IS NORMALLY RESET TO ZERO SO THAT IT WILL TIME-OUT IN THE 1.6 SECONDS. IN CASE OF A SYSTEM TROUBLE THE ON-LINE IS GIVEN ADEQUATE TIME TO PERFORM ITS INITALIZATION BEFORE THE OFF-LINE HAS AN OPPORTUNITY.

NOTE THAT THE OUTPUT OF THE BTC FLIP-FLOP ALSO INHIBITS THE OUTPUT OF THE PT. THAT IS, WHEN THE BTC FLIP-FLOP IS SET, NO INITIALIZATIONS CAN TAKE PLACE BY THE PROGRAM TIMER. THIS IS NECESSARY SO THAT DURING THE MRF INITIALIZATION PERIOD, A 3A CC CAN INHIBIT THE PROGRAM TIMER UNTIL IT REACHES A STABLE SOFTWARE STATE. NOTE AGAIN THAT THE BTC FLIP-FLOP CAN ONLY BE SET FOR A MAXIMUM OF 30ms BEFORE IT IS AUTOMATICALLY CLEARED. IN ADDITION, THE TEST MODE KEY ON THE 3A CC PANEL ALLOWS A MANUAL INTERVENTION OF THE PT INITIALIZATION FUNCTION. WHEN THE TEST MODE KEY IS ACTIVE, THE INITIALIZATION CAUSED BY THE PT CANNOT OCCUR BUT ALL OTHER TIMING FUNCTIONS OF THE TC, NAMELY THE TIME INTERRUPTS, MAY STILL OCCUR.

PART OF FS 8

3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES
SD-1C900-01
B8GF

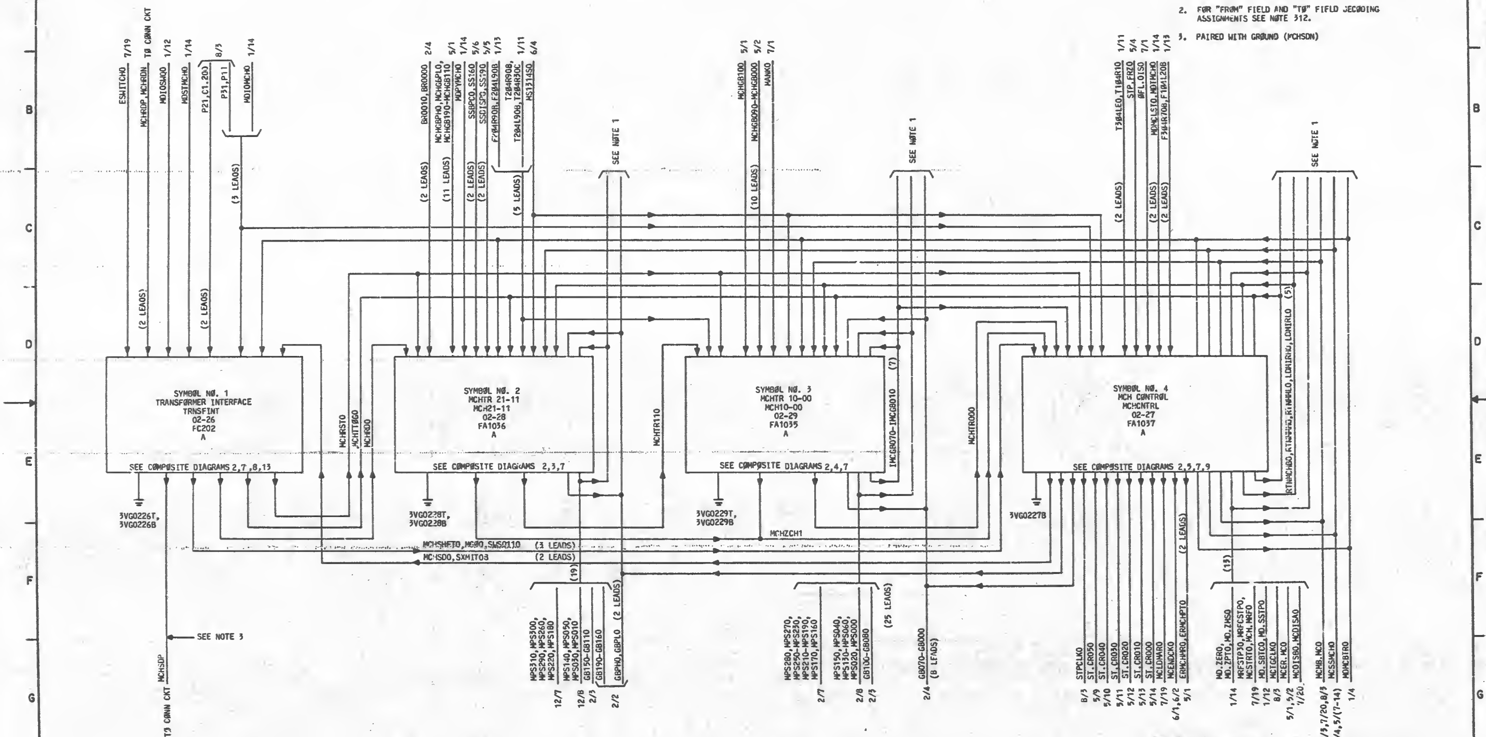
PRINTED IN U.S.A.

PART OF FS 9

MAINTENANCE CHANNEL
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (0I). ALL OFF-PAGE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.
2. FOR "FROM" FIELD AND "TO" FIELD DECODING ASSIGNMENTS SEE NOTE 312.
3. PAIRED WITH GROUND (MCHSDN)



PART OF FS 9
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B9AA

E-7471 (12-73)

PRINTED IN U.S.A.

PART OF FS 9

MAINTENANCE CHANNEL

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
BR0000,BR0010	BITS 00 AND 01 OF THE BR REGISTER (COPY 0)
C1.200	MCA CLOCK PULSE OF 1.2 USEC
ERMCHMR0	SWITCH RECEIVED BY ON-LINE CENTRAL CONTROL - SET BIT 19 OF ERROR REGISTER
ERMCHPT0	PROGRAM TIMER RESET RECEIVED BY ON-LINE CENTRAL CONTROL - SET BIT 18 OF ERROR REGISTER
ESWITCH0	ENABLE A CENTRAL CONTROL SWITCH VIA MCA
GBPH0	PARITY HIGH OF THE GATING BUS
GBPL0	PARITY LOW OF THE GATING BUS
GB000-GB190	BITS 0-19 OF THE GATING BUS
IMCGB070-IMCGB010	MCA GATING BUS LEADS BITS 7-0
LDMIRH0	MCA CONTROL - LOAD MIR HIGH BITS (31-16)
LDMIRL0	MCA CONTROL - LOAD MIR LOW BITS (15-0)
MANK0	PANEL MANUAL KEY (BIT 04 OF MISCELLANEOUS BITS)
MCDISA0	MCA CONTROL, DISABLE A
MCDISB0	MCA CONTROL, DISABLE B
MCENDCK0	MCA CONTROL ENABLE TO AND FROM FIELD CHECKERS
MCER.MC0	MCA CONTROL, ERROR REGISTER TO THE MCA
MCH.MRF0	MCA CONTROL, INITIALIZATION LEAD TO THE CENTRAL CONTROL
MCHGBPH0	PARITY HIGH OF MCA GATING BUS
MCHGBPL0	PARITY LOW OF MCA GATING BUS
MCHGB000-MCHGB190	BITS 0-19 OF SPECIAL MCA GATING BUS
MCHRDN	MCA RECEIVE DATA (TRANSFORMER INPUT - NEGATIVE LEAD)
MCHRDP	MCA RECEIVE DATA (TRANSFORMER INPUT - POSITIVE LEAD)
MCHRD0	MCA RECEIVE DATA - SERIAL DATA INPUT TO HIGH ORDER BIT OF THE SHIFT REGISTER
MCHRST0	MCA START LEAD
MCHSDP	MCA SEND DATA (TRANSFORMER OUTPUT - POSITIVE LEAD)
MCHSD0	MCA SEND DATA LEAD
MCHSHFT0	MCA SHIFT LEAD
MCHTR000	SERIAL OUTPUT OF BIT 0 OF THE MCHTR IN THE MCA
MCHTR110	SERIAL OUTPUT OF BIT 11 OF THE MCHTR IN THE MCA
MCHTTOG0	MCA SHIFT CONTROL
MCHZCH1	ALL ZEROS DETECTOR ATTACHED TO BITS 0-19, PL AND PH OF THE MCHTR IN THE MCA
MCLDMAR0	MCA CONTROL, LOAD THE MAR AND SET THE FREEZE FLIP-FLOP
MCMB.MC0	MCA CONTROL, LOAD THE MISCELLANEOUS BITS REGISTER INTO THE MCA
MCSSMCH0	MCA CONTROL, GATE THE SS TO THE MCA

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MCSTRT0	MCA CONTROL, CLEAR THE FREEZE FLIP-FLOP AND START THE MICROCONTROL
MCTGCLK0	MCA CONTROL, TOGGLE THE CLOCK SIGNAL
MD.SBTC0	MISC. DECODER, SET BLOCK TIMER CHECK BIT (BIT 3 OF THE SS)
MD.SSTP0	MISC. DECODER, SET STOP FLIP-FLOP (BIT 14 OF THE SS)
MD.ZER0	MISC. DECODER, ZERO THE ERROR REGISTER
MD.ZMS0	MISC. DECODER, ZERO THE MAINTENANCE STATE REGISTER
MD.ZPT0	MISC. DECODER, ZERO THE PROGRAM TIMER
MDIDMCH0	MISC. DECODER, IDLE THE MCA
MDIDSWQ0	MISC. DECODER, IDLE THE SWITCH SEQUENCER (DOES NOT IDLE SWITCH SEQUENCER)
MDMCBRT0	MISC. DECODER, GATE THE MCHB TO THE MCHTR (MCA TRANSMIT/RECEIVE SHIFT REGISTER)
MDMCLST0	MISC. DECODER, LOAD THE START BIT INTO THE MCA
MDPYMCH0	MISC. DECODER, GATE BR PARITY BITS TO THE MCA
MDSTMCH0	MISC. DECODER, START THE MCA
MDTMCH0	MISC. DECODER, TEST THE MCA - GATE MCH STATUS BIT TO THE C REGISTER
MGO0	MCA GO SIGNAL
MPS000-MPS310	BITS 0-31 OF THE MICROPROGRAM STORE OUTPUT
MRFCSTP0	MCA CONTROL, CLEAR STOP FLIP-FLOP
MRFSTP30	MCA CONTROL, INITIALIZE CLOCK TO PHASE P3
MS1314S0	THE "OR" OF SPECIAL BUFFERED OUTPUT OF THE MAINTENANCE STATE REGISTERS BIT 13 AND 14 - BLOCK TO FIELD GATING INTO MCA
OFL.DIS0	INDICATES CC IN LOCKED OFF-LINE OR DISABLED
P11	CLOCK PHASE P1 (POSITIVE ACTIVE)
P21	CLOCK PHASE P2 (POSITIVE ACTIVE)
P31	CLOCK PHASE P3 (POSITIVE ACTIVE)
RTNMCHB0	MCA CONTROL, LOAD THE MCHB INTO THE MCHTR
RTNMMH0	MCA CONTROL, RETURN OUTPUT OF MICROSTORE HIGH (BITS 15-31) TO MCA
RTNMML0	MCA CONTROL, RETURN OUTPUT OF MICROSTORE BITS 0-15 TO MCA
SSBPC0	BLOCK BUS PARITY CHECK BIT (BIT 18 OF THE SS)
SSDISP0	DISPLAY BIT (BIT 17 OF THE SS)
SS160	BIT 16 OF THE SS REGISTER
SS190	BIT 19 OF THE SS REGISTER
ST.CR000-ST.CR050	DIRECT SET OF BITS 0-5 OF THE CR REGISTER
STP.FRZ0	"OR" OF THE STOP FLIP-FLOP AND THE FREEZE FLIP-FLOP TO MCH
STPCLK0	MCA CONTROL, STOP CLOCK CONTROL

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SWSQ110	SWITCH SEQUENCER LOAD AND GO STATE
SXMIT0B	MAIN MCH SEQUENCER STATE, SLAVE TRANSMIT

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

89AB

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11/17/75

PART OF FS 9

MAINTENANCE CHANNEL

SYMBOL NO. 1

TRANSFORMER INTERFACE

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TRNSFINT	02-26	FC202	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
C1.200	I	315	8/3		INCR0	2A3
ESWITCH0	I	313	7/19		ENASW0	2A3
MCHRDN	I	107	TO CONN CKT		MCHRDN	2A4
MCHRDP	I	007	TO CONN CKT		MCHRDP	2A4
MCHRD0	O	307	9/2		MCHRD0	2G3
MCHRST0	O	318	9/2,9/3 9/4		MCHRST0	2G3
MCHSDP	O	108	TO CONN CKT		MCHSDP	2G4
MCHSD0	I	317	9/4		MCHSD0	2A4
MCHSHFT0	O	309	9/4		MCHSHFT0	2G5
MCHTTOG0	OT	209	9/4		SNDTOG0	2G4
MDIDMCH0	I	219	1/14		MCH1DLE0	2A4
MDIDSWQ0	I	215	1/12		IDLSWSQ0	2A3
MDHC3TR0	I	216	1/14		LDMCHB0	2A3
MDSTMCH0	I	214	1/14		MCHG00	2A3
MG00	O	218	9/4		MG00	2G3
P11	I	217	8/3		CP11	2A4
P21	I	208	8/3		CP21	2A5
P31	I	308	8/3		CP31	2A3
SWSQ110	O	316	9/4		SWSQ110	2G3
SXMIT0B	I	314	9/4		SXMIT0	2A3
3T054C	GRD	200		203	GRD	
	GRD	319		203	GRD	
	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
3VG0226B	O	008	7/21		MCHSDN	2G4
	GRD	200			GRD	
3VG0226T	GRD	319	7/21		GRD	
3V054C	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 2

MCHTR 21-11

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCH21-11	02-28	FA1036	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
BR0000	I	105	2/4	202	BR00	4A5
BR0010	I	305	2/4	202	BR10	4A3
F204L90B	I	019	1/13		F204L90	2A2
F204R90B	I	219	1/13		F204R90	2A2
GBPH0	OIT	103	2/2		MBGB210	9H2
GBPL0	OIT	109	2/2		MBGB200	9H4
GB110	OIT	208	2/3		MBGB110	10G7
GB120	OIT	108	2/3		MBGB120	10G8
GB130	OIT	007	2/3		MBGB130	10G4
GB140	OIT	010	2/3		MBGB140	10G5
GB150	OIT	309	2/3		MBGB150	10G1
GB160	OIT	008	2/2		MBGB160	10G2
GB170	OIT	303	2/2		MBGB170	9H7
GB180	OIT	004	2/2		MBGB180	9H7
GB190	OIT	003	2/2		MBGB190	9H4

SYMBOL NO. 2 (CONT)

MCHTR 21-11

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCH21-11	02-28	FA1036	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
LDMIRH0	I	014	9/4		LDMIRH0	2A9
LDM1RL0	I	204	9/4		LDMIRL0	2A9
MCHGBPH0	I	117	5/1	202	SPEC210	3A1
MCHGBPL0	I	018	5/1	202	SPEC200	3A2
MCHGB110	I	315	5/1	202	SPEC110	7A7
MCHGB120	I	115	5/1	202	SPEC120	7A5
MCHGB130	I	215	5/1	202	SPEC130	7A3
MCHGB140	I	015	5/1	202	SPEC140	7A1
MCHGB150	I	316	5/1	202	SPEC150	5A5
MCHGB160	I	116	5/1	202	SPEC160	5A3
MCHGB170	I	216	5/1	202	SPEC170	5A2
MCHGB180	I	016	5/1	202	SPEC180	5A0
MCHGB190	I	317	5/1	202	SPEC190	3A3
MCHRD0	I	201	9/1		RDATA0	4A2
MCHRST0	I	313	9/1		ZMCHTR0	2A3
MCHTR110	O	301	9/3		MCHTR110	8G7
MCHTTOG0	I	104	9/4		TTOG0	3A6
MCHZCH1	OT	101	9/3		TMCHCZA1	3H1
MCSSMCH0	I	006	9/4		RTNSSH0	2A1
MDMCBTR0	I	206	1/14		LDMCHB0	2A7
MDPYMCH0	I	113	1/14		LPARXPT0	2A1
MPS010	OIT	112	12/8		MCTR130A	8G3
MPS030	OIT	312	12/8		MCTR140A	8G1
MPS050	OIT	211	12/8		MCTR150A	6H5
MPS140	OIT	011	12/8		MCTR110B	8G6
MPS180	OIT	210	12/7		MCTR120B	8G4
MPS220	OIT	214	12/7		MCTR130B	8G3
MPS260	OIT	310	12/7		MCTR140B	8G1
MPS290	OIT	111	12/7		MCTR110A	8G7
MPS300	OIT	110	12/7		MCTR150B	6H6
MPS310	OIT	311	12/7		MCTR120A	8G5
MS1314S0	I	209	6/4		BTGAT0	2A4
RTNMCHB0	I	106	9/4		RTNMCHB0	2A0
RTNMMH0	I	013	9/4		RTNMMH0	2A7
RTNMML0	I	213	9/4		RTNMML0	2A7
SSBPC0	I	300	5/6		SSI180	5A1
SSDISP0	I	001	5/5	202	SSI170	5A1
SS160	I	100	5/6		SSI160	5A2
SS190	I	304	5/5		SSI190	3A2
T204L90B	I	118	1/11		T204L90	2A4
T204R30C	I	218	1/11		T204R30	2A3
T204R90B	I	318	1/11		T204R90	2A5
3T054C	GRD	200		203	GRD	
	GRD	0GD		203	GRD	
	GRD	319		203	GRD	
	GRD	2GD		203	GRD	
3VG0228B	GRD	107			GRD107	2H1
	GRD	205			GRD205	2H2
	GRD	207			GRD207	2H2
	GRD	002			GRD002	2H0
	GRD	005			GRD005	2H0
	GRD	202			GRD202	2H2
	GRD	200			GRD	
	GRD	307			GRD307	2H3
	GRD	302			GRD302	2H3
	GRD	102			GRD102	2H1
3VG0228T	GRD	212			GRD212	2H3
	GRD	319			GRD	
	GRD	012			GRD012	2H1
	GRD	114			GRD114	2H2

SYMBOL NO. 2 (CONT)

MCHTR 21-11

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCH21-11	02-28	FA1036	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
3VG0228T	GRD	017			GRD017	2H1
	GRD	314			GRD314	2H4
	GRD	217			GRD217	2H3
3V054C	PWR	119		203	+3	
	PWR	000		203	+3	

SYMBOL NO. 3

MCHTR 10-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCH10-00	02-29	FA1035	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
F204L90B	I	015	1/13		F204L90	2A5
F204R90B	I	215	1/13		F204R90	2A5
GB000	OIT	211	2/4		MBGB000	10H7
GB010	OIT	213	2/4		MBGB010	10H7
GB020	OIT	312	2/4		MBGB020	10H4
GB030	OIT	013	2/4		MBGB030	10H4
GB040	OIT	216	2/4		MBGB040	10H1
GB050	OIT	113	2/4		MBGB050	10H2
GB060	OIT	311	2/4		MBGB060	9G7
GB070	OIT	111	2/4		MBGB070	9G7
GB080	OIT	308	2/3		MBGB080	9G4
GB090	OIT	310	2/3		MBGB090	9G5
GB100	OIT	011	2/3		MBGB100	9G2
IMCGB010	OI	206	9/4		GBB010	7G6
IMCGB020	OI	106	9/4		GBB020	7G4
IMCGB030	OI	306	9/4		GBB030	7G2
IMCGB040	OI	108	9/4		GBB040	5G8
IMCGB050	OI	007	9/4		GBB050	5G6
IMCGB060	OI	207	9/4		GBB060	5G4
IMCGB070	OI	107	9/4		GBB070	5G2
LDMIRH0	I	100	9/4		LDMIRH0	2A7
LDMIRL0	I	300	9/4		LDM1RL0	2A5
MANK0	I	109	7/1	202	MANSW0	5A6
MCHGB000	I	318	5/2	202	SPEC000	7A6
MCHGB010	I	118	5/2	202	SPEC010	7A4
MCHGB020	I	218	5/2	202	SPEC020	7A2
MCHGB030	I	018	5/2	202	SPEC030	7A0
MCHGB040	I	309	5/2	202	SPEC040	5A7
MCHGB050	I	209	5/2	202	SPEC050	5A5
MCHGB060	I	219	5/2	202	SPEC060	5A3
MCHGB070	I	019	5/2	202	SPEC070	5A1
MCHGB080	I	110	5/2	202	SPEC080	3A6
MCHGB090	I	210	5/2	202	SPEC090	3A4
MCHGB100	I	010	5/1	202	SPEC100	3A2
MCHRST0	I	212	9/1		ZMCHTR0	2A2
MCHTR000	O	315	9/4		MCHTR000	8G8
MCHTR110	I	116	9/2		MCHTR110	4A1
MCHTTOG0	I	112	9/4		TTOG0	4A1
MCHZCH1	OT	016	9/2		TMCHCZB1	3G9
	I		9/4			

SYMBOL NO. 3 (CONT)

MCHTR 10-00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCH10-00	02-29	FA1035	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
MCM8.MC0	I	012	9/4		RTNMB0	2A8
MDMCBTR0	I	115	1/14		LDMCHB0	2A0
MPS000	OIT	006	12/8		MCTR000B	8G8
MPS020	OIT	003	12/8		MCTR080B	4H6
MPS040	OIT	304	12/8		MCTR010B	8G5
MPS060	OIT	202	12/8		MCTR090B	4H3
MPS070	OIT	307	12/8		MCTR000A	8G7
MPS080	OIT	001	12/8		MCTR020B	8G3
MPS090	OIT	008	12/8		MCTR010A	8G5
MPS100	OIT	101	12/8		MCTR100B	4H1
MPS110	OIT	208	12/8		MCTR020A	8G3
MPS120	OIT	305	12/8		MCTR030B	8G1
MPS130	OIT	004	12/8		MCTR030A	8G1
MPS150	OIT	105	12/8		MCTR040A	6G8
MPS160	OIT	205	12/7		MCTR040B	6G9
MPS170	OIT	104	12/7		MCTR050A	6G6
MPS190	OIT	303	12/7		MCTR060A	6G4
MPS200	OIT	204	12/7		MCTR050B	6G6
MPS210	OIT	002	12/7		MCTR070A	6G1
MPS230	OIT	203	12/7		MCTR080A	4H5
MPS240	OIT	103	12/7		MCTR060B	6G4
MPS250	OIT	302	12/7		MCTR090A	4H3
MPS270	OIT	301	12/7		MCTR100A	4H1
MPS280	OIT	201	12/7		MCTR070B	6G2
MS1314S0	I	117	6/4		BTGAT0	2A3
RTNMCHB0	I	313	9/4		RTNMCHB0	2A7
RTNMMH0	I	317	9/4		RTNMMH0	3A1
RTNMML0	I	009	9/4		RTNMML0	3A0
T204L90B	I	214	1/11		T204L90	2A4
T204R30C	I	014	1/11		T204R30	2A3
T204R90B	I	314	1/11		T204R90	2A4
3T054E	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
	GRD	0GD		203	GRD	
3VG0229B	GRD	102			GRD102	2H1
	GRD	200			GRD	
	GRD	005			GRD005	2H0
3VG0229T	GRD	217			GRD217	2H2
	GRD	017			GRD017	2H1
	GRD	319			GRD	
	GRD	316			GRD316	2H2
	GRD	114			GRD114	2H1
3V054E	PWR	119		203	+3	
	PWR	000		203	+3	

PART OF FS 9
SYMBOL(S) 1 2 3

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B9CA

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PART OF FS 9

MAINTENANCE CHANNEL

SYMBOL NO. 4

MCH CONTROL

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCHCNTRL	02-27	FA1037	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ERMCHMR0	O	306	5/1		ONLMRF0	10G7
ERMCHPT0	O	106	5/1		ONLCLPT0	11G6
F104L20B	I	218	1/13		F104L20	2A1
F304R70B	I	118	1/13		F304R70	2A0
GBPH0	OT	311	2/2		JAMPH0	2H1
GBPL0	OT	012	2/2		JAMPL0	2H1
GB000	OT	313	2/4		STRT0	6H7
GB010	OT	113	2/4		MCC000	6H5
GB020	OT	213	2/4		MCC010	6H3
GB030	OT	013	2/4		MCC020	6H1
GB040	OT	314	2/4		MCC030	5H7
GB050	OT	114	2/4		MCC040	5H5
GB060	OT	214	2/4		MCC050	5H3
GB070	OT	014	2/4		MCC060	5H1
IMCGB010	I	316	9/3		GBB010	6A6
IMCGB020	I	017	9/3		GBB020	6A4
IMCGB030	I	217	9/3		GBB030	6A2
IMCGB040	I	115	9/3		GBB040	5A8
IMCGB050	I	315	9/3		GBB050	5A6
IMCGB060	I	016	9/3		GBB060	5A4
IMCGB070	I	216	9/3		GBB070	5A2
LDMIRH0	OI	300	9/2,9/3		TLDMIRH0	11G6
LDMIRL0	OI	206	9/2,9/3		LDMIRL0	11G4
MCDISA0	OI	208	7/20		OISA0	12G5
MCDISB0	OI	205	7/20		OISB0	12G6
MCENDCK0	O	303	6/1,6/2		ENABER0	11G3
MCER.MC0	OI	007	5/1,5/2		RTNER0	10G7
MCH.MRF0	OI	211	7/19		SWITCH0	10G7
MCHRST0	I	309	9/1		MCHRST0	8A0
MCHSD0	O	312	9/1		MCHSD0	6H8
MCHSHFT0	I	109	9/1		SHFT0	2A5
MCHTR000	I	116	9/3		MCHTR000	5A2
MCHTTOG0	OIT	010	9/1		TTOG0	2H7
	I		9/2,9/3			
MCHZCH1	I	102	9/3		TMCHZCK1	8A1
MCLDMAR0	O	006	7/19		SETFRZ0	11G6
MCMB.MC0	OI	015	7/3,7/20 8/3,9/3		RTNMB0	10G5
MCSSMCH0	OI	215	5/4,5/7 5/8,5/9 5/10,5/11 5/12,5/13 5/14,9/2		RTNSS0	10G5
MCSTRT0	OI	207	7/19		MSTART0	11G2
MCTGCLK0	OI	110	8/3		TOGCLK0	10G5
MD.SBTC0	OIT	210	1/12		CLTT00	12G4
MD.SSTP0	OIT	004	1/12		MSTOP0	11G3
MD.ZER0	OIT	105	1/14		CLER0	12G5
MD.ZMS0	OIT	204	1/14		CLMSR0	12G3
MD.ZPT0	OIT	310	1/14		CLPT0	11G2
MDIDMCH0	I	317	1/14		RSTCLK0	4A6
MDMCBTR0	OIT	104	1/14		TLDMCHB0	12G1
MDMCLST0	I	117	1/14		LDSTRT0	6A8
MDTMCH0	I	203	1/14		MCHTST0	7A1
MG00	I	202	9/1		MG00	8A1
MRFCSTP0	OIT	005	7/19		CLRSTP0	11G5
MRFSTP30	OIT	305	7/19		INITCLK0	10G2
MS1314S0	I	018	6/4		BTGAT0	2A1
OFL.DIS0	I	103	7/1		SSCC0	11A1
P11	I	209	8/3		CP11	8A3

SYMBOL NO. 4 (CONT)

MCH CONTROL

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MCHCNTRL	02-27	FA1037	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
P31	I	308	8/3		CP31	8A1
RTNMCHB0	OI	304	9/2,9/3		RTNMCHB0	12G2
RTNMMH0	OI	111	9/2,9/3		RTNMMH0	10G3
RTNMML0	OI	011	9/2,9/3		RTNMML0	10G4
ST.CR000	O	001	5/14		MCHCOMP0	7G6
ST.CR010	O	301	5/13		MCHERR0	7G7
ST.CR020	O	002	5/12		MCHMRF0	7G9
ST.CR030	O	201	5/11		MCHSR00	7G5
ST.CR040	O	100	5/10		MCHSR10	7G3
ST.CR050	O	101	5/9		MCHSR20	7G1
STP.FRZ0	I	302	5/4		SSTPFRZ0	11A2
STPCLK0	O	112	8/3		CTLCLK0	4H6
SWS0110	I	003	9/1		MRF110	9A4
SXMIT0B	O	212	9/1		SXMIT0B	3H6
T104R10	I	318	1/11		T104R10	2A1
T304LE0	I	019	1/11		T304LE0	2A2
3T054C	GRD	2GU		203	GRD	
	GRD	319		203	GRD	
	GRC	0GD		203	GRD	
	GRD	200		203	GRD	
3VG0227B	GRD	107			GRD107	2H5
	GRD	008			GRD008	2H4
	GRD	307			GRD307	2H4
	GRD	200			GRD	
3V054C	PWR	119		203	+3	
	PWR	000		203	+3	

PART OF FS 9
SYMBOL(S) 4

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	3A

BELL LABORATORIES
SD-1C900-01
B9CB

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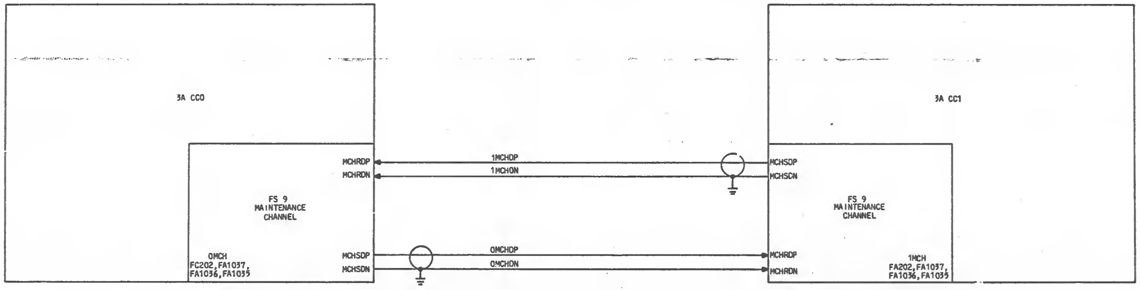
10/28/75

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM I

MCH INTERCONNECTION



CIRCUIT OPERATION

THE MAINTENANCE CHANNEL (MCH) INTERCONNECTS AND PROVIDES THE MAIN SOURCE OF COMMUNICATION BETWEEN THE DUPLICATED 3A CC PROCESSORS. IT IS A SERIAL HIGH-SPEED (6.67 MB/S) DATA TRANSFER SYSTEM CAPABLE OF TRANSMITTING A 30-BIT MESSAGE COMPRISED OF A 20-BIT DATA FIELD, TWO PARITY BITS AND AN 8-BIT CONTROL FIELD. THE MCH CONTROLLER CONTAINS THE NECESSARY SEQUENCE LOGIC TO EXECUTE THE CONTROL FUNCTION INDICATED BY THE CONTROL FIELD CONTENTS. THE RESULT OF THESE OPERATIONS MAY BE RETURNED TO THE CONTROLLING PROCESSOR VIA SUBSEQUENT MCH TRANSMISSIONS FOR ANALYSIS. IN THIS MANNER, DIAGNOTSTIC ROUTINES MAY BE EXECUTED UNDER EXTERNAL CONTROL USING THE 3A CC MICROCONTROL LOGIC. BY USING THIS FACILITY, THE MCH MAY CAUSE EXECUTION OF CERTAIN SEGMENTS OF 3A CC MICROCODE AND VERIFY ITS CORRECT OPERATION.

THE MCH MAY ALSO EXECUTE MICROINSTRUCTIONS INDEPENDENTLY OF THE MICROSTORE BY LOADING THESE INSTRUCTIONS ONE AT A TIME DIRECTLY INTO THE MICROCONTROL LOGIC. THIS ABILITY ALLOWS CERTAIN DIAGNOSTIC ROUTINES TO BE INDEPENDENT OF THE MICROSTORE CONTENTS.

TRANSMISSIONS MAY BE INITIATED BY EITHER OF THE 3A CC PROCESSORS INDEPENDENTLY OF THEIR ON-LINE/OFF-LINE STATUS. NO FIXED PRIORITIES EXIST, THE TRANSMISSION LINK IS SEIZED ON A FIRST-COME FIRST-SERVED BASIS. THE TWO MCH CONTROLLERS ARE AC COUPLED TO PROVIDE ISOLATION, THEREBY PREVENTING HARD FAULTS IN ONE PROCESSOR FROM AFFECTING THE OTHER. THESE CONTROLLERS OPERATE ASYNCHRONOUSLY, DERIVING THE NECESSARY CLOCKING DIRECTLY FROM THE INCOMING DATA MESSAGE. A CERTAIN AMOUNT OF ERROR CHECKING IS INTEGRATED INTO THE DESIGN OF THE MCH, AND PARITY IS PRESERVED IN THE TRANSMITTED MESSAGE.

THE MCH ALSO HAS THE RESPONSIBILITY TO INITIATE AN AUTOMATIC TRANSMISSION IF A FATAL ERROR IS ENCOUNTERED WITHIN THE 3A CC. THIS TRANSMISSION RESULTS IN THE STANDBY PROCESSOR COMING ON-LINE, TO TAKE OVER THE CALL PROCESSING RESPONSIBILITY. THE 3A CC MAINTENANCE CHANNEL HAS THE ABILITY TO CONTROL THE 3A CC AT ITS MOST BASIC LEVEL, THE MICROINSTRUCTION LEVEL. IT HAS THE ABILITY TO INHIBIT THE NORMAL MICROSEQUENCING, AND LOAD THE MICROPROGRAM STORE OUTPUT REGISTER (MIR), (SEE COMPOSITE DIAGRAM 2). THE LOADING OF THIS REGISTER CAUSES ITS CONTENTS TO BE EXECUTED USING THE CONTROLLED PROCESSOR'S HARDWARE AND TIMING. SINCE ALL MICROINSTRUCTIONS ARE EXECUTED FROM THE MIR, THIS PROVIDES ONE 3A CC WITH COMPLETE EXTERNAL CONTROL IN EXERCISING THE OTHER 3A CC.

CIRCUIT OPERATION (CONT)

ANOTHER IMPORTANT FUNCTION OF THE MCH IS ITS ABILITY TO VERIFY THE CONTENTS OF MICROSTORE. THIS IS ACCOMPLISHED BY STOPPING THE PROCESSOR AND LOADING THE NEXT ADDRESS (NA) FIELD OF THE MIR (SEE COMPOSITE DIAGRAM 2). THIS NEXT ADDRESS FIELD IS GATED TO THE MICROSTORE ADDRESS REGISTER (MAR) VIA PROCESSOR TIMING-FREEZING THE MAR AT THIS NEW ADDRESS AND CAUSING A READ FROM THIS LOCATION. THE CONTENTS OF THIS WORD CAN THEN BE RETURNED TO THE OTHER PROCESSOR VIA SUBSEQUENT MCH COMMANDS. ONCE THE MICROSTORE IS FROZEN, THE MCH HAS THE ABILITY TO BEGIN THE NORMAL MICROSEQUENCING AT THIS NEW ADDRESS.

ALSO INCLUDED ARE MORE SPECIALIZED FUNCTIONS TO PROVIDE SPECIFIC DIAGNOSTIC DATA. FOR EXAMPLE, UNDER MCH CONTROL, THE SYSTEM CLOCK CAN BE STOPPED AND STEPPED ALONG ONE CLOCK PHASE AT A TIME. IN BETWEEN STEPS, THE STATE OF ALL PHASES CAN BE RETURNED TO THE OTHER PROCESSOR FOR ANALYSIS. ADDITIONAL MCH ORDERS ARE DESCRIBED ON SHEET B9GJ.

PART ØF FS 9
COMPØSITE DIAGRAM 1

ISSUE
5A

3A CENTRAL CONTROL ②

SD-1C900-01-B9GA

BELL TELEPHONE LABORATORIES
INCORPORATED

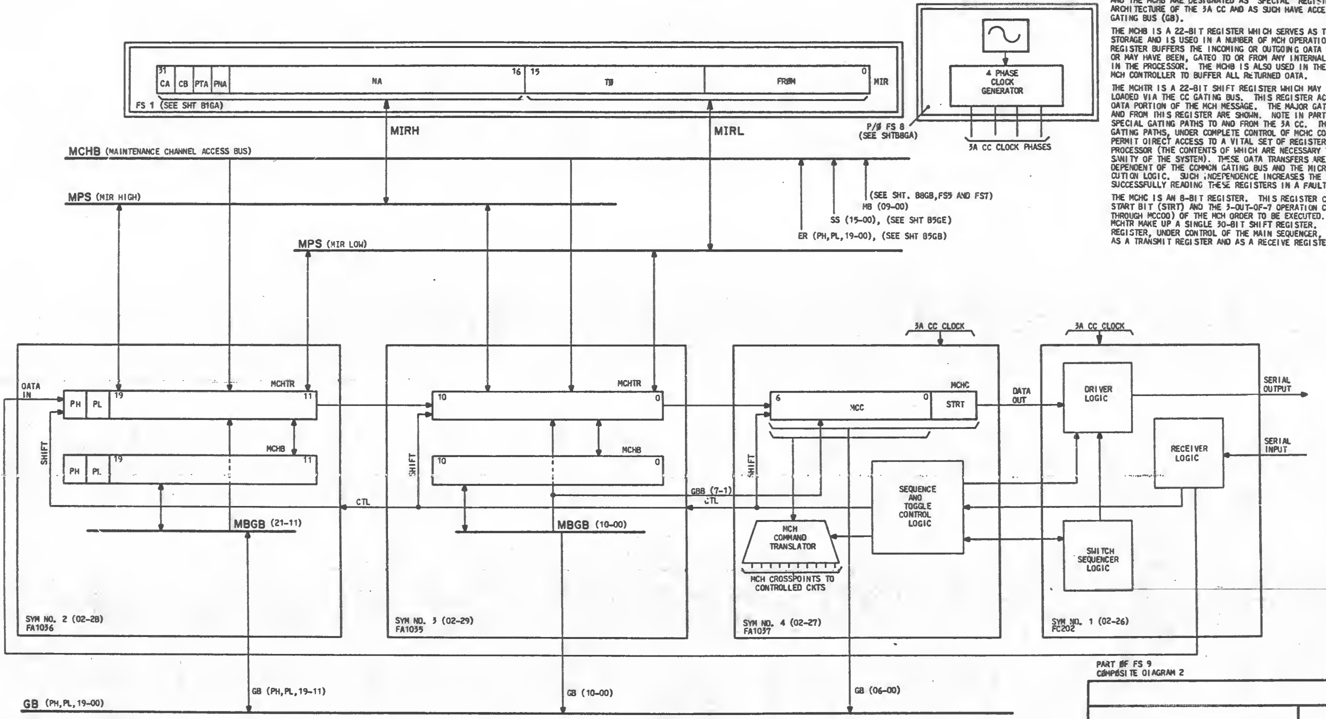
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 2

FUNCTIONAL PARTITIONING OF MAINTENANCE CHANNEL



CIRCUIT OPERATION

ORGANIZATION

THE MCH CONSISTS OF TWO IDENTICAL SEMI-INDEPENDENT CONTROLLERS, ONE LOCATED IN EACH PROCESSOR CONNECTED BY A PAIR OF COAXIAL CABLES. ALTHOUGH EACH CONTROLLER HAS THE CAPABILITY OF INITIATING A TRANSMISSION TO THE OTHER AND LIKEWISE RECEIVING SUCH A TRANSMISSION, THE SYSTEM IS RUN IN A HALF-DUPLEX MODE IN WHICH ONLY ONE-WAY TRANSMISSION IS PERMITTED AT ANY GIVEN TIME.

THE BASIC STRUCTURE OF A MCH CONTROLLER IS SHOWN IN COMPOSITE DIAGRAM 2. IT CONSISTS OF A TRANSMIT/RECEIVE REGISTER (MCHTR), A COMMAND REGISTER (MCHC), A BUFFER REGISTER (MCHB), SEQUENCE AND CONTROL LOGIC, VARIOUS INTRAPROCESSOR GATING PATHS, ERROR CHECK CIRCUITRY, AND A COMMAND DECODER WHICH DECODES THE COMMAND PORTION OF THE RECEIVED MESSAGE. THE MCHTR, MCHC, AND THE MCHB ARE DESIGNATED AS "SPECIAL" REGISTERS IN THE ARCHITECTURE OF THE 3A CC AND AS SUCH HAVE ACCESS TO THE CC GATING BUS (GB).

THE MCHB IS A 22-BIT REGISTER WHICH SERVES AS TEMPORARY STORAGE AND IS USED IN A NUMBER OF MCH OPERATIONS. THIS REGISTER BUFFERS THE INCOMING OR OUTGOING DATA WHICH MAY BE, OR MAY HAVE BEEN, GATED TO OR FROM ANY INTERNAL REGISTER WITHIN THE PROCESSOR. THE MCHB IS ALSO USED IN THE ORIGINATING MCH CONTROLLER TO BUFFER ALL RETURNED DATA.

THE MCHTR IS A 22-BIT SHIFT REGISTER WHICH MAY BE PARALLEL LOADED VIA THE CC GATING BUS. THIS REGISTER ACCEPTS THE DATA PORTION OF THE MCH MESSAGE. THE MAJOR GATING PATHS TO AND FROM THIS REGISTER ARE SHOWN. NOTE IN PARTICULAR THE SPECIAL GATING PATHS TO AND FROM THE 3A CC. THESE PRIVATE GATING PATHS, UNDER COMPLETE CONTROL OF MCHC COMMAND REGISTER, PERMIT DIRECT ACCESS TO A VITAL SET OF REGISTERS WITHIN THE PROCESSOR (THE CONTENTS OF WHICH ARE NECESSARY TO DETERMINE THE SANITY OF THE SYSTEM). THESE DATA TRANSFERS ARE NECESSARILY INDEPENDENT OF THE COMMON GATING BUS AND THE MICROCONTROL EXECUTION LOGIC. SUCH INDEPENDENCE INCREASES THE PROBABILITY OF SUCCESSFULLY READING THESE REGISTERS IN A FAULTY PROCESSOR.

THE MCHC IS AN 8-BIT REGISTER. THIS REGISTER CONTAINS THE START BIT (STRT) AND THE 3-OUT-OF-7 OPERATION CODE (MCC06 THROUGH MCC00) OF THE MCH ORDER TO BE EXECUTED. THE MCHC AND THE MCHTR MAKE UP A SINGLE 30-BIT SHIFT REGISTER. THIS SHIFT REGISTER, UNDER CONTROL OF THE MAIN SEQUENCER, SERVES BOTH AS A TRANSMIT REGISTER AND AS A RECEIVE REGISTER.

PART ØF FS 9
CØMPØSITE DIAGRAM 2

3A CENTRAL CONTROL

DWG SIZE
6S

ISSUE
5A

BELL LABORATORIES
SD-1C900-01
B9GB

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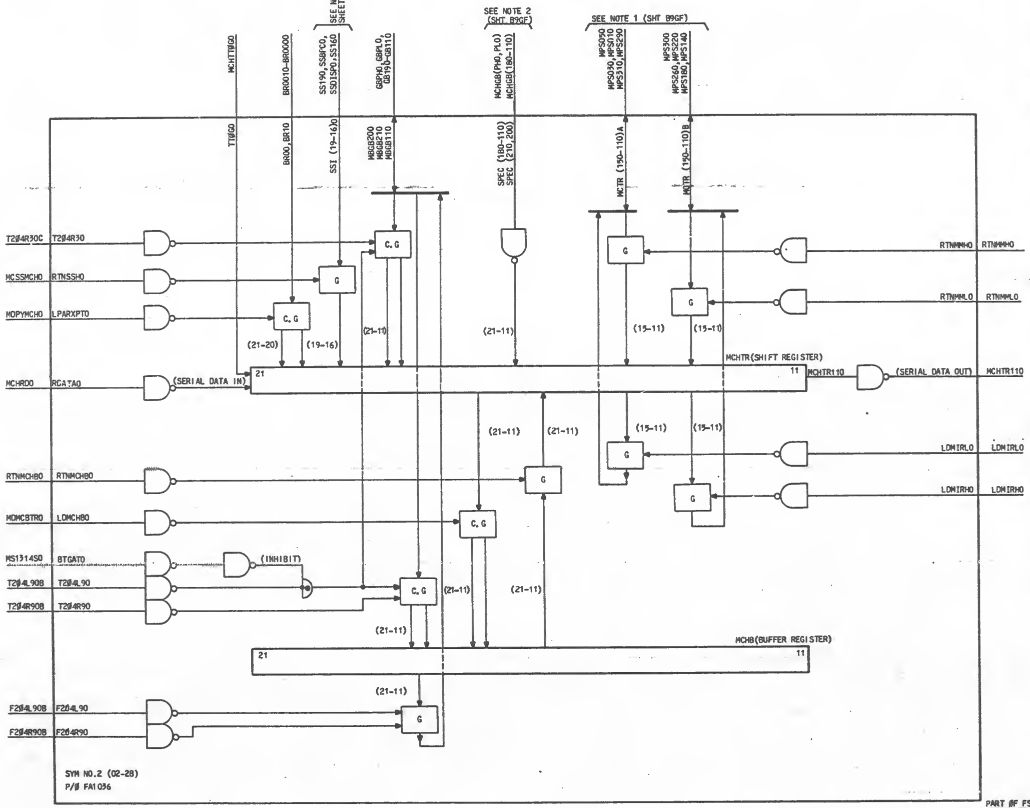
PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 3

GATING PATHS



SYM NO.2 (02-28)
P/0 FA1036

CIRCUIT OPERATION

COMPOSITE DIAGRAM 3 AND 4 DETAIL THE VARIOUS GATING PATHS ASSOCIATED WITH THE MCHTR AND THE MCHB. THERE ARE TWO BASIC TYPES OF GATING FUNCTIONS PERFORMED ON THESE REGISTERS. ONE IS THE NORMAL CLEAR AND GATE TYPE UNDER DIRECT CONTROL OF THE CC TO FIELDS AND FROM FIELDS. THE OTHER IS THE DIRECT SET TYPE UNDER CONTROL OF THE DECODED COMMAND FIELD OF THE SERIAL MESSAGE RECEIVED FROM THE OTHER CC. THE LATTER TYPE REQUIRES THAT THE CONTENTS OF THE MCHTR BE ZERO PRIOR TO THE GATING. THAT IS, THE MCHTR PORTION OF THE 30-BIT SERIAL MESSAGE, WHOSE DECODED COMMAND FIELD INITIATED THE PARTICULAR GATING FUNCTION, MUST CONTAIN ALL ZEROS.

CC GATING BUS TO MCHTR AND MCHG

THIS GATING IS OF THE CLEAR AND GATE TYPE. BITS GBPH0, GBPL0, AND GB190 THROUGH GB000 ARE GATED TO THE CORRESPONDING BITS OF THE MCHTR OR MCHB UNDER TO-FIELD CONTROL. MISCELLANIOUS DECODER SIGNAL, MS1314S0, IS A DC MAINTENANCE STATE WHICH, WHEN ACTIVE (GROUND), INHIBITS ALL GATING TO THESE REGISTERS. THIS MAINTENANCE STATE IS USED TO PREVENT INTERACTION WITH MAINTENANCE CHANNEL OPERATION DURING CERTAIN DIAGNOSTIC ROUTINES.

WHILE BOTH THE MCHTR AND THE MCHB MAY BE LOADED FROM THE CC GATING BUS, ONLY THE MCHB MAY BE GATED DIRECTLY BACK ONTO IT.

MCHTR TO MIRH(L)

MCH DECODER OUTPUTS LDMIRH(L) GATE THE MCHTR (15-00) TO EITHER THE MICROINSTRUCTION REGISTER HIGH BITS (MIR[31-16]) OR LOW BITS (MIR[15-00]). THE DATA DRIVES INTO BACKPLANE COLLECTOR TIES ORING WITH THE MICRO STORE OUTPUTS AT THE INPUT TO THE MIR. THE MICROSTORE IS FORCED INACTIVE DURING THIS GATING INTERVAL SO THAT ONLY THE DATA FROM THE MCHTR IS TRANSFERRED TO THE MIR.

MIRH(L) TO MCHTR

MCH DECODER OUTPUTS RTNMMH(L) GATE THE ABOVE COLLECTOR TIES INTO THE MCHTR WITH THE MICROSTORE OUTPUTS ACTIVE AND FROZEN AT THE MICRO-ADDRESS OF INTEREST. NOTE THAT TO READ THE FULL 32 BITS OF A SINGLE MICROSTORE WORD, TWO MCH TRANSMISSIONS ARE REQUIRED. ONE IS TO READ AND RETURN THE HIGH BITS AND ANOTHER IS TO READ AND RETURN THE LOW BITS.

SPECIAL GATING BUS

INPUT LEADS MCHGB(PH,PL 18 THROUGH 00) ARE NON-GATED DIRECT SET INPUTS TO THE CORRESPONDING BITS OF THE MCHTR. THESE NON-GATED INPUTS REPRESENT A COLLECTOR TIE ON THE CC BACKPLANE. THIS IS WHERE DATA FROM A SEPARATE SOURCES MAY BE PLACED INTO THE MCHTR WITH GATING CONTROL SUPPLIED AT THE ORGINATING REGISTER BY DECODED CONTROL OUTPUTS FROM THE MCHC. THIS FUNCTION REQUIRES THE CONTENTS OF THE MCHTR TO BE ZERO PRIOR THE GATING. THE REGISTERS WHICH HAVE ACCESS TO THIS SPECIAL GATING BUS ARE LISTED IN NOTE 2 OF SHEET B9GF.

LOAD PARITY BITS OF MCHTR

MISCELLANEOUS DECODER CONTROL SIGNAL MDPYMCH0 LOADS THE PARITY BITS OF THE MCHTR FROM THE TWO LEAST SIGNIFICANT BITS OF THE B REGISTER OF THE DML. THIS FUNCTION IS PROVIDED FOR MAINTENANCE USE.

THE REST OF THE GATING PATHS ARE UNDER CONTROL OF THE MCH COMMAND DECODER AND CAUSE THE APPROPIATE DATA TRANSFERS. SEE SHEET B9GJ FOR A COMPLETE LIST OF THE MCH COMMANDS AND A DESCRIPTION OF EACH.

PART 0F FS 9
C0MP0SITE DIAGRAM 3

ISSUE
5A

3A CENTRAL CONTROL

SD-1C900-01-B9GC

BELL TELEPHONE LABORATORIES
INCORPORATED

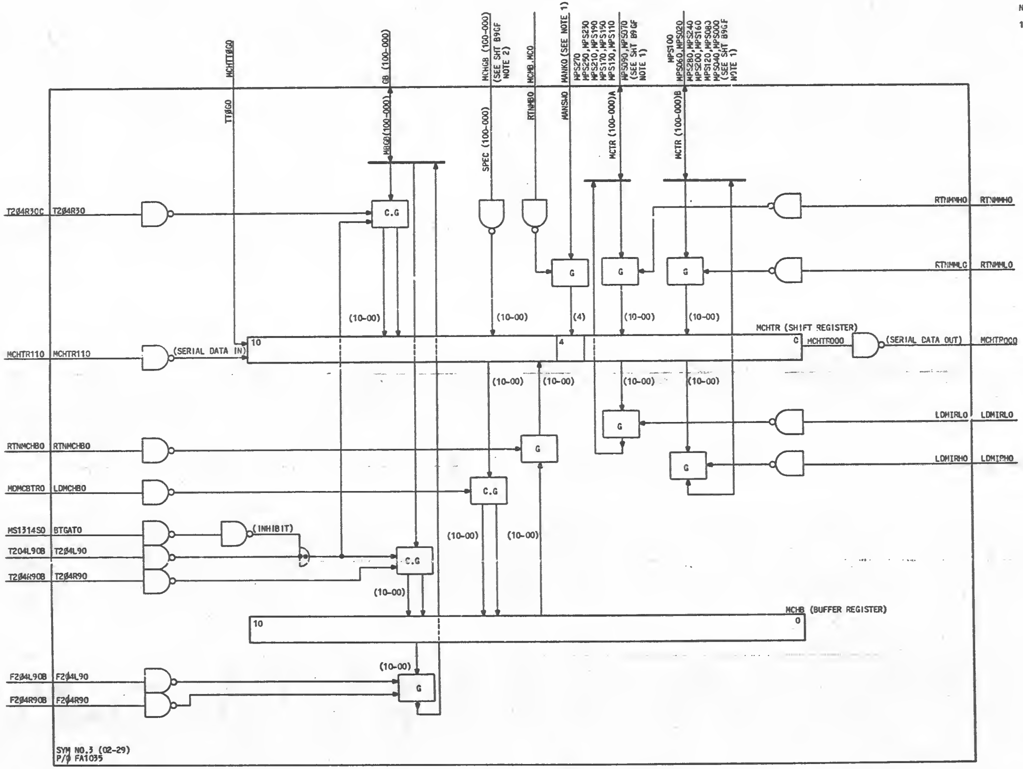
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 4

GATING PATHS



NOTES:

1. BIT 4 OF THE MISCELLANEOUS BITS GATING FUNCTION IS GATED DIRECTLY FROM THE MANUAL SWITCH UNDER MCH DECODER CONTROL (SEE SHT B9GF - NOTE 2).

PART OF FS 9
COMPOSITE DIAGRAM 4

ISSUE
3A

3A CENTRAL CONTROL

SD-1C900-01-B9GD

BELL TELEPHONE LABORATORIES
INCORPORATED

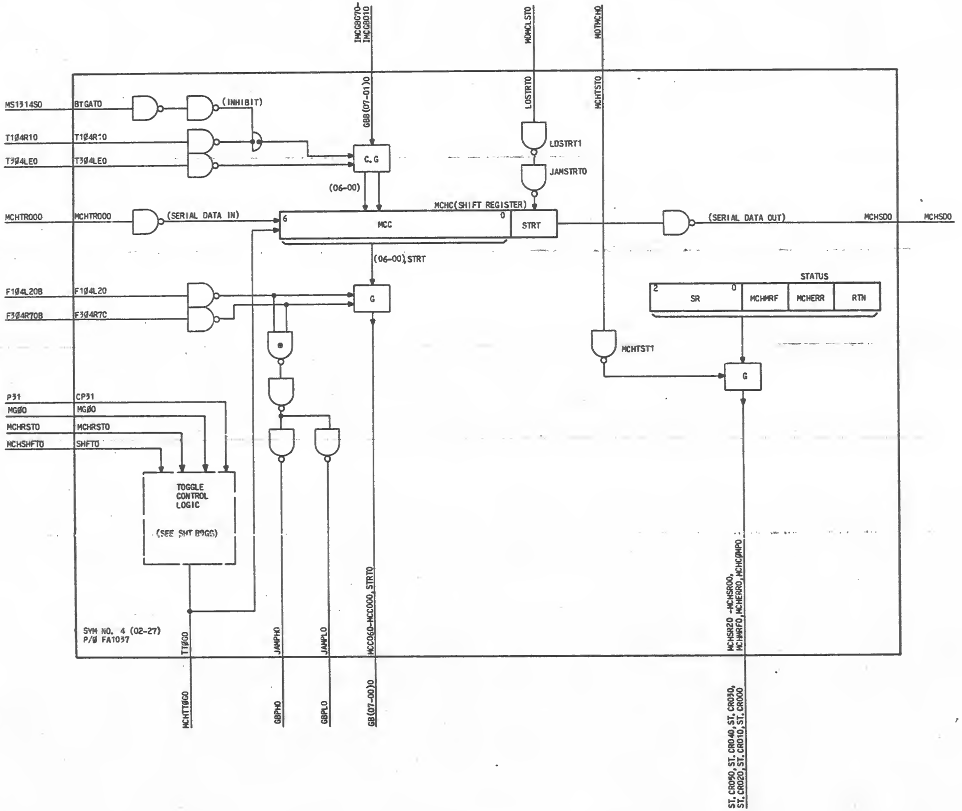
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 5

TOGGLE CONTROL AND GATING PATHS



CIRCUIT OPERATION

COMPOSITE DIAGRAM 5 DETAILS THE VARIOUS GATING PATHS ASSOCIATED WITH THE MCMC:

1. PROCESSOR GATING BUS TO MCMC - THE MCC PORTION OF THE MCMC (MCC06 THROUGH MCC00) MAY BE LOADED VIA THE GB BITS GBB07 THROUGH GBB01 IN THE NORMAL TO-FIELD CLEAR AND GATE OPERATION (SEE FS 3 SHEET B3GB). NET MS131450 IS A DC MAINTENANCE STATE WHICH, WHEN ACTIVE (GROUND), INHIBITS ALL GATING INTO THIS REGISTER. THIS MAINTENANCE STATE PREVENTS INTERACTION WITH THE MCH OPERATION DURING CERTAIN DIAGNOSTIC ROUTINES. THE GB INPUTS TO THE MCC ARE NOT DRIVEN DIRECTLY FROM THE GB BUT ARE DOUBLE BUFFERED ON FA1035 FOR FANOUT REASONS. THE LOW-ORDER BIT OF THE MCMC (STRT) IS NOT GATED FROM THE GB. THE CLEAR IS PERFORMED BY THIS GATING FUNCTION, BUT THE GATING OPERATION TO THIS BIT (ACTUALLY A JAM SET) IS PERFORMED BY CONTROL SIGNAL MOMCLSTO. IN NORMAL OPERATION, IT WOULD BE EXECUTED AS A SEPARATE CONTROL OPERATION IMMEDIATELY FOLLOWING THE GATING OPERATION UNDER PROGRAM CONTROL.

2. MCMC TO THE CC GATING BUS - THE OUTPUTS OF THE MCC06 THROUGH MCC00 AND STRT ARE GATED DIRECTLY TO THE GATING BUS GB07 THROUGH GB00.

   THE CC GATING BUS IS 20 DATA BITS WIDE, WITH TWO SEPARATE PARITY BITS. THE PARITY LOW BIT (PL) IS ASSOCIATED WITH THE LOWER 8 BITS OF THE GB AND THE PARITY HIGH BIT (PH) IS ASSOCIATED WITH THE UPPER 12 BITS. SPECIAL ATTENTION, THEREFORE, MUST BE GIVEN TO INSURE THAT DATA OF CORRECT PARITY IS GATED TO THE BUS DURING THIS OPERATION. THE MCMC CONTAINS 8 BITS AND IS GATED TO THE LOWER 8 BITS OF THE GB. FURTHERMORE, THE ONLY VALID DATA NORMALLY CONTAINED WITHIN THIS REGISTER ARE 4-OUT-OF-8 CODES, REQUIRING PARITY LOW (PL) ALWAYS TO BE A ONE. SINCE THE UPPER 12 BITS ARE NOT GATED BY THIS OPERATION (THEREFORE ZERO), THE PARITY HIGH (PH) MUST ALSO BE A ONE. THEREFORE, OUTPUTS JAMPHO AND JAMPLO FORCE ONES ON THE GB PARITY BITS (GBPHO AND GBPLO), DURING THIS GATING OPERATION.

3. MCH STATUS GATING - CERTAIN MCH STATUS BITS CONTAINED WITHIN THE MCH MAY BE GATED TO THE C REGISTER (CR) OF THE CENTRAL CONTROL. THESE BITS AND THEIR FUNCTIONS ARE LISTED BELOW.

STATUS BIT	CR BIT	FUNCTION
MCHC0MPO	0	INDICATION THAT THIS MCH CONTROLLER HAS RECEIVED A RETURN MESSAGE FROM THE OTHER CC'S MCH INDICATING MESSAGE COMPLETE.
MCHERRO	1	MAINTENANCE CHANNEL ERROR INDICATION OF EITHER A DOUBLE OUTPUT DETECTED IN THE OTHER CC'S MCH, OR AN ERROR CAUSED BY BOTH CC'S MCH CONTROLLERS TRANSMITTING SIMULTANEOUSLY.
MCHMRFO	2	INDICATION THAT THIS MCH CONTROLLER RECEIVED A TRANSMISSION FROM THE ON-LINE CC TO INITIALIZE THIS, THE OFF-LINE CC.
MCHSR00	3	INDICATES THE STATE OF THE MCH SEQUENCER.
MCHSR10	4	
MCHSR20	5	

THIS GATING PATH IS A SPECIAL DIRECT CONNECTION FROM THE MCH STATUS BITS TO THE DIRECT SET INPUTS OF THE ASSOCIATED CR BITS. SINCE THIS GATING FUNCTION IS NOT OF THE AUTOMATIC CLEAR AND GATE CLASS PREVIOUSLY DESCRIBED, THE CR MUST BE CLEARED UNDER PROGRAM CONTROL PRIOR TO THE EXECUTION OF THIS GATING.

MISCELLANEOUS DECODER CONTROL SIGNAL MOTMCHO PERFORMS THIS GATING.

PART OF FS 9
COMPOSITE DIAGRAM 5

ISSUE
5A

3A CENTRAL CONTROL ②

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6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 6

MAIN SEQUENCER

NOTE:

1. MICRO PROGRAM STORE (MPS)-MICRO INSTRUCTION REGISTER (MIR)-BIT MAPPING TO THE MAINTENANCE CHANNEL SHIFT REGISTER.

MCHTR	RTNMMLO/LDMIRLO		RTNMMHO/LDMIRHO	
	MPS	MIR	MPS	MIR
0	000	0	070	16
1	040	1	090	17
2	080	2	110	18
3	120	3	130	19
4	160	4	150	20
5	200	5	170	21
6	240	6	190	22
7	280	7	210	23
8	020	8	230	24
9	060	9	250	25
10	100	10	270	26
11	140	11	290	27
12	180	12	310	28
13	220	13	010	29
14	260	14	030	30
15	300	15	050	31

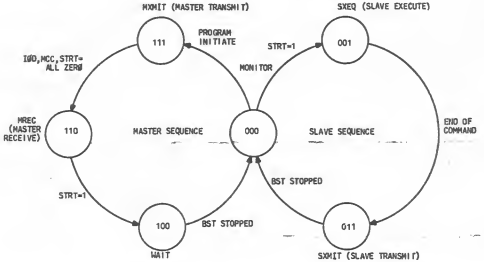
NOTE:

2. DATA LEADS WHICH MAKE UP THE SPECIAL PRIVATE GATING BUS (MCHGB) FROM SELECTED PROCESSOR REGISTERS TO THE MAINTENANCE CHANNEL SHIFT REGISTER.

SPECIAL MCH GATING BUS (MCHGB)	ERROR REGISTER (ER)	SYSTEM STATUS REGISTER (SS)	MISCELLANEOUS BITS
000	00	00	P0
010	01	01	P1
020	02	02	P2
030	03	03	P3
040	04	04	*
050	05	05	SDIS (SEMI-DISABLE)
060	06	06	SEN (SEMI-ENABLE)
070	07	07	DISSFF (DISABLE FLIP-FLOP)
080	08	08	PWK (POWER KEY)
090	09	09	TMK (TEST MODE KEY)
100	10	10	
110	11	11	
120	12	12	
130	13	13	
140	14	14	
150	15	15	
160	16	**	
170	17	**	
180	18	**	
190	19	**	
PLO	PL		
PHO	PH		

* BIT 4 OF THE MISCELLANEOUS BITS IS THE MANNUAL KEY, AND IS GATED DIRECTLY TO MCHTR BIT 4, THE SPECIAL GATING BUS IS NOT USED.

** BITS 19 THROUGH 16 OF THE SS ARE GATED DIERCTLY TO THE MCHTR (19 THROUGH 16), THE SPECIAL GATING BUS IS NOT USED.



STATE DIAGRAM OF THE MAIN SEQUENCER

CIRCUIT OPERATION

MCH MAIN SEQUENCER OPERATION

THE MAIN SEQUENCER IS RESPONSIBLE FOR THE BASIC CONTROL OF THE MCH CONTROLLER. OTHER THAN THE START-UP PROCEDURE, THE MCH CONTROLLER IS COMPLETELY AUTONOMOUS. THE STATE DIAGRAM OF THE MAIN MCH SEQUENCER IS SHOWN.

THE NORMAL OR REST STATE OF THE SEQUENCERS (BOTH ON-LINE AND OFF-LINE) IS THE MONITOR STATE. IN THIS STATE EACH MCH CONTROLLER IS ACTIVELY MONITORING ITS OWN INCOMING SERIAL DATA BUS. ANY INCOMING BIT STREAM WILL BE REGISTERED IN ITS SHIFT REGISTER INDEPENDENTLY OF THE STATUS OF ITS ASSOCIATED CC.

NORMAL TRANSMISSION

IN NORMAL OPERATION A TRANSMISSION IS INITIATED BY SOFTWARE. THE MCHC AND MCHTR ARE LOADED, THE STRT BIT IS SET, AND THE MOSTMCHO MICROINSTRUCTION IS ISSUED. THE LOAD OF THE MCHC REMOVES THE CONTROLLER FROM THE MONITOR STATE AND FORCES THE SEQUENCE REGISTER TO THE MASTER TRANSMIT STATE (MXMIT).

THE MDMCLSTO MICROINSTRUCTION (MISCELLANEOUS DECODER CROSSPOINT) SETS THE START BIT (STRT). THE TRANSMIT SEQUENCE IS INITIATED BY MICROINSTRUCTION MOSTMCHO. THE MCH CONTROLLER BEGINS TO SERIALLY OUTPULSE THE 30-BIT MESSAGE ALLOWING ZEROS TO FILL THE VACATED BIT POSITIONS IN THE SHIFT REGISTER, UNTIL AN ALL-ZERO FIELD EXISTS ACROSS THE MCHTR AND THE MCHC. THE SEQUENCER THEN ADVANCES TO THE MASTER RECEIVE STATE WHILE CONTINUING TO OUTPULSE AN ALL-ZERO DATA STREAM. IT CONTINUES TO DO SO UNTIL THIS STATE IS ABANDONED. THIS ALL-ZERO DATA STREAM IS USED BY THE RECEIVING CONTROLLER AS A TIMING SOURCE.

THE MCH CONTROLLER IN THE OTHER CC (IN THIS INSTANCE THE SLAVE CONTROLLER), STILL IN THE MONITOR STATE, BEGINS TO SHIFT IN THE DATA, DERIVING ITS CLOCKING FROM THE DATA STREAM, UNTIL START-BIT REGISTRATION IS OBTAINED, I.E., 30 BITS HAVE BEEN RECEIVED INTO ITS MCHTR/MCHC SHIFT REGISTER.

WITH THE START BIT EQUAL TO 1 AND THE MAIN SEQUENCER IN THE MONITOR STATE, THE SLAVE CONTROLLER ADVANCES TO THE SLAVE EXECUTE STATE (SXEQ). IN THIS STATE THE COMMAND FIELD (MCHC) IS DECODED AND THE RESULTING COMMAND EXECUTED. UPON DETECTION OF AN END-OF-COMMAND SIGNAL, THE SLAVE CONTROLLER FORCES THE RETURN CODE INTO THE MCHC, SETS THE STRT BIT EQUAL TO 1, CHECKS FOR DOUBLE OUTPUT ERRORS FROM THE MCH COMMAND TRANSLATOR, AND ADVANCES THE SEQUENCER TO THE SLAVE TRANSMIT STATE (SXMIT), ENABLING THE RETURN TRANSMISSION. THIS RETURN MESSAGE IS TRANSMITTED FROM ITS SHIFT REGISTER (MCHTR/MCHC) VIA TIMING DERIVED FROM THE STRING OF ZEROS (BIT STREAM TIMING) BEING SENT FORM THE MASTER CONTROLLER.

THE MASTER CONTROLLER, STILL IN THE MREC STATE AND STILL OUTPULSING ZEROS, DETECTS THE INCOMING RETURN MESSAGE AND BEGINS TO REGISTER IT IN ITS SHIFT REGISTER. UPON REGISTRATION OF THE START BIT, THE CONTROLLER GATES THE DATA FIELD (MCHTR) INTO THE MCHB, CEASES ITS ALL-ZERO OUTPULSING. AND DECODES THE RETURN CODE IN THE MCHC. THIS IN TURN, SETS THE RETURN BIT (RTN) IN THE MCH STATUS REGISTER. IF AN ERROR CODE WAS ALSO RETURNED, THE ERROR BIT (MCHERR) IN THIS REGISTER IS ALSO SET. HAVING ACCOMPLISHED THIS, THE WAIT STATE IS THEN ENTERED. MEANWHILE THE SLAVE CONTROLLER IN THE SXMIT STATE "SEES" THE INTERRUPTION OF THIS ZEROS-BIT STREAM AND INITIALIZES TO THE MONITOR STATE. LIKEWISE, THE MASTER SEQUENCER "SEES" ITS INCOMING BIT STREAM TERMINATE AND ALSO INITIALIZES TO THE MONITOR STATE. THE MCHB IS NOT INITIALIZED BY THIS SEQUENCE SINCE IT CONTAINS THE REPLY MESSAGE.

PART ØF FS 9
CØMPØSITE DIAGRAM 6

ISSUE 5A

3A CENTRAL CONTROL

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INCORPORATED

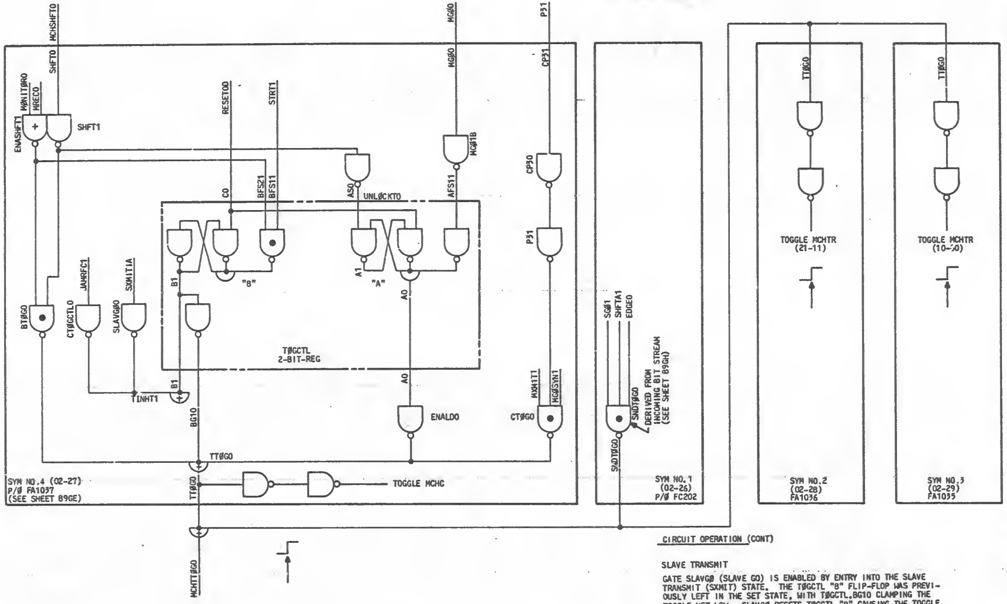
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 7

MCH TOGGLE CONTROL LOGIC



CIRCUIT OPERATION

COMPOSITE DIAGRAM 7 DETAILS THE ACTION OF THE TOGGLE CONTROL LOGIC.

MASTER TRANSMIT

THE FOLLOWING PROGRAM CONTROLLED SEQUENCE IS PERFORMED TO INITIATE A MCH TRANSMISSION TO THE OTHER CC. (SEE SHEET B9GK FOR TIMING DIAGRAM).

1. RESET COMMAND (MISCELLANEOUS DECODER SIGNAL MCHRSTO) IS EXECUTED, INITIALIZING THE CONTROL FLIP-FLOPS, TØGCTL "A" AND "B". TØGCTL.AO OUTPUT ENABLES GATE ENALDO CLAMPING THE TOGGLE NODE TTØGO (MCHTTØGO) LOW, PERMITTING THE SHIFT REGISTERS MCHTR AND MCHC TO BE PARALLEL LOADED.
2. THE MCHC IS PARALLEL LOADED AND IN THE PROCESS JAMS THE MCH SEQUENCE REGISTER TO THE TRANSMIT (MXMIT) STATE.
3. THE START BIT IS SET BY MISCELLANEOUS DECODER SIGNAL MDMCLSTO.
4. THE START CHANNEL COMMAND IS ISSUED. INPUT MGØO ACTIVATES ON THE TRAILING EDGE OF CLOCK PHASE P3, SETTING TØGCTL "A" DRIVING NODE TTØGO HIGH. THIS LOW-TO-HIGH TRANSITION CAUSES AN INITIAL DATA SHIFT FOR THE FINAL DATA REGISTRATION OF THE MESSAGE PRIOR TO OUTPUSLING. THE BUFFER BIT (MSDATA) IN THE BIPOLAR INTERFACE LOGIC (SHEET B9GH) HAS BEEN LOADED AND THE REMAINDER OF THE SERIAL MESSAGE IS REGISTERED WITH IT. MGØO ALSO CAUSES LEAD MGØSYN1 TO ACTIVATE AT THE LEADING EDGE OF THE FOLLOWING P1 CLOCK PHASE, WHICH ALLOWS GATE CTØGO TO TAKE CONTROL OF THE TOGGLE NODE. CTØGO, CLOCKED AT P3, WILL GENERATE A SERIES OF TOGGLE PULSES AT THE TRAILING EDGE OF EACH SEBSEQUENT P3. THE BIPOLAR PULSE IS FORMED ON FC202 (SEE SHEET B9GH).

MASTER RECEIVE

THE MREC STATE NOW ACTIVE, ALLOWS THE MCH TO MONITOR FOR A REPLY MESSAGE. LEAD MRECO ENABLES GATE ENASHFT1, REMOVING THE INHIBIT FROM GATE BTØGO. GATE BTØGO IS NOW FREE TO RESPOND TO THE ASYNCHROUS SHIFT PULSES DERIVED FROM THE BIT STREAM OF AN INCOMING SERIAL MESSAGE (INPUT MCHSHFTO). THE LEADING EDGE OF THE FIRST SHFTO PULSE, PRODUCED IN THE MREC STATE, DRIVES THE TOGGLE NODE (COLLECTOR TIE TTØGO) LOW ARMING THE "T1" INPUTS OF EACH SHIFT REGISTER CELL. THE TRAILING EDGE OF THIS PULSE THEN CAUSES THE DATA AT THE "0" INPUTS TO THESE CELLS TO BE ENTERED. THE SHFTO PULSE IS SYNCHRONIZED WITH THE SERIAL DATA INPUT LEAD. THIS SHIFTING ACTION CONTINUES UNTIL THE COMPLETE MESSAGE HAS BEEN RECEIVED, WITH THE START BIT OF THE MESSAGE REGISTERED IN THE LEAST SIGNIFICANT BIT POSITION OF THE SHIFT REGISTER (I.E. STRT=1). STRT BEING SET, SETS THE TØGCTL "B" FLIP-FLOP (MREC STATE STILL ACTIVE), WHICH CLAMPS THE TTØGO NODE LOW, IMMEDIATELY DISABLING ANY FURTHER INCOMING TOGGLES. THE WAIT STATE IS NOW ENTERED. NO FURTHER ACTION TAKES PLACE IN THIS MODE UNTIL A RESET PULSE IS RECEIVED ON EXTERNAL INPUT MCHRSTO FROM CIRCUIT PACK FC202. THIS RESET PULSE SIGNIFIES THE SUCCESSFUL INITIALIZATION OF THE MCH SEQUENCER IN THE OTHER CC. IT IS IMPORTANT TO NOTE THAT THIS RESET PULSE INITAILIZES THE MCH AND PLACES THE MCH SEQUENCER TO THE MONITOR STATE, BUT DOES NOT DESTROY THE JUST RECEIVED MESSAGE RESIDING IN THE MCH BUFFER REGISTER.

MONITOR (SEE SHEET B9GL FOR TIMING DIAGRAM)

THE QUIESCENT STATE OF THE MCH IS THE MONITOR STATE. THE TØGCTL FLIP-FLOPS ARE RESET CLAMPING THE TOGGLE NODE (TTØGO) LOW VIA GATE ENALDO. IN THIS STATE, THE MCH IS ACTIVELY MONITORING IN INCOMING SERIAL DATA BUS. GATE ENASHFT1 ENABLED BY LEAD MONITOR, ALLOWS GATE BTØGO (BUS TOGGLE) TO RESPOND TO ANY PULSING SEEN ON EXTERNAL INPUT SHFTO VIA GATE SHFT1. SHFTO IS THE STROBE PULSE DERIVED FROM INCOMING SERIAL DATA AND IS IN SYNCHRONISM WITH THE SERIAL DATA INPUT MCHRDO (SEE B9GC). AT THIS TIME, HOWEVER, THE OUTPUT OF GATE BTØGO IS CLAMPED LOW BY GATE ENALDO VIA COLLECTOR TIE TTØGO. THE INITIAL SHFTO PULSE (GROUND ACTIVE) SETS THE TØGCTL "A" FLIP-FLOP VIA GATE UNLOCKTO RELEASING CONTROL OF THE TTØGO NODE TO GATE BTØGO (BUS TOGGLE). THE GATE DELAYS INVOLVED (4 TO 1) GUARANTEE THAT THE TTØGO NODE REMAINS LOW DURING THIS TRANSITION OF CONTROL. THE TRAILING EDGE OF SHFTO CAUSES A LOW-TO-HIGH TRANSITION ON THE TTØGO NODE WHICH IN TURN, INITIATES A TOGGLE TO THE SHIFT REGISTER. THE REMAINDER OF THE TOGGLES ARE CONTROLLED BY BTØGO THROUGH SHFTO.

WHEN THE INCOMING MESSAGE IS FULLY REGISTERED IN THE SHIFT REGISTER, STRT BECOMES SET. STRT BEING SET COMBINED WITH THE MONITOR STATE ACTIVE, SETS THE TØGCTL "B" FLIP-FLOP CAUSING TØGCTL.BG10 TO IMMEDIATELY DRIVE AND HOLD THE TTØGO NET LOW. THIS CLAMP PREVENTS ADDITIONAL TOGGLE PULSES AFTER THE MESSAGE IS REGISTERED.

CIRCUIT OPERATION (CONT)

SLAVE TRANSMIT

GATE SLAVGØ (SLAVE GO) IS ENABLED BY ENTRY INTO THE SLAVE TRANSMIT (SXMIT) STATE. THE TØGCTL "B" FLIP-FLOP WAS PREVIOUSLY LEFT IN THE SET STATE, WITH TØGCTL.BG10 CLAMPING THE TOGGLE NET LOW. SLAVGØ RESETS TØGCTL "B" CAUSING THE TOGGLE NODE TTØGO TO GO POSITIVE ALLOWING THE MCH SHIFT REGISTER TO TOGGLE (SHIFT RIGHT ONE BIT POSITION). THIS ACTION ACCOMPLISHES TWO FUNCTIONS: 1) IT RELEASES THE INHIBIT ON THE TTØGO NET AND 2) IT ACCOMPLISHES FINAL DATA REGISTRATION OF THE OUTPUT MESSAGE (I.E., COMPENSATES FOR THE SERIAL BUFFER BIT LOCATED ON FC202 THROUGH WHICH THE SERIAL MESSAGE MUST PASS). ONCE THE TTØGO NET IS RELEASED BY SLAVGØO, SUBSEQUENT TOGGLES ARE GENERATED BY FC202 VIA A BACKPLANE COLLECTOR TIE ON THIS NODE (GATE SNDTØGO). THESE TOGGLES ARE DERIVED DIRECTLY FROM THE INCOMING BIT STREAM.

THE MCH SEQUENCER REMAINS IN THIS STATE, CONTINUOUSLY TRANSMITTING BEYOND THE END OF MESSAGE, UNTIL THE INCOMING BIT STREAM CEASES. WHEN THIS IS DETECTED, A RESET PULSE (MCHRSTO) IS GENERATED BY CIRCUIT PACK FC202 RETURNING THE MCH SEQUENCER TO THE MONITOR STATE.

PART ØF FS 9
CØMPØSITE DIAGRAM 7

ISSUE
5A

3A CENTRAL CONTROL

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BELL TELEPHONE LABORATORIES
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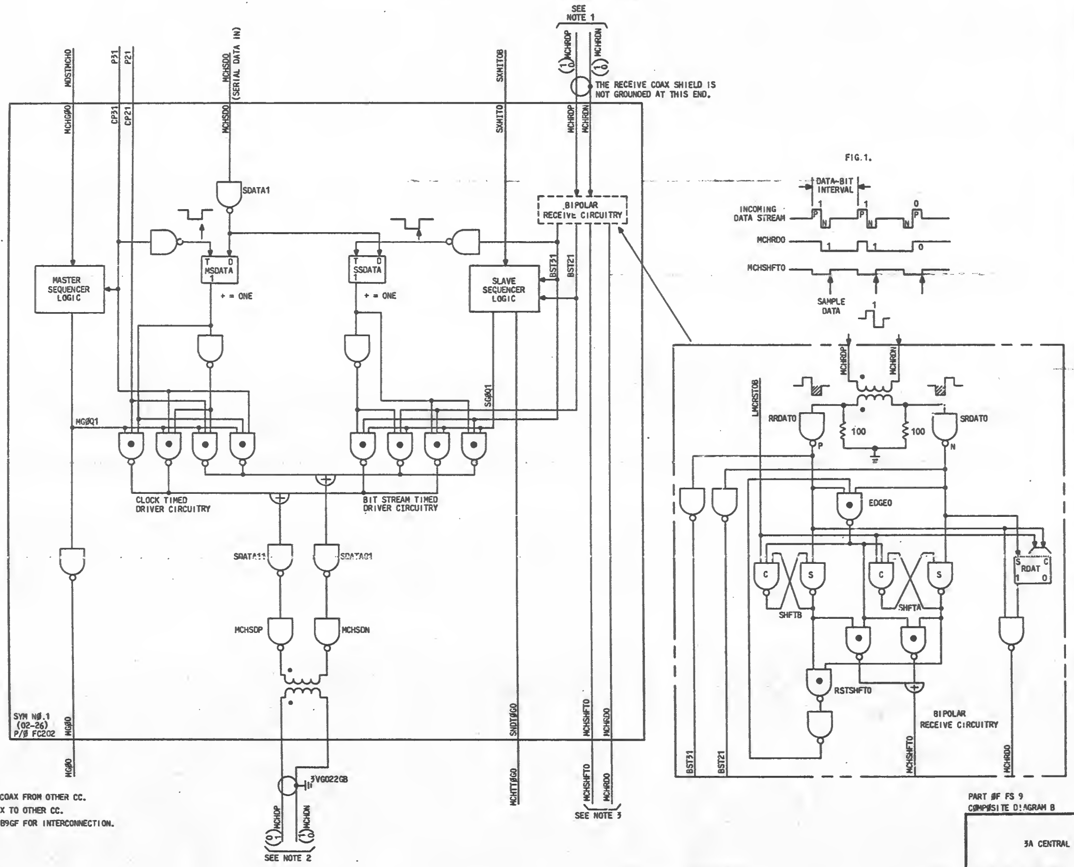
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 8

BIPOLAR INTERFACE



NOTES:

1. "RECEIVE" COAX FROM OTHER CC.
2. "SEND" COAX TO OTHER CC.
3. SEE SHEET B9GF FOR INTERCONNECTION.

CIRCUIT OPERATION

DRIVER CIRCUITRY

TO MINIMIZE THE TRANSMIT AND RECEIVE CIRCUITRV AND TO MAKE THE TRANSMISSION SCHEME INSENSITIVE TO THE TRANSMITTED DATA PATTERNS, TWO BIPOLAR PULSES ARE USED TO REPRESENT A SINGLE BIT OF DATA. EACH SERIAL BIT OF INFORMATION IS ENCODED INTO A DATA-BIT PAIR (SEE FIG. 1). THIS DATA-BIT PAIR CONSISTS OF TWO ADJACENT PULSES OF EQUAL AMPLITUDE BUT OF OPPOSITE POLARITY. PULSING THE TRANSMISSION LINE WITH TWO EQUAL AND OPPOSITE PULSES RESULTS IN MAINTAINING A ZERO VOLTAGE SHIFT IN THE GROUND REFERENCE LEVEL OVER THE LENGTH OF THE MESSAGE. EACH DATA-BIT, THEREFORE, PULSES AND FORCEFULLY RECOVERS THE LINE PRIOR TO THE NEXT DATA-BIT INTERVAL, REGARDLESS OF THE CHARACTERISTICS OF THE TRANSMISSION MEDIA.

TO FORM THE DATA-BIT PAIR, TWO HIGH FANOUT GATES ARE USED (MCHSDP, MCHSDN). THEIR TOTEM POLE OUTPUTS ARE CONNECTED IN A PUSH-PULL CONFIGURATION WITH THE PRIMARY OF THE DRIVER TRANSFORMER. THE ORDER IN WHICH THESE DRIVER GATES ARE PULSED DETERMINES THE PHASE RELATION, AND THEREFORE, THE DATA CONTENT, OF THE DATA-BIT PAIR.

TWO SETS OF DATA ENCODING GATES ARE PROVIDED. ONE SET IS FOR SYSTEM CLOCK-TIMED TRANSMISSIONS, AND ONE SET IS FOR BIT STREAM-TIMED TRANSMISSION. IN EITHER CASE, THE DATA TO BE TRANSMITTED IS PRESENTED TO THEIR RESPECTIVE SET OF ENCODING GATES FROM THE ASSOCIATED BUFFER FLIP-FLOP (MSDATA OR SSDATA), AND CLOCKED ACCORDINGLY. WHEN OPERATING IN THE BIT STREAM-TIMED MODE, THE INCOMING DATA STREAM IS A STRING OF ZEROS.

RECEIVER CIRCUITRY

THE RECEIVER GATES (SRDATO AND RRDATO) HAVE CLIPPING CIRCUITS ON THEIR INPUTS. THE BIPOLAR PULSE IS PRESENTED TO BOTH INPUT GATES 180° OUT OF PHASE WITH EACH OTHER. THE NEGATIVE PORTIONS OF THE BIPOLAR WAVE FORMS ARE REMOVED BY THE CLIPPING CIRCUITS TO PREVENT THE INPUTS FROM BEING DRIVEN BELOW GROUND. THE POSITIVE PORTIONS OF THE BIPOLAR WAVEFORM THEN SEQUENTIALLY DRIVE THE RECEIVER GATES, THE ORDER REFLECTING THE DATA CONTENT OF THE BIPOLAR WAVEFORM. THESE GATES DRIVE DIRECTLY INTO THE RDAT FLIP-FLOP, WHERE THE DATA CONTENT IS STORED. THE SHIFT LOGIC DETECTS THE PRESENCE OF THE DATA-BIT PAIR AND GENERATES A SHIFT PULSE (MCHSHFTO) IN SYNCHRONISM WITH THE RECONSTITUTED DATA (MCHRDO).

THE SHIFT PULSE, MCHSHFTO, IS GENERATED BY THE SHFT FLIP-FLOPS AND ASSOCIATED GATES. THE QUIESCENT STATE OF THESE FLIP-FLOPS ARE RESET, WITH MCHSHFTO POSITIVE (INACTIVE). THE FIRST LOBE OF A DATA-BIT PAIR ACTIVATES EITHER GATE, SRDATO OR RRDATO DEPENDING ON ITS DATA CONTENT. ASSUME A "ONE" IS ENTERING, GATE RRDATO RESPONDS TO THE FIRST LOBE OF THE DATA BIT PAIR, SETTING THE SHFT "B" FLIP-FLOP DRIVING THE MCHSHFTO COLLECTOR TIE TO GROUND. THE SECOND LOBE, DRIVING GATE SRDATO, SETS THE SHFT "A" FLIP-FLOP. GATE RSTSHFTO ACTIVATES AND REMOVES THE INHIBIT FROM GATE EDGEO. SRDATO, STILL GROUND, PREVENTS EDGEO FROM ACTIVATING UNTIL THE SECOND LOBE OF THE DATA-BIT PAIR IS PASSED. EDGEO, THEREFORE, ACTIVATES ON THE TRAILING EDGE OF THE SECOND LOBE OF THE DATA-BIT PAIR. EDGEO RESETS BOTH SHFT FLIP-FLOPS AND ALSO CAUSES MCHSHFTO TO PULSE POSITIVE WITHIN ONE GATE DELAV BECAUSE EDGEO DIRECTLY INHIBITS THE SHIFT OUTPUT GATES. WITHOUT THIS INHIBIT CONNECTION, IT WOULD REQUIRE 3 GATE DELAYS AFTER EDGEO ACTIVATES TO TURN OFF THE MCHSHFTO PULSE. THIS LOW-TO-HIGH TRANSITION ON OUTPUT LEAD MCHSHFTO CAUSES A DATA SHIFT IN THE MCHTR/MCHC SHIFT REGISTER.

PART ØF FS 9
CØMPØSITE DIAGRAM 8

ISSUE 5A

3A CENTRAL CONTROL ②

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NOTES:

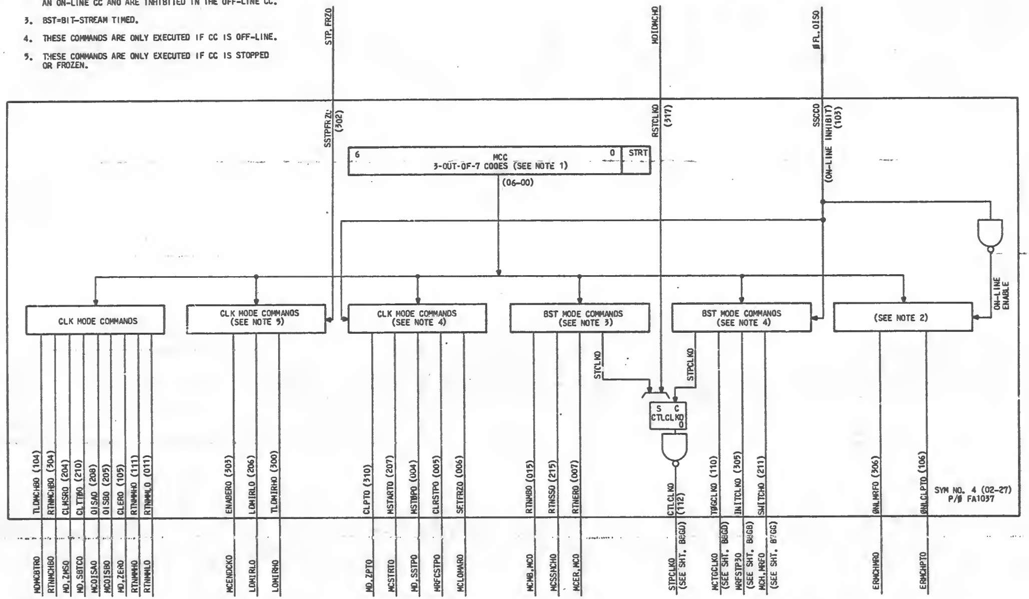
1. MCH CHANNEL CODES ARE NORMALLY REPRESENTED AS 4-OUT-OF-8 CODES. THE EXTRA 1 IS THE START BIT, BUT THIS BIT NEED NOT BE DECODED AS IT IS COMMON TO ALL CODES.
2. THESE MCH OUTPUTS CAUSE INTERRUPTS WHEN DECODED IN AN ON-LINE CC AND ARE INHIBITED IN THE OFF-LINE CC.
3. BST=BIT-STREAM TIMED.
4. THESE COMMANDS ARE ONLY EXECUTED IF CC IS OFF-LINE.
5. THESE COMMANDS ARE ONLY EXECUTED IF CC IS STOPPED OR FROZEN.

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 9

MCH COMMAND TRANSLATOR



CIRCUIT OPERATION

COMMANDS

THERE ARE TWO BASIC TYPES OF MCH COMMANDS: THE ONES WHICH CAN ONLY BE EXECUTED IF THE SYSTEM CLOCK IN THE CONTROLLED (SLAVE) CC IS RUNNING AND THE ONES WHICH CAN OPERATE INDEPENDENTLY OF THE SYSTEM CLOCK.

BECAUSE THERE ARE TWO TYPES OF COMMANDS, THE SLAVE SEQUENCE HAS TWO OPERATIONAL MODES IN THE SXEQ STATE. THEY ARE THE BIT STREAM TIMING MODE (BSTM) AND THE CLOCK TIMING MODE (CTM). FOR BSTM OPERATION ALL EXECUTION TIMING IS DERIVED FROM THE INCOMING BIT STREAM WHILE CTM OPERATION IS CARRIED OUT IN SYNC WITH THE CONTROLLED CC'S CLOCK.

THE COMMAND FIELD OF THE RECEIVED MESSAGE (MCC) CONTAINS A 3-OUT-OF-7 CODE. THE FIRST BIT OF THIS FIELD IS THE MODE SELECT BIT. OUT OF THE POSSIBLE 35 CODE COMBINATIONS AVAILABLE THE SIX BSTM COMMANDS WERE ASSIGNED FROM THAT SUBSET OF THE 35 WITH THE LEAST SIGNIFICANT BIT EQUAL TO 1. THE 17 CTM COMMANDS WERE ASSIGNED FROM THE REMAINING CODES WITH THE MODE BIT EQUAL TO 0. THIS MODE BIT IS GATED TO THE SEQUENCE LOGIC SETTING IT INTO THE PROPER CONFIGURATION (BSTM OR CTM) PRIOR TO ENTRY INTO THE SXEQ STATE.

FOR ADDED PROTECTION, CERTAIN COMMANDS ARE RESTRICTED TO OFF-LINE EXECUTION OR EXECUTION ONLY IN A STOPPED OR FROZEN PROCESSOR. FOR EXAMPLE, A COMMAND TO STOP THE CLOCK IN THE ON-LINE PROCESSOR WOULD NOT BE EXECUTED. THE FOLLOWING IS THE LIST OF MCH COMMANDS, THEIR 4-OUT-OF-8 CODES AND THEIR RESTRICTIONS.

MAINTENANCE CHANNEL COMMANDS

MNEMONIC	ACTION IN RECEIVING	CONDITIONAL ON	4-OUT-OF-8 CODE (HEX) (SEE NOTE 1)
CLER	CLEAR ERROR REGISTER		65
CLMSR	CLEAR MAINTENANCE STATES REGISTER		35
CLPT	CLEAR PROGRAM TIMER	CC=OFF-LINE	C5
CLTTO	CLEAR TIMER TIMEOUT REGISTER		20
DISA	IO DISABLE A		A5
DISB	IO DISABLE B		E1
INITCLK	INITIALIZE CLOCK (BST)+	CC=OFF-LINE	47
LDMAR	CLEAR STP;MAR←MCHTR;SET FREEZE	CC=OFF-LINE AND EITHER STOP OR FREEZE	4D
LDMCHB	MCHB←MCHTR	STOP OR FREEZE	99
LDMIRH	MIRH←MCHTR	STOP OR FREEZE	8D
LDMIRL	MIRL←MCHTR;EXECUTE ONE CYCLE	CC=OFF-LINE	.0
MSTART	CLEAR FREEZE	CC=OFF-LINE	C9
MSTOP	SET STOP FLIP-FLOP		D1
*RTNER	MCHTR←ER;TRANSMIT (BST)		88
*RTNMB	MCHTR←MB;TRANSMIT (BST)		A3
*RTNMCHB	MCHTR←MCHB;TRANSMIT		91
*RTNMMH	MCHTR←MMH;TRANSMIT		55
*RTNMML	MCHTR←MML;TRANSMIT		95
*RTNSS	MCHTR←SS;TRANSMIT (BST)		93
SPCLK	STOP THE CLOCK (BST)	CC=OFF-LINE	17
STCLK	START THE CLOCK (BST)		C3
SWITCH	HARDWARE INITIALIZATION(BST)	CC=OFF-LINE	0F
TOGCLK	TOGGLE CLOCK INPUT (BST)	CLK STOPPED	27

COMMAND DESCRIPTIONS

CLER - CLEARS THE OTHER CC'S ERROR REGISTER (ER).

CLMSR - CLEARS THE OTHER CC'S MAINTENANCE STATE REGISTER (MSR).

CLPT - CAUSES THE OTHER CC'S PROGRAM TIMER (PT) TO BE CLEARED. THIS COMMAND IS PERFORMED INDEPENDENTLY OF ANY NORMAL CC CONTROL OR DATA PATHS. IF THIS COMMAND IS ATTEMPTED IN AN ON-LINE PROCESSOR, THE COMMAND IS NOT EXECUTED AND AN ERROR SIGNAL IS GENERATED.

CLTTO - CLEARS THE TIMER TIMEOUT REGISTER (TTO) WHICH CLEARS THE BACK UP TIMING COUNTER (BTC) AFTER IT HAS BEEN SET FOR A FIXED PERIOD OF TIME. IN ORDER TO KEEP THE OTHER CC'S PROGRAM TIMER (PT) BLOCKED, THE TTO MUST BE CLEARED PERIODICALLY.

DISA - CAUSES THE FIRST DISABLE SIGNAL TO BE SENT TO THE OTHER CC'S DISABLE I/Ø CIRCUIT.

DISB - CAUSES THE SECOND DISABLE SIGNAL TO BE SENT TO THE OTHER CC'S DISABLE I/Ø CIRCUIT.

INITCLK - INITIALIZES THE CLOCK TO PHASE 3. THE RUNNING OR STOPPED STATUS OF THE CLOCK IS NOT AFFECTED BY THIS COMMAND.

* THESE COMMANDS REQUIRE A ZERO DATA FIELD FORMAT IN THE TRANSMITTED MESSAGE.

+ BST (BIT STREAM TIMING) SIGNIFIES CLOCK-INDEPENDENT COMMANDS.

CIRCUIT OPERATION (CONT)

RTNSS - RETURNS THE SYSTEM STATUS REGISTER (SS) FROM THE OTHER CC. THE SS IS GATED TO THE MCHTR AND TRANSMITTED BACK INDEPENDENTLY OF ANY NORMAL CC CONTROL OR DATA PATHS.

SPCLK - STOPS THE CLOCK WITH PHASE 3 ACTIVE. CC MUST BE OFF-LINE.

STCLK - STARTS THE CLOCK AT THE PHASE 3 TO PHASE 0 TRANSITION.

SWITCH - PERFORMS A HARDWARE INITIALIZATION OF THE OTHER CC IN ORDER TO SWITCH IT ON-LINE. THIS COMMAND IS PERFORMED ONLY IF THE CC FLIP-FLOP IS CLEARED (OFF-LINE). IF THE CC FLIP-FLOP IS SET (ON-LINE) THEN AN INTERRUPT IS GENERATED IN THE ON-LINE CC.

TOGCLK - CAUSES THE OTHER CC'S CLOCK TO BE ADVANCED ONE-HALF PHASE. THIS COMMAND IS USED WHEN THE OTHER CC'S CLOCK HAS BEEN STOPPED TO MANUALLY STEP IT THROUGH ALL OF ITS STATES.

CIRCUIT OPERATION (CONT)

MSTOP - SETS THE STOP FLIP-FLOP WHICH JAMS THE MAR TO A MAINTENANCE ADDRESS RESULTING IN ALL ZEROS BEING READ OUT OF THE MICROMEMORY. THIS COMMAND IS PERFORMED ONLY IF THE CC FLIP-FLOP IS CLEARED (OFF-LINE).

RTNER - RETURNS ERROR REGISTER (ER) FROM THE OTHER CC. THE ER IS GATED TO THE MCHTR AND TRANSMITTED BACK, INDEPENDENTLY OF ANY NORMAL CC CONTROL OR DATA PATHS.

RTNMB - RETURNS MISCELLANEOUS BITS (MB) FROM THE OTHER CC. THE MB IS GATED TO THE MCHTR AND TRANSMITTED BACK INDEPENDENTLY OF ANY NORMAL CC CONTROL OR DATA PATHS.

RTNMCHB - CAUSES THE CONTENTS OF THE MCHB IN THE OTHER CC'S MAINTENANCE CHANNEL TO GE GATED TO ITS MCHTR AND TRANSMITTED BACK.

RTNMMH - CAUSES THE HIGH 16 BITS OF THE MICROMEMORY WORD CURRENTLY ADDRESSED BY THE MICROADDRESS REGISTER (MAR) TO BE GATED TO THE MCHTR AND TRANSMITTED BACK.

RTNMML - CAUSES THE LOW 16 BITS OF THE MICROMEMORY WORD CURRENTLY ADDRESSED BY THE MICROADDRESS REGISTER TO BE GATED TO THE MCHTR AND TRANSMITTED BACK.

CIRCUIT OPERATION (CONT)

LDMAR - RESETS THE STOP FLIP-FLOP, LOADS THE OTHER CC'S MICROADDRESS REGISTER (MAR) WITH THE LOW 12 BITS OF THE DATA FIELD (MCHTR) AND SETS THE FREEZE FLIP-FLOP, FREEZING THE MAR CONTENTS. THE CONTROLLED CC MUST BE STOPPED PRIOR TO THIS COMMAND'S EXECUTION AND BE OFF-LINE.

LDMCHB - CAUSES THE 20-BIT DATA FIELD AND 2 PARITY BITS OF THE MCHTR TO BE LOADED INTO THE OTHER CC'S MAINTENANCE CHANNEL BUFFER REGISTER (MCHB).

LDMIRH - CAUSES THE DATA FIELD TO BE GATED TO THE OTHER CC'S MIR FOR ONE MICROCYCLE. THIS COMMAND IS EXECUTED ONLY IF THE OTHER CC IS STOPPED OR FROZEN.

LDMIRL - CAUSES THE DATA FIELD TO BE GATED TO THE MICROINSTRUCTION REGISTER (MIR) LOW 16 BITS AND THE RESULTANT TO- AND FROM-CONTROL FIELDS TO BE ACTIVE FOR A SINGLE CYCLE. THIS COMMAND IS EXECUTED ONLY IF THE OTHER IS STOPPED OR FROZEN.

MSTART - RESETS THE FREEZE FLIP-FLOP ALLOWING THE OTHER CC TO START PROCESSING MICROINSTRUCTIONS AT THE ADDRESS FROZEN IN THE MAR. THIS COMMAND IS PERFORMED ONLY IF THE CC FLIP-FLOP IS CLEARED (OFF-LINE).

PART ØF FS 9
COMPOSITE DIAGRAM 9

ISSUE 5A

3A CENTRAL CONTROL

SD-1C900-01-B9GJ

BELL TELEPHONE LABORATORIES
INCORPORATED

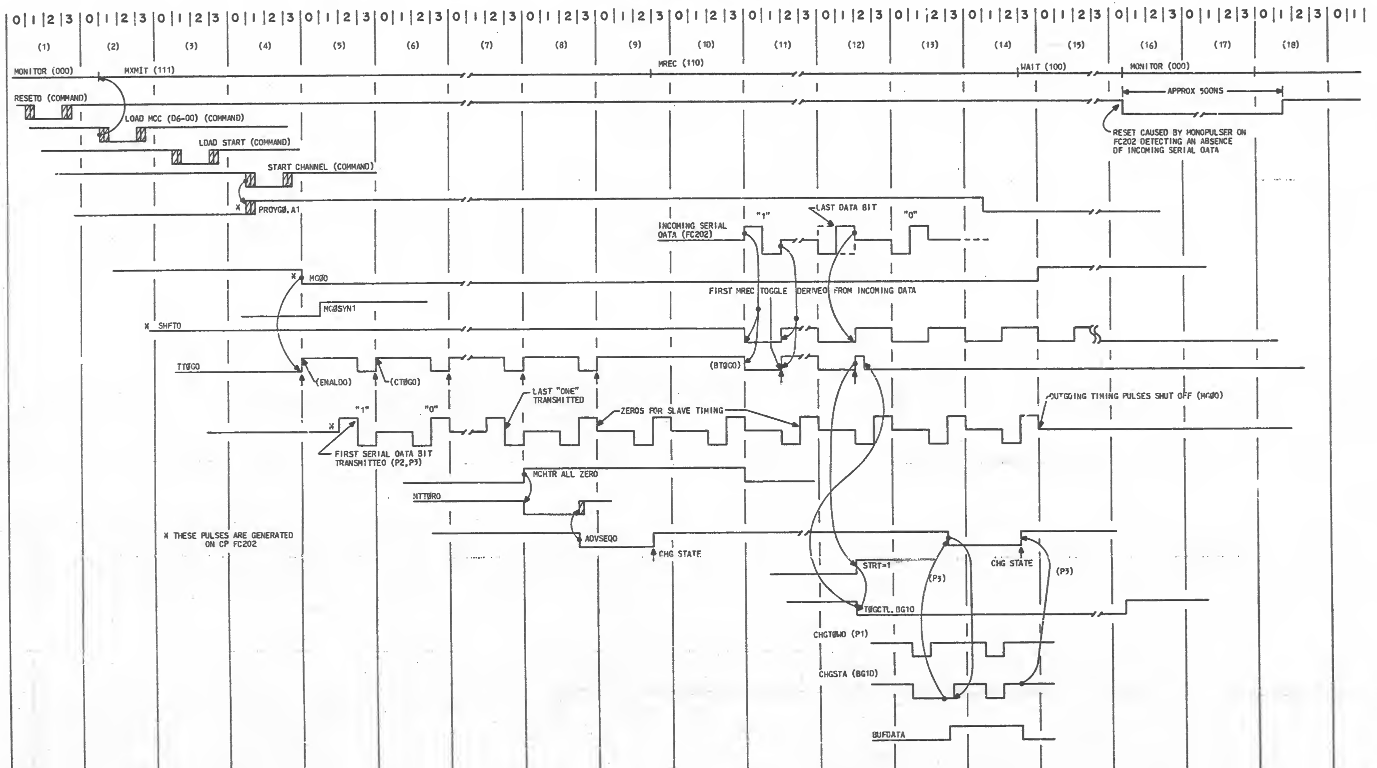
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 10

MASTER SEQUENCE-TIMING DIAGRAM



PART OF FS 9
COMPOSITE DIAGRAM 10

ISSUE
3A

3A CENTRAL CONTROL

②

SD-1C900-01-B9GK

BELL TELEPHONE LABORATORIES
INCORPORATED

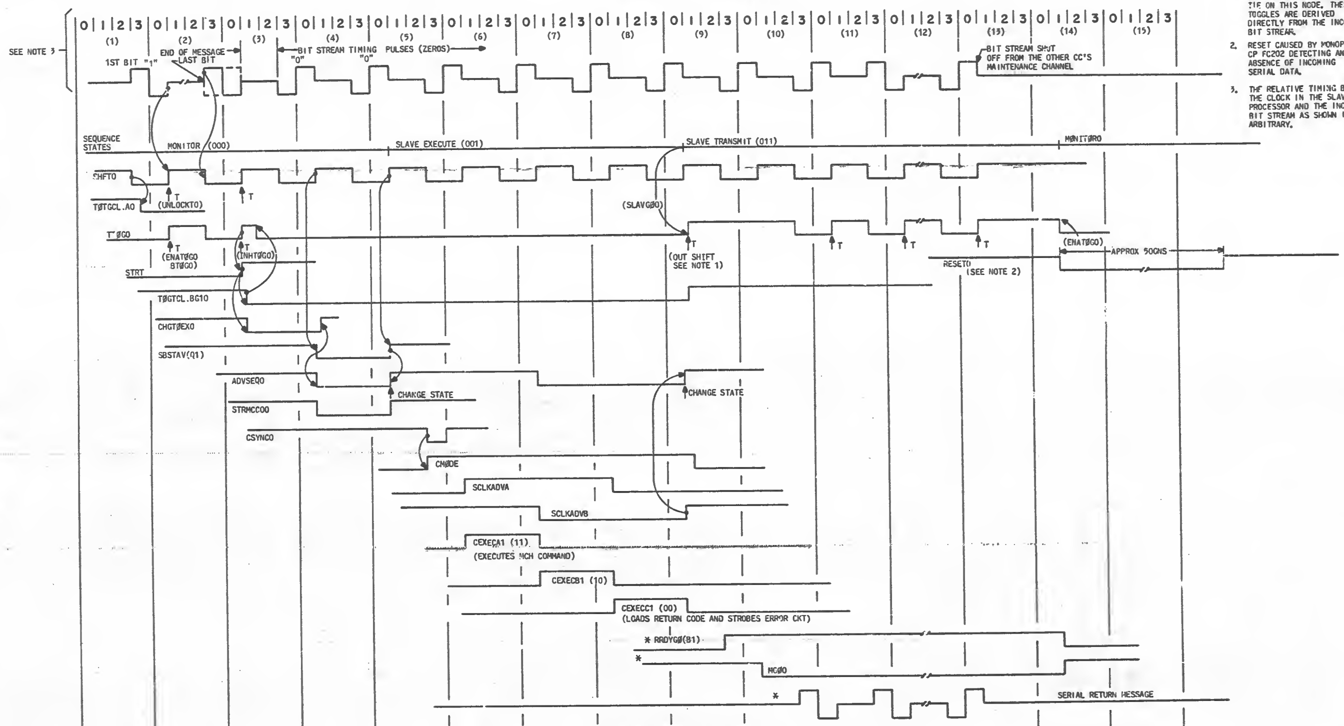
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM II

SLAVE SEQUENCE (CLOCK) - TIMING DIAGRAM



* THESE PULSES GENERATED ON CP FC202

NOTES:

1. ONCE TTØGO IS RELEASED BY SLAVE TRANSMIT (SXMIT1), THE SLAVE TRANSMIT TOGGLES ARE GENERATED BY FC202 VIA A BACKPLANE COLLECTOR TIE ON THIS NODE. THESE TOGGLES ARE DERIVED DIRECTLY FROM THE INCOMING BIT STREAM.
2. RESET CAUSED BY MONOPULSER ON CP FC202 DETECTING AN ABSENCE OF INCOMING SERIAL DATA.
3. THE RELATIVE TIMING BETWEEN THE CLOCK IN THE SLAVE PROCESSOR AND THE INCOMING BIT STREAM AS SHOWN IS ARBITRARY.

PART ØF FS 9
CØMPØSITE DIAGRAM 11

ISSUE
3A

3A CENTRAL CONTROL

SD-1C900-01-B9GL

BELL TELEPHONE LABORATORIES
INCORPORATED

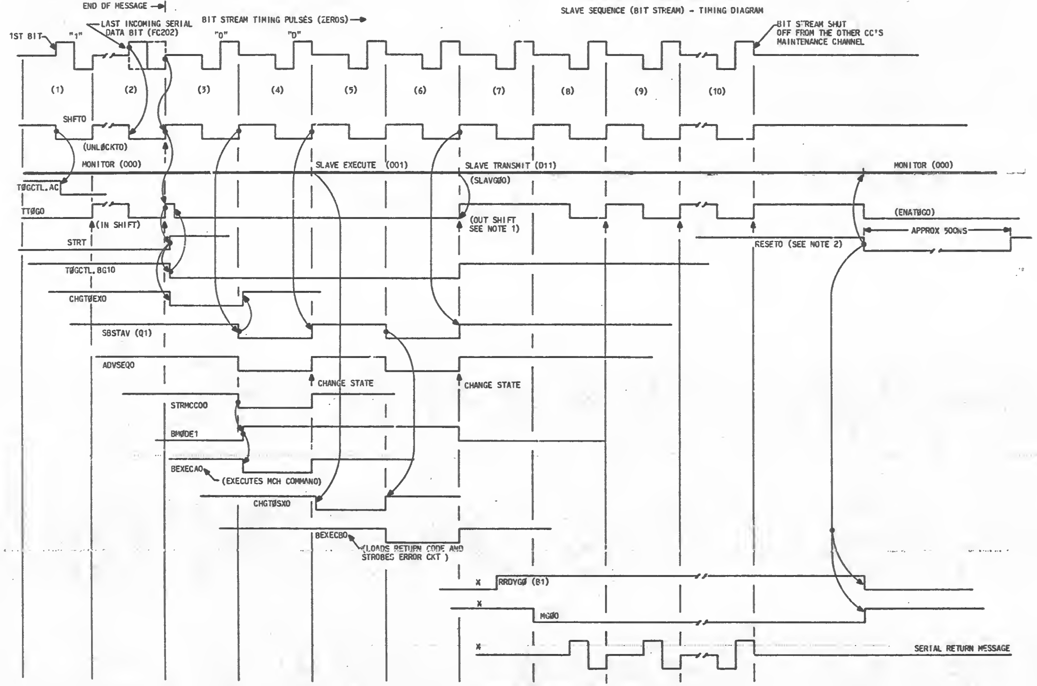
6S

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 12

SLAVE SEQUENCE (BIT STREAM) - TIMING DIAGRAM



X THESE PULSES GENERATED ON CP FC202

NOTES:

1. ONCE TT0GO IS RELEASED BY SLAVE TRANSMIT (SXMIT1), THE SLAVE TRANSMIT TOGGLES ARE GENERATED BY CP FC202 VIA A BACKPLANE COLLECTOR TIE ON THIS NODE. THESE TOGGLES ARE DERIVED DIRECTLY FROM THE INCOMING BIT STREAM.
2. RESET CAUSED BY MONOPULSER ON CP FC202 DETECTING AN ABSENCE OF INCOMING SERIAL DATA.

PART 0F FS 9
C0MP0SITE DIAGRAM 12

ISSUE
3A

3A CENTRAL CONTROL

SD-1C900-01-B9GM

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

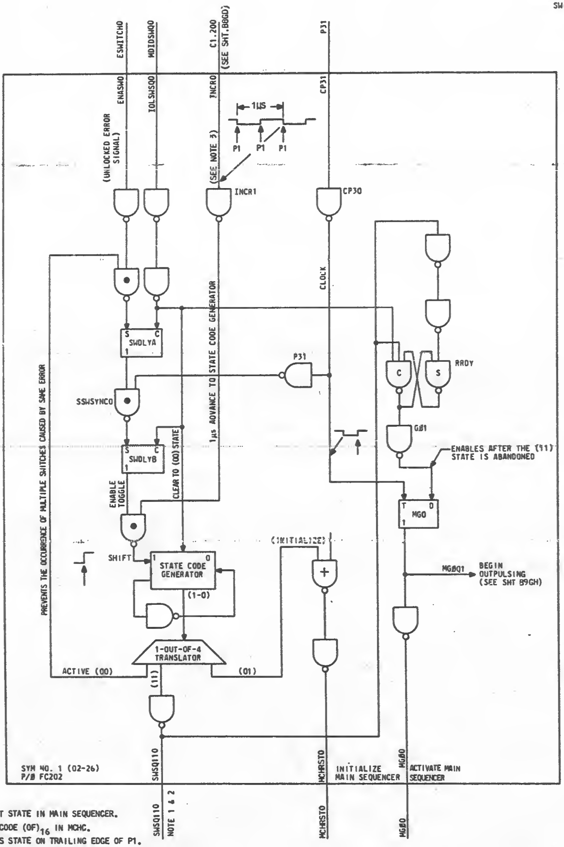
PRINTED IN U.S.A.

PART OF FS 9

MAINTENANCE CHANNEL

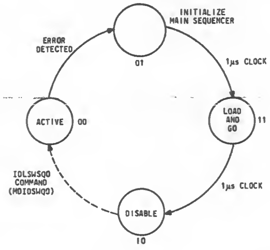
COMPOSITE DIAGRAM 13

SWITCH SEQUENCER



NOTES:

1. LOADS TRANSMIT STATE IN MAIN SEQUENCER.
2. LOADS SWITCH CODE $(OF)_{16}$ IN MCHC.
3. C1.200 CHANGES STATE ON TRAILING EDGE OF P1.



SWITCH SEQUENCER STATE DIAGRAM

FIG. 1

CIRCUIT OPERATION

SWITCH TRANSMISSION (SEE SHEET B9CP FOR TIMING DIAGRAM)

ANOTHER OPERATIONAL MODE OF THE MCH IS THE AUTOMATIC GENERATION OF THE "SWITCH" MESSAGE. IF AS A RESULT OF FATAL ERROR IN THE ON-LINE CC, A SYSTEM RECONFIGURATION IS NECESSARY, A SWITCH SIGNAL IS SENT TO ITS MCH CONTROLLER. SINCE THIS SIGNAL IS GENERATED BY A PROCESSOR IN TROUBLE (HARDWARE FAULT, PARITY ERROR, ETC.), THE MCH MUST RESPOND TO THIS FATAL ERROR SIGNAL AUTOMATICALLY WITH A CODED TRANSMISSION TO THE STAND-BY PROCESSOR TO ORDER IT TO SWITCH ITSELF ON-LINE AND TAKE OVER THE CALL PROCESSING RESPONSIBILITY. SINCE THIS SWITCH MESSAGE CAN OCCUR AT ANY TIME RELATIVE TO MCH OPERATION, IT HAS THE ABILITY TO ABORT ANY CURRENT MCH TRANSMISSION, INITIALIZE THE MAIN SEQUENCER, JAM THE MCH TO THE 3-OUT-OF-7 SWITCH CODE, SET THE STRT BIT, AND INITIATE THE SWITCH TRANSMISSION WITHOUT ANY EXTERNAL CONTROL OTHER THAN CLOCK FROM THE FAULTY PROCESSOR.

TO ACCOMPLISH THIS A SEPARATE SEQUENCER, THE SWITCH SEQUENCER, IS INCORPORATED INTO THE MCH CONTROLLER INDEPENDENTLY OF THE MAIN SEQUENCER. SEE FIG. 1 FOR THE STATE DIAGRAM. IN THE NORMAL OR ACTIVE STATE IT CONTINUALLY MONITORS THE ERROR BUS, ESWITCHO. UPON RECEIVING AN ERROR PULSE, IT SYNCS WITH A TIMING SOURCE (CLOCK-DERIVED) AND ENTERS AN INITIALIZATION STATE (INITIALIZE) WHERE THE MAIN SEQUENCER IS INITIALIZED (MCHRSTO). THE NEXT STATE (LOAD & GO) JAMS THE MCHC TO THE 3-OUT-OF-7 SWITCH CODE, SETS STRT, JAMS THE MAIN SEQUENCE REGISTER TO MXMIT, AND THEN ACTIVATES THE MAIN SEQUENCER (MGØO). FROM THIS POINT THE MAIN SEQUENCER TAKES COMMAND AND TRANSMITS THE SWITCH MESSAGE AS IF IT WERE A SOFTWARE INITIATED TRANSMISSION (SHEET B9GF). MEANWHILE, THIS SWITCH SEQUENCER CYCLES TO ITS NEXT STATE (DISABLE) WHERE IT REMAINS UNTIL INITIALIZED BY THE NEWLY ON-LINE PROCESSOR. THIS DISABLE STATE PREVENTS REPETITIVE SWITCH MESSAGES. THE SWITCH MESSAGE IS SENT ONLY ONCE.

SINCE THE MASTER SEQUENCER ADVANCES TO MREC AFTER OUTPULSING THE SWITCH MESSAGE, IT THEN EXPECTS A NORMAL RETURN MESSAGE TO RECYCLE IT TO THE MONITOR STATE. THIS IS WHERE THE NEWLY ON-LINE PROCESSOR CAN EXERCISE CONTROL, REQUEST STATUS INFORMATION, AND PERFORM ANY SUBSEQUENT DIAGNOSTICS. THE NEWLY ON-LINE PROCESSOR IS INITIALIZED BY THE DECODED SWITCH MESSAGE. BUT THE MCH, NOT DIRECTLY INITIALIZED BY THE SWITCH MESSAGE, IS NOT RESET UNTIL THE INITIALIZATION SEQUENCE IN THE MICROCODE IS PERFORMED. THIS DELAY IN RESETTING THE NEWLY ON-LINE MCH ALLOWS THIS MCH CONTROLLER TO BEGIN OUTPULSING A RETURN MESSAGE TO THE OTHER CC, THEREBY CAUSING THE OTHER CC TO INITIALIZE TO THE MONITOR STATE WHEN THIS MESSAGE IS INTERRUPTED. AT THIS POINT, BOTH MCH CONTROLLERS ARE IN THE MONITOR STATE AND NORMAL COMMUNICATION MAY BE INITIATED. BEFORE RESTORING THE SWITCH SEQUENCER TO THE ACTIVE STATE, THE SOURCE OF THE ERROR MUST BE REMOVED TO PREVENT SUBSEQUENT SWITCH TRANSMISSIONS.

PART ØF FS 9
CØMPØSITE DIAGRAM 13

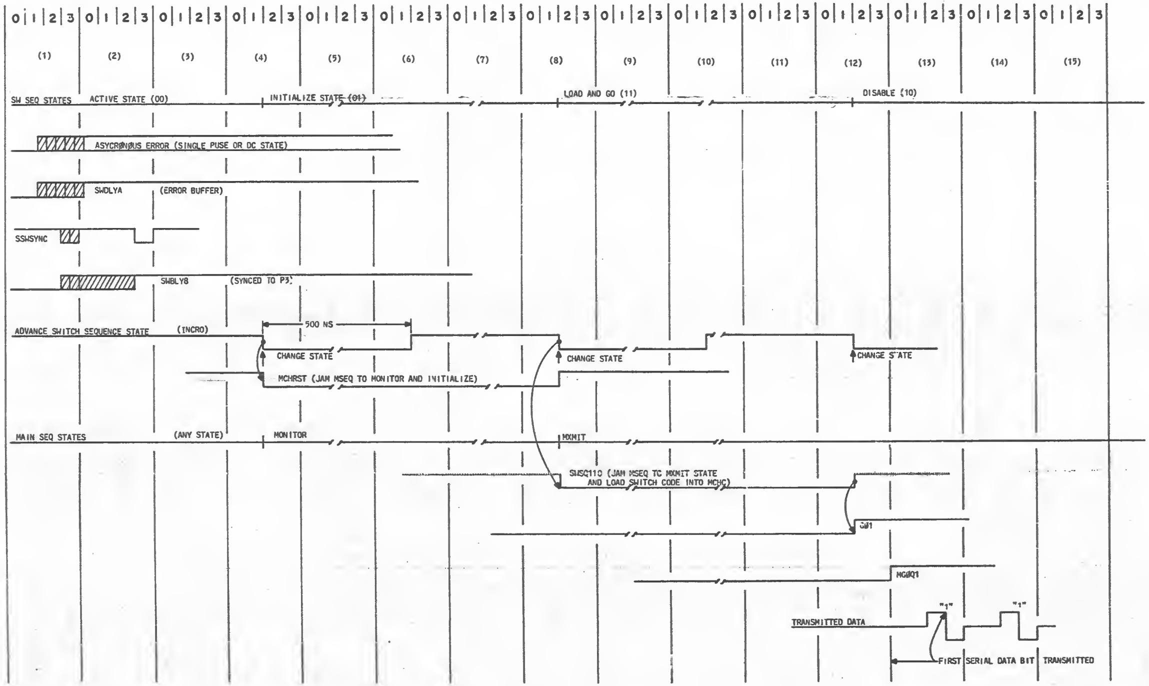
3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B9GN

PART OF FS 9

MAINTENANCE CHANNEL

COMPOSITE DIAGRAM 14

SWITCH SEQUENCE-TIMING DIAGRAM



CONTINUED ON SHEET B9GK TO COMPLETE SEQUENCE

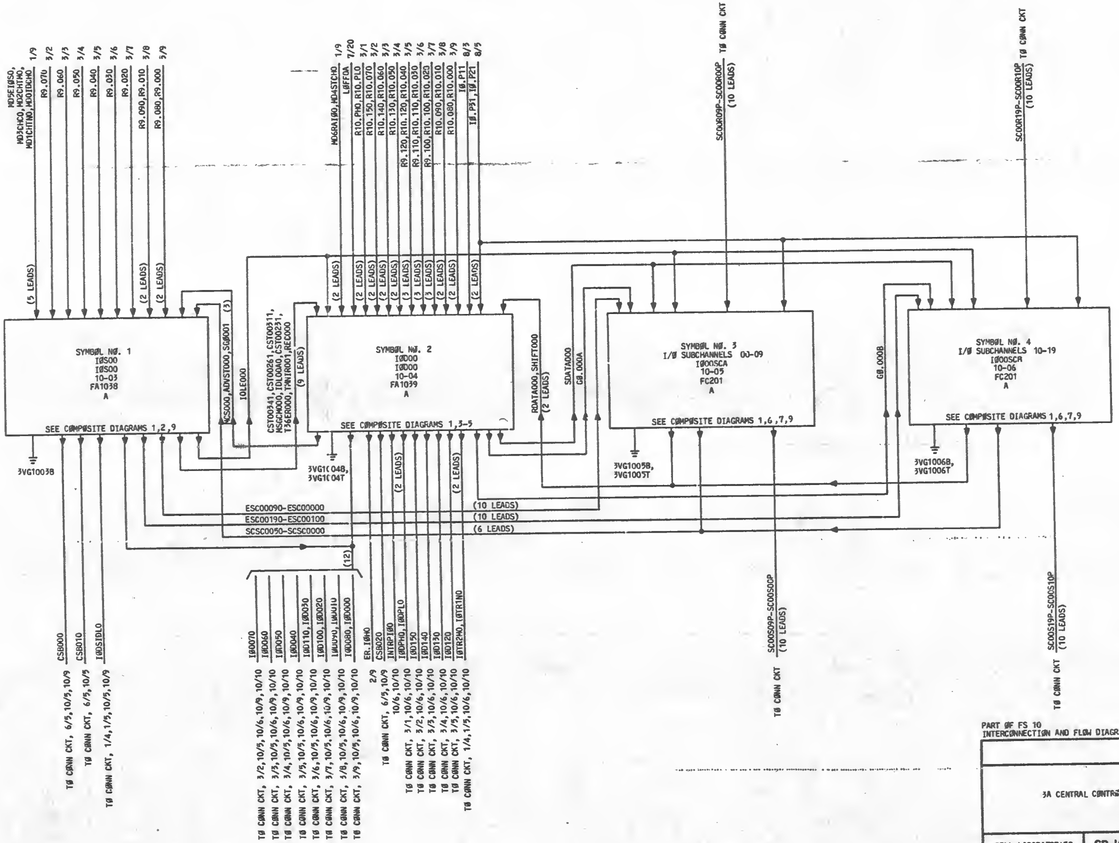
PART OF FS 9
COMPOSITE DIAGRAM 14

3A CENTRAL CONTROL	SD-1C900-01-B9GP
BELL TELEPHONE LABORATORIES INCORPORATED	6S

ISSUE 3A

PART OF FS 10

I/Ø CHANNELS
INTERCØNNECTIØN AND FLØW DIAGRAM



MD5EIØSO, MD3CHCO, MD2CHTMO, MD1CHTNO, MD0IDCHO 1/9
R9.070 3/2
R9.060 3/3
R9.050 3/4
R9.040 3/5
R9.030 3/6
R9.020 3/7
R9.090, R9.010 3/8
R9.080, R9.000 3/9
(5 LEADS)
(2 LEADS)
(2 LEADS)
MD6RAIØO, MD4STCHO 1/9
LØFFOA 7/20
R10.PHO, R10.PLO 3/1
R10.150, R10.070 3/2
R10.140, R10.060 3/3
R10.130, R10.050 3/4
R9.120, R10.120, R10.040 3/5
R9.110, R10.110, R10.030 3/6
R9.100, R10.100, R10.020 3/7
R10.090, R10.010 3/8
R10.080, R10.000 3/9
IØ.P11 8/3
IØ.P31, IØ.P21 8/5
(2 LEADS)
(3 LEADS)
SCOOR09P-SCOOROOP (10 LEADS) TØ CØNN CKT
SCOOR19P-SCOOR10P (10 LEADS) TØ CØNN CKT
SYMBØL NØ. 1
IØS00
IØS00
10-03
FA1038
A
SEE CØMPØSITE DIAGRAMS 1,2,9
MCS000, ADVST000, SGØ001 (3)
IOLE000
CST00341, CST00261, CST00311, MSGCM000, IDL00A0, CST00231, T36ER000, TMNIR001, REC000 (9 LEADS)
SYMBØL NØ. 2
IØD00
IØD00
10-04
FA1039
A
SEE CØMPØSITE DIAGRAMS 1,3-5
RDATA000, SHIFT000 (2 LEADS)
SDATA000
GØ.000A
SYMBØL NØ. 3
I/Ø SUBCHANNELS 00-09
IØ00SCA
10-05
FC201
A
SEE CØMPØSITE DIAGRAMS 1,6,7,9
GØ.000B
SYMBØL NØ. 4
I/Ø SUBCHANNELS 10-19
IØ00SCR
10-06
FC201
A
SEE CØMPØSITE DIAGRAMS 1,6,7,9
3VG1003B
3VG1C04B, 3VG1C04T
3VG1005B, 3VG1005T
3VG1006B, 3VG1006T
ESC00090-ESC00000 (10 LEADS)
ESC00190-ESC00100 (10 LEADS)
SCSC0050-SCSC0000 (6 LEADS)
(12)
CSB000 TØ CØNN CKT, 6/5,10/5,10/9
CSB010 TØ CØNN CKT, 6/5,10/5
IØDSTBLO TØ CØNN CKT, 1/4,1/5,10/5,10/9
IØD070 TØ CØNN CKT, 3/2,10/5,10/6,10/9,10/10
IØD060 TØ CØNN CKT, 3/3,10/5,10/6,10/9,10/10
IØD050 TØ CØNN CKT, 3/4,10/5,10/6,10/9,10/10
IØD040 TØ CØNN CKT, 3/5,10/5,10/6,10/9,10/10
IØD110, IØD030 TØ CØNN CKT, 3/6,10/5,10/6,10/9,10/10
IØD100, IØD020 TØ CØNN CKT, 3/7,10/5,10/6,10/9,10/10
IØD090, IØD010 TØ CØNN CKT, 3/8,10/5,10/6,10/9,10/10
IØD080, IØD000 TØ CØNN CKT, 3/9,10/5,10/6,10/9,10/10
ER.IØHO 2/9
CSB020 TØ CØNN CKT, 6/5,10/9
INTRPIØ0 10/6,10/10
IØDPHO, IØDPLO
IØD150 TØ CØNN CKT, 3/1,10/6,10/10
IØD140 TØ CØNN CKT, 3/2,10/6,10/10
IØD130 TØ CØNN CKT, 3/3,10/6,10/10
IØD120 TØ CØNN CKT, 3/4,10/6,10/10
IØTR2HO, IØTR1NO TØ CØNN CKT, 3/5,10/6,10/10
TØ CØNN CKT, 1/4,1/5,10/6,10/10
(2 LEADS)
(2 LEADS)
SC00S09P-SC00S00P (10 LEADS) TØ CØNN CKT
SC00S19P-SC00S10P (10 LEADS) TØ CØNN CKT

PART ØF FS 10
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL ②

DWG SIZE 6S

ISSUE 3A

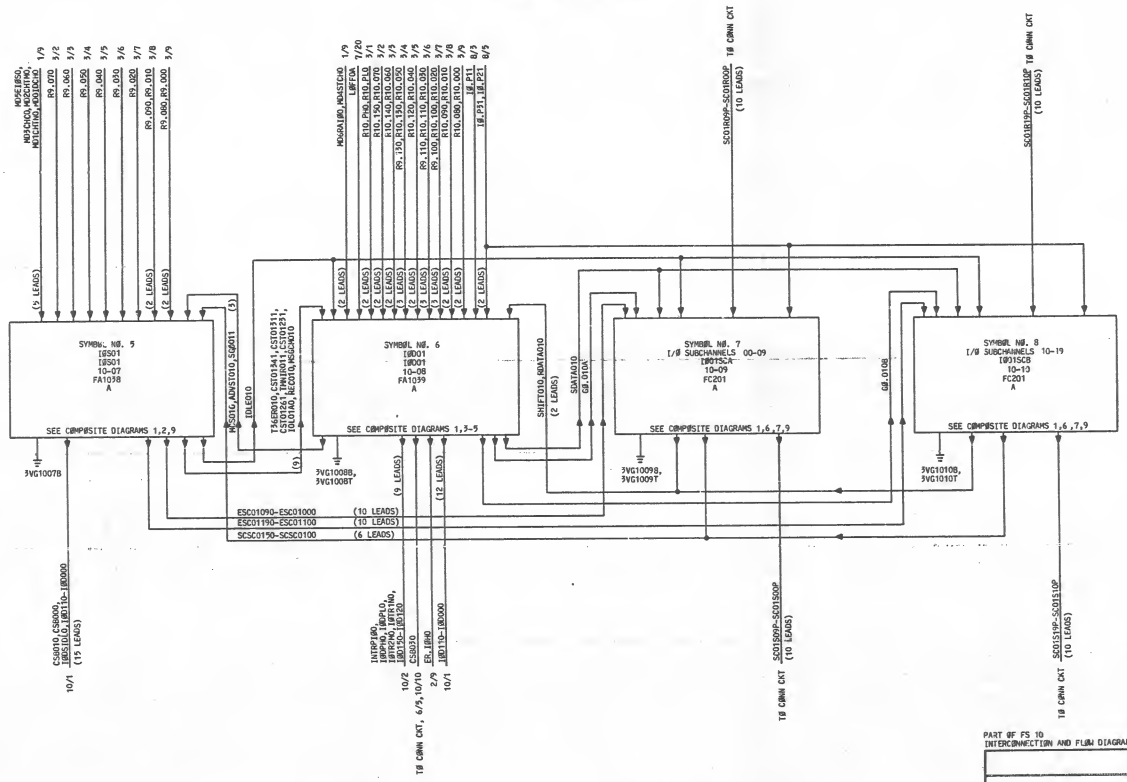
BELL LABORATORIES

SD-1C900-01

BIOAA

PART OF FS 10

I/Ø CHANNELS
INTERCØNNECTIØN AND FLØW DIAGRAM



PART ØF FS 10
INTERCØNNECTIØN AND FLØW DIAGRAM

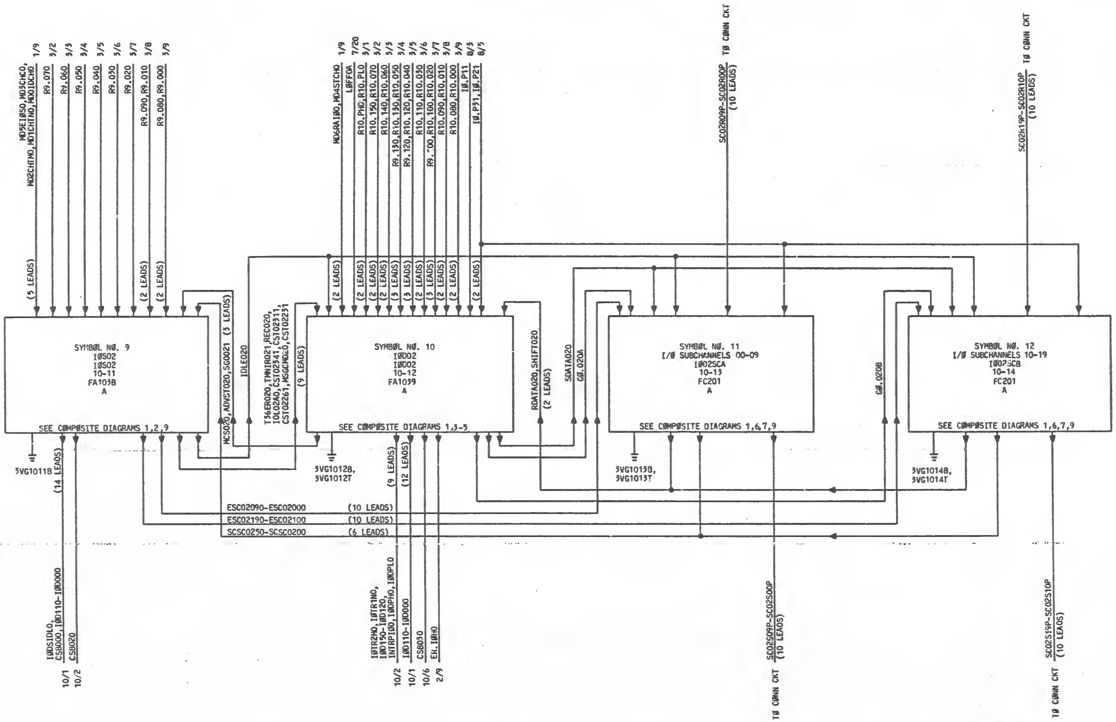
3A CENTRAL CØNTRØL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	BIOAB

PRINTED IN U.S.A.

E-7021 (12-73)

PART OF FS 10

I/Ø CHANNELS
INTERCØNNECTIØN AND FLØW DIAGRAM



PART ØF FS 10
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL

DWG SIZE 5S

ISSUE 5A

BELL LABORATORIES SD-1C900-01 BIOAC

PRINTED IN U.S.A.

PART OF FS 10

I/O CHANNELS

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ADVST000	ADVANCE SEQUENCER CONTROL LEAD - I/O MAIN CHANNEL 0 (INTERNAL)
ADVST010	ADVANCE SEQUENCER CONTROL LEAD - I/O MAIN CHANNEL 1 (INTERNAL)
ADVST020	ADVANCE SEQUENCER CONTROL LEAD - I/O MAIN CHANNEL 2 (INTERNAL)
CSB000-CSB030	I/O MAIN CHANNEL'S 3 OUT OF 6 RETURN CHECK CODE BITS 0-3
CST00231	I/O MAIN CHANNEL "0", DECODED I/O SEQUENCER STATE - LOADED RECEIVE (INTERNAL)
CST00261	I/O MAIN CHANNEL "0", DECODED I/O SEQUENCER STATE - LOADED MESSAGE COMPLETE (INTERNAL)
CST00311	I/O MAIN CHANNEL "0", DECODED I/O SEQUENCER STATE - TRANSMIT MAINTENANCE (INTERNAL)
CST00341	I/O MAIN CHANNEL "0", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST01231	I/O MAIN CHANNEL "1", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST01261	I/O MAIN CHANNEL "1", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST01311	I/O MAIN CHANNEL "1", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST01341	I/O MAIN CHANNEL "1", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST02231	I/O MAIN CHANNEL "2", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST02261	I/O MAIN CHANNEL "2", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST02311	I/O MAIN CHANNEL "2", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
CST02341	I/O MAIN CHANNEL "2", DECODED I/O SEQUENCER STATE - TRANSMIT NORMAL (INTERNAL)
ER.IOH0	I/O CHANNEL ERROR (I/O DML MATCH ERROR, 3 OUT OF 6 SUBCHANNEL SELECT OR CONTROL STATES ERROR)
ESC00000-ESC00190	ENABLE MAIN CHANNEL 0 SUBCHANNEL 0-19 (INTERNAL)
ESC01000-ESC01190	ENABLE MAIN CHANNEL 1 SUBCHANNEL 0-19 (INTERNAL)
ESC02000-ESC02190	ENABLE MAIN CHANNEL 2 SUBCHANNEL 0-19 (INTERNAL)
GO.000A	CONTROL OUTPULSING ON I/O MAIN CHANNEL 0, SUBCHANNELS 0-9 (INTERNAL)
GO.000B	CONTROL OUTPULSING ON I/O MAIN CHANNEL 0, SUBCHANNELS 10-19
GO.010A	CONTROL OUTPULSING ON I/O MAIN CHANNEL 1, SUBCHANNELS 0-9 (INTERNAL)
GO.010B	CONTROL OUTPULSING ON I/O MAIN CHANNEL 1, SUGCHANNELS 10-19 (INTERNAL)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
GO.020A	CONTROL OUTPULSING ON I/O MAIN CHANNEL 2, SUBCHANNELS 0-9 (INTERNAL)
GO.020B	CONTROL OUTPULSING ON I/O MAIN CHANNEL 2, SUBCHANNELS 10-19 (INTERNAL)
IDLE000	BUFFERED MISC. DECODER CROSSPOINTS, I/O MAIN CHANNEL 0 (INTERNAL)
IDLE010	BUFFERED MISC. DECODER CROSSPOINTS, I/O MAIN CHANNEL 1 (INTERNAL)
IDLE020	BUFFERED MISC. DECODER CROSSPOINTS, I/O MAIN CHANNEL 2 (INTERNAL)
IDL00A0	DEFINES THE LOAD I/O INTERVAL INTO I/O MAIN CHANNEL 0 (INTERNAL)
IDL01A0	DEFINES THE LOAD I/O INTERVAL INTO I/O MAIN CHANNEL 1 (INTERNAL)
IDL02A0	DEFINES THE LOAD I/O INTERVAL INTO I/O MAIN CHANNEL 2 (INTERNAL)
INTRPI00	INTERRUPT FROM IO MAIN CHANNELS 0, 1, 2
IO.P11	P1 CLOCK TO IO CHANNELS
IO.P21	P2 CLOCK TO IO CHANNELS
IO.P31	P3 CLOCK TO IO CHANNELS
IODPH0	PARITY HIGH OF THE IOD REGISTER
IODPL0	PARITY LOW OF THE IOD REGISTER
IODSIDL0	IDLE STATUS CONDITION FROM IO CHANNELS TO THE DS BIT
IOD000-IOD150	BITS 0-15 OF THE IOD REGISTER
IOTR1N0	IO MESSAGE COMPLETE FLAG - NORMAL. FROM IO CHANNELS TO TR1 BIT.
IOTR2M0	IO MESSAGE COMPLETE FLAG - MAINTENANCE. FROM IO CHANNELS TO TR2 BIT.
LOFF0A	LOCK OFF-LINE OR DISABLE INDICATION (DISABLES IO)
MCS000	DECODED I/O MAIN CHANNEL "0" SELECT SIGNAL (INTERNAL)
MCS010	DECODED I/O MAIN CHANNEL "1" SELECT SIGNAL (INTERNAL)
MCS020	DECODED I/O MAIN CHANNEL "2" SELECT SIGNAL (INTERNAL)
MD0IDCH0	MISC. DECODER, IDLE THE SELECTED I/O CHANNEL
MD1CHTN0	MISC. DECODER, LOAD THE SELECTED I/O CHANNEL WITH TRANSMIT NORMAL STATE CODE
MD2CHTM0	MISC. DECODER, LOAD THE SELECTED I/O CHANNEL WITH TRANSMIT MAINTENANCE STATE CODE
MC3CHC0	MISC. DECODER, LOAD THE SELECTED I/O CHANNEL SEQUENCER WITH THE CONTROL FIELD DEFINED BY THE LOW 4 BITS OF GENERAL REGISTER 9
MD4STCH0	MISC. DECODER, START THE SELECTED I/O CHANNEL
MD5EIOS0	MISC. DECODER, ENABLE THE OUTPUTS OF THE IOS REGISTER TO BE ORED WITH THE OUTPUTS OF THE IOD IN THE SELECT I/O CHANNEL (MAINTENANCE ONLY)
MD6RAI00	MISC. DECODER, ENABLE GATING FROM R10 TO THE IOD REGISTER IN THE SELECTED I/O CHANNEL

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MSGCM000	"OR" OF MESSAGE COMPLETE STATES IN I/O MAIN CHANNEL 0 (INTERNAL)
MSGCM010	"OR" OF MESSAGE COMPLETE STATES IN I/O MAIN CHANNEL 1 (INTERNAL)
MSGCM020	"OR" OF MESSAGE COMPLETE STATES IN I/O MAIN CHANNEL 2 (INTERNAL)
RDATA000	SERIAL INPUT DATA TO THE IOD DATED OF I/O MAIN CHANNEL 0 (INTERNAL)
RDATA010	SERIAL INPUT DATA TO THE IOD OF I/O MAIN CHANNEL 1 (INTERNAL)
RDATA020	SERIAL INPUT DATA TO THE IOD OF I/O MAIN CHANNEL 2 (INTERNAL)
REC000	"OR" OF RECEIVE STATES IN I/O MAIN CHANNEL 0 (INTERNAL)
REC010	"OR" OF RECEIVE STATES IN I/O MAIN CHANNEL 1 (INTERNAL)
REC020	"OR" OF RECEIVE STATES IN I/O MAIN CHANNEL 2 (INTERNAL)
R10.PH0	PARITY HIGH OF GENERAL REGISTER 10
R10.PL0	PARITY LOW OF GENERAL REGISTER 10
R10.000-R10.150	BITS 0-15 OF GENERAL REGISTER 10
R9.000-R9.130	BITS 0-13 OF GENERAL REGISTER 9
SCSC0000-SCSC0050	I/O MAIN CHANNELS 0, SUBCHANNEL SELECT 3 OUT OF 6 CODE CHECK (BITS 0-5) (INTERNAL)
SCSC0100-SCSC0150	I/O MAIN CHANNEL 1, SUBCHANNEL SELECT 3 OUT OF 6 CODE CHECK (BITS 0-5) (INTERNAL)
SCSC0200-SCSC0250	I/O MAIN CHANNEL 2, SUBCHANNEL SELECT 3 OUT OF 6 CODE CHECK (BITS 0-5) (INTERNAL)
SC00R00P-SC00R19P	I/O MAIN CHANNEL 0, SUBCHANNELS 0-19 RECEIVE INPUTS (TRANSFORMER INPUTS - POSITIVE)
SC00S00P-SC00S19P	I/O MAIN CHANNEL 0, SUBCHANNELS 0-19 SEND OUTPUTS (TRANSFORMER OUTPUTS - POSITIVE)
SC01R00P-SC01R19P	I/O MAIN CHANNEL 1, SUBCHANNELS 0-19 RECEIVE INPUTS (TRANSFORMER OUTPUTS - POSITIVE)
SC01S00P-SC01S19P	I/O MAIN CHANNEL 1, SUBCHANNEL 0-19 SEND OUTPUTS (TRANSFORMER OUTPUTS - POSITIVE)
SC02R00P-SC02R19P	I/O MAIN CHANNEL 2, SUBCHANNEL 0-19 RECEIVE INPUTS (TRANSFORMER OUTPUTS - POSITIVE)
SC02S00P-SC02S19P	I/O MAIN CHANNEL 2, SUBCHANNEL 0-19 SEND OUTPUTS (TRANSFORMER OUTPUTS - POSITIVE)
SDATA000	I/O MAIN CHANNEL 0, SEND DATA SERIAL OUTPUT FROM IOD (INTERNAL)
SDATA010	I/O MAIN CHANNEL 1, SEND DATA SERIAL OUTPUT FROM IOD (INTERNAL)
SDATA020	I/O MAIN CHANNEL 2, SEND DATA SERIAL OUTPUT FROM IOD (INTERNAL)
SG0001	BEGIN TRANSMIT SIGNAL FOR I/O MAIN CHANNEL 0 (INTERNAL)
SG0011	BEGIN TRANSMIT SIGNAL FOR I/O MAIN CHANNEL 1 (INTERNAL)
SG0021	BEGIN TRANSMIT SIGNAL FOR I/O MAIN CHANNEL 2 (INTERNAL)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SHIFT000	INCOMING SHIFT LEAD TO IOD FOR I/O MAIN CHANNEL 0 (INTERNAL)
SHIFT010	INCOMING SHIFT LEAD TO IOD FOR I/O MAIN CHANNEL 1 (INTERNAL)
SHIFT020	INCOMING SHIFT LEAD TO IOD FOR I/O MAIN CHANNEL 2 (INTERNAL)
TMNIR001	I/O MAIN CHANNEL 0, TRANSMIT MAINTENANCE, TRANSMIT NORMAL, IDLE OR RECEIVE STATE (INTERNAL)
TMNIR011	I/O MAIN CHANNEL 1, TRANSMIT MAINTENANCE, TRANSMIT NORMAL, IDLE, OR RECEIVE STATE (INTERNAL)
TMNIR021	I/O MAIN CHANNEL 2, TRANSMIT MAINTENANCE, TRANSMIT NORMAL, IDLE, OR RECEIVE STATES (INTERNAL)
T36ER000	I/O MAIN CHANNEL 0, 3 OUT OF 6 CODE CHECK OF I/O SUBCHANNELS AND CONTROL STATES (INTERNAL)
T36ER010	I/O MAIN CHANNEL 1, 3 OUT OF 6 CODE CHECK OF I/O SUBCHANNELS AND CONTROL STATES (INTERNAL)
T36ER020	I/O MAIN CHANNEL 2, 3 OUT OF 6 CODE CHECK OF I/O SUBCHANNELS AND CONTROL STATES (INTERNAL)

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

B10AD

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PART OF FS 10

I/O CHANNELS

SYMBOL NO. 1

IOS00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS00	10-03	FA1038	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
		211			CTLST251	6G8
		215			TRANRECO	6G8
ADVST000	I	305	10/2	202	ADVSTA0	5A2
CS8000	OT	111	10/5,10/9	202	MCSRA0	2H1
	I		6/5 TO CONN CKT			
CS8010	OT	307	10/5	202	MCSRC0	2H0
	I		6/5 TO CONN CKT			
CST00231	0	314	10/2		CTLST231	6G4
CST00261	0	011	10/2		CTLST261	6G7
CST00311	0	315	10/2		CTLST311	6G7
CST00341	0	115	10/2		CTLST341	6G6
ESC00000	0	203	10/3		ESC00.0	7G9
ESC00010	0	007	10/3		ESC01.0	7G9
ESC00020	0	207	10/3		ESC02.0	7G9
ESC00030	0	008	10/3		ESC03.0	7G8
ESC00040	0	003	10/3		ESC04.0	7G8
ESC00050	0	202	10/3		ESC05.0	7G8
ESC00060	0	002	10/3		ESC06.0	7G7
ESC00070	0	206	10/3		ESC07.0	7G7
ESC00080	0	103	10/3		ESC08.0	7G7
ESC00090	0	004	10/3		ESC09.0	7G6
ESC00100	0	105	10/4		ESC10.0	7G6
ESC00110	0	304	10/4		ESC11.0	7G6
ESC00120	0	104	10/4		ESC12.0	7G5
ESC00130	0	106	10/4		ESC13.0	7G5
ESC00140	0	010	10/4		ESC14.0	7G5
ESC00150	0	306	10/4		ESC15.0	7G4
ESC00160	0	006	10/4		ESC16.0	7G4
ESC00170	0	210	10/4		ESC17.0	7G4
ESC00180	0	204	10/4		ESC18.0	7G3
ESC00190	0	303	10/4		ESC19.0	7G3
IOLE000	0	110	10/2,10/3 10/4	202	XIOLE0A	2H4
IOL00A0	0	310	10/2		IOLEA0	2H5
IODSIOL0	OT	014	10/5,10/9	202	IOLFLG0	6G1
	I		1/4,1/5 TO CONN CKT			
IOD000	OT	301	10/2,10/5 10/6,10/9 10/10	202	IOS.000	5H6
	I		3/9 TO CONN CKT			
IOD010	OT	101	10/2,10/5 10/6,10/9 10/10	202	IOS.010	5H4
	I		3/8 TO CONN CKT			
IOD020	OT	201	10/2,10/5 10/6,10/9 10/10	202	IOS.020	5H2
	I		3/7 TO CONN CKT			
IOD030	OT	001	10/2,10/5 10/6,10/9 10/10	202	IOS.030	4H4
	I		3/6 TO CONN CKT			
IOD040	OT	300	10/2,10/5 10/6,10/9 10/10	202	IOS.040	4H2
	I		3/5 TO CONN CKT			
IOD050	OT	100	10/2,10/5 10/6,10/9 10/10	202	IOS.050	4H1
	I		3/4 TO CONN CKT			

SYMBOL NO. 1 (CONT)

IOS00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS00	10-03	FA1038	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
IOD060	OT	218	10/2,10/5 10/6,10/9 10/10	202	IOS.060	3G6
	I		3/3 TO CONN CKT			
IOD070	OT	018	10/2,10/5 10/6,10/9 10/10	202	IOS.070	3G6
	I		3/2 TO CONN CKT			
IOD080	OT	219	10/2,10/5 10/6,10/9 10/10	202	IOS.080	3G4
	I		3/9 TO CONN CKT			
IOD090	OT	019	10/2,10/5 10/6,10/9 10/10	202	IOS.090	3G4
	I		3/8 TO CONN CKT			
IOD100	OT	318	10/2,10/5 10/6,10/9 10/10	202	IOS.100	3G3
	I		3/7 TO CONN CKT			
IOD110	OT	118	10/2,10/5 10/6,10/9 10/10	202	IOS.110	3G2
	I		3/6 TO CONN CKT			
MCS000	I	309	10/2		MCS0	2A1
MD0IOCH0	I	213	1/9		IOLXPT0	2A4
MD1CHTN0	I	312	1/9		TNXPT0	2A3
MD2CHTM0	I	013	1/9		TMXPT0	2A3
MD3CHC0	I	112	1/9		R9XIOS0	2A2
MD5EIOS0	I	012	1/9		IOSXIO80	2A6
MSGCM000	0	114	10/2		MSGCMP0	6G3
REC000	0	015	10/2		REC0	6G5
R9.000	I	113	3/9	202	R9.8000	5A8
R9.010	I	313	3/8	202	R9.8010	5A5
R9.020	I	016	3/7	202	R9.8020	5A3
R9.030	I	216	3/6	202	R9.8030	4A6
R9.040	I	116	3/5	202	R9.8040	3A6
R9.050	I	316	3/4	202	R9.8050	3A6
R9.060	I	017	3/3	202	R9.8060	3A4
R9.070	I	217	3/2	202	R9.8070	3A4
R9.080	I	117	3/9	202	R9.8080	3A3
R9.090	I	317	3/8	202	R9.8090	3A2
SCSC0000	I	208	10/4		SCSCC00	8A2
SCSC0010	I	108	10/4		SCSCC10	8A2
SCSC0020	I	308	10/4		SCSCC20	8A1
SCSC0030	I	009	10/4		SCSCC30	8A1
SCSC0040	I	209	10/4		SCSCC40	8A0
SCSC0050	I	109	10/4		SCSCC50	8A0
SG0001	I	212	10/2		SG01	2A5
TMNIR001	0	311	10/2		TMTNIR1A	2H6
T36ER000	0	214	10/2		T3.6ERR0	8H7
3T062C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1003B	GRD	005			GRD005	2B9
	GRD	102			GRD102	2B9
	GRD	107			GRD107	2B9

SYMBOL NO. 1 (CONT)

IOS00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS00	10-03	FA1038	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
3VG1003B	GRD	200			GRD	
	GRD	205			GRD205	2B9
	GRD	302			GRD302	2C9
3V062C	PWR	000		203	+3	
	~~PWR~~	~~119~~		203	+3	

SYMBOL NO. 2

IOD00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD00	10-04	FA1039	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
ADVST000	0	001	10/1	202	ADVSTA0	11H4
CS8020	OT	202	10/9	202	MCSR80	5H0
	I		6/5 TO CONN CKT			
CST00231	I	207	10/1		CTLST231	2A6
CST00261	I	108	10/1		CTLST261	2A8
CST00311	I	208	10/1		CTLST311	2A4
CST00341	I	008	10/1		CTLST341	2A5
ER.IOH0	OT	301	2/9		ERROR0	2G2
GO.000A	0	201	10/3		GO.DLY0A	3H6
GO.000B	0	302	10/4		GO.DLY0B	3H4
IOLE000	I	112	10/1	202	XIOLE0A	3A6
IOL00A0	I	113	10/1		IOLEA0	10A1
INTRPIO0	OT	107	10/6,10/10		INTRPT0	11H7
IO.P11	I	106	8/3		P11	3A4
IO.P21	I	304	8/5		P21	4A6
IO.P31	I	103	8/5		P31	3A4
IODPH0	OT	013	10/6,10/10	202	IODPHG10	5H4
	I		3/1 TO CONN CKT			
IODPL0	OT	009	10/6,10/10	202	IODPLG10	7G7
	I		3/1 TO CONN CKT			
IOD000	OT	219	10/1	202	IOD00G10	9G7
IOD010	OT	019	10/1	202	IOD01G10	9G5
IOD020	OT	318	10/1	202	IOD02G10	9G3
IOD030	OT	118	10/1	202	IOD03G10	9G1
IOD040	OT	218	10/1	202	IOD04G10	8G7
IOD050	OT	018	10/1	202	IOD05G10	8G5
IOD060	OT	317	10/1	202	IOD06G10	8G3
IOD070	OT	117	10/1	202	IOD07G10	8G1
IOD080	OT	310	10/1	202	IOD08G10	7G5
IOD090	OT	110	10/1	202	IOD09G10	7G3
IOD100	OT	210	10/1	202	IOD10G10	7G1
IOD110	OT	010	10/1	202	IOD11G10	6G6
IOD120	OT	309	10/6,10/10	202	IOD12G10	6G5
	I		3/5 TO CONN CKT			
IOD130	OT	109	10/6,10/10	202	IOD13G10	6G3
	I		3/4 TO CONN CKT			
IOD140	OT	209	10/6,10/10	202	IOD14G10	6G1
	I		3/3 TO CONN CKT			
IOD150	OT	213	10/6,10/10	202	IOD15G10	5H6

SYMBOL NO. 2 (CONT)

IOD00

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD00	10-04	FA1039	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
	I		3/2 TO CONN CKT			
IOTR1N0	OT	002	10/6,10/10		NORMSG0	11H5
	I		1/4,1/5 TO CONN CKT			
IOTR2M0	OT	003	10/6,10/10	202	MTCMSG0	11H6
	I		1/4,1/5 TO CONN CKT			
LOFF0A	I	102	7/20		IOCINH0	3A3
MCS000	0	306	10/1		MCS0	5H3
MD4STCH0	I	312	1/9		GOXPT0	3A5
MD6RAIO0	I	311	1/9		R10XIOD0	5A3
MSGCM000	I	308	10/1		MSGCMP0	2A8
RDATA000	I	004	10/4		RDATA0	5A5
REC000	I	007	10/1		REC0	2A7
R10.PH0	I	111	3/1	202	R10.BPH0	5A6
R10.PL0	I	116	3/1	202	R10.BPL0	7A8
R10.000	I	114	3/9	202	R10.B000	9A8
R10.010	I	214	3/8	202	R10.8010	9A6
R10.020	I	014	3/7	202	R10.8020	9A4
R10.030	I	313	3/6	202	R10.8030	9A2
R10.040	I	115	3/5	202	R10.8040	8A8
R10.050	I	215	3/4	202	R10.8050	8A6
R10.060	I	015	3/3	202	R10.8060	8A4
R10.070	I	314	3/2	202	R10.8070	8A2
R10.080	I	216	3/9	202	R10.8080	7A6
R10.090	I	016	3/8	202	R10.8090	7A4
R10.100	I	315	3/7	202	R10.8100	7A2
R10.110	I	011	3/6	202	R10.8110	6A8
R10.120	I	217	3/5	202	R10.8120	6A6
R10.130	I	017	3/4	202	R10.8130	6A4
R10.140	I	316	3/3	202	R10.8140	6A2
R10.150	I	211	3/2	202	R10.8150	5A8
R9.100	I	204	3/7	202	MCSA0	2A4
R9.110	I	104	3/6	202	MCSB0	2A3
R9.120	I	105	3/5	202	MCSC0	2A3
SDATA000	0	100	10/3,10/4		SDATA0	10G8
SG0001	0	300	10/1		SG01	3H6
SHIFT000	I	303	10/4		SHFT0	4A4
TMNIR001	I	203	10/1		TMTNIR1A	2A1
T36ER000	I	206	10/1		T3.6ERR0	2A2
3T062C	GRD	0G0		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1004B	GRD	005			GRD005	2G0
	GRD	107			GRD107	2G1
	GRD	200			GRD	
	GRD	205			GRD205	2G1
	GRD	307			GRD307	2G1

PART OF FS 10

SYMBOL(S) 1 2

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B10CA

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PART OF FS 10

I/O CHANNELS

SYMBOL NO. 2 (CONT)

IODOO

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IODOO	10-04	FA1039	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG1004T	GRD	012			GRD012	2G0
3VG1004T	GRD	212			GRD212	2G1
	GRD	319			GRD	
3V062C	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 3

I/O SUBCHANNELS 00-09

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IO00SCA	10-05	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ESC00000	I	207	10/1		ESCD0	2B3
ESC00010	I	209	10/1		ESCJ0	2E3
ESC00020	I	310	10/1		ESCI0	2F3
ESC00030	I	211	10/1		ESCH0	2F3
ESC00040	I	306	10/1		ESCC0	2C3
ESC00050	I	208	10/1		ESCB0	2D3
ESC00060	I	308	10/1		ESCA0	2D3
ESC00070	I	105	10/1		ESCG0	2G3
ESC00080	I	005	10/1		ESCF0	2H3
ESC00090	I	008	10/1		ESCE0	2B3
GO.000A	I	006	10/2		GO.OLY0	2B3
IOLE000	I	203	10/1	202	INIT0	3A2
IO.P21	I	106	8/5		P21	2C3
IO.P31	I	307	8/5		P31	2C3
RDATA000	OT	303	10/4		RDATA0	3C6
SCSC0000	OT	311	10/4		HIJ0	2F7
SCSC0010	OT	007	10/4		EFG0	2A7
SCSC0020	OT	206	10/4		BCD0	2C7
SCSC0030	OT	205	10/4		ABCEFHI0	2D7
SCSC0040	OT	305	10/4		ABDEGHJ0	2D7
SCSC0050	OT	304	10/4		ACDFGIJ0	2D7
SC00R00P	I	104	TO CONN CKT		RSCDP	3C2
SC00R01P	I	103	TO CONN CKT		RSCJP	3F2
SC00R02P	I	312	TO CONN CKT		RSCIP	3E2
SC00R03P	I	102	TO CONN CKT		RSCHP	3E2
SC00R04P	I	110	TO CONN CKT		RSCCP	3B2
SC00R05P	I	109	TO CONN CKT		RSCBP	3B2
SC00R06P	I	313	TO CONN CKT		RSCAP	3A2
SC00R07P	I	101	TO CONN CKT		RSCGP	3D2
SC00R08P	I	316	TO CONN CKT		RSCFP	3D2
SC00R09P	I	201	TO CONN CKT		RSCEP	3D2
SC00S00P	O	117	TO CONN CKT		SSCDP	2B7
SC00S01P	O	114	TO CONN CKT		SSCJP	2E7
SC00S02P	O	113	TO CONN CKT		SSCIP	2F7
SC00S03P	O	112	TO CONN CKT		SSCHP	2G7
SC00S04P	O	116	TO CONN CKT		SSCCP	2C7
SC00S05P	O	115	TO CONN CKT		SSCBP	2C7
SC00S06P	O	318	TO CONN CKT		SSCAP	2D7
SC00S07P	O	111	TO CONN CKT		SSCGP	2G7

SYMBOL NO. 3 (CONT)

I/O SUBCHANNELS 00-09

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IO00SCA	10-05	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SC00S08P	O	317	TO CONN CKT		SSCFP	2H7
SC00S09P	O	118	TO CONN CKT		SSCEP	2B7
SDATA000	I	108	10/2		SDATA0	2C3
SHIFT000	OT	204	10/4		SHFT0	3B6
3T062C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1005B	I	001			RSCGN	3E2
	I	002			RSCHN	3E2
	I	003			RSCJN	3F2
	I	004			RSCDN	3C2
	I	009			RSCBN	3B2
	I	301			RSCEN	3D2
	GRD	200			GRD	
3VG1005T	OT	011			SSCGN	2G7
	OT	012			SSCHN	2F7
	OT	013			SSCIN	2F7
	OT	014			SSCJN	2E7
	OT	015			SSCBN	2C7
	OT	016			SSCCN	2B7
	OT	017			SSCDN	2B7
	OT	018			SSCEN	2A7
	OT	217			SSCFN	2H7
	OT	218			SSCAN	2D7
	I	010			RSCCN	3C2
	I	212			RSCIN	3F2
	I	213			RSCAN	3B2
	I	216			RSCFN	3D2
	GRD	319			GRD	
3V062C	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 4

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IO00SCB	10-06	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ESC00100	I	209	10/1		ESCJ0	2E3
ESC00110	I	310	10/1		ESCI0	2F3
ESC00120	I	211	10/1		ESCH0	2F3
ESC00130	I	005	10/1		ESCF0	2H3
ESC00140	I	008	10/1		ESCE0	2B3
ESC00150	I	208	10/1		ESCB0	2D3
ESC00160	I	306	10/1		ESCC0	2C3
ESC00170	I	207	10/1		ESCD0	2B3
ESC00180	I	308	10/1		ESCA0	2D3
ESC0019G	I	105	10/1		ESCG0	2G3
GO.000B	I	006	10/2		GO.OLY0	2B3
IOLE000	I	203	10/1	202	INIT0	3A2

SYMBOL NO. 4 (CONT)

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IO00SCB	10-06	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IO.P21	I	106	8/5		P21	2C3
IO.P31	I	307	8/5		P31	2C3
RDATA000	OT	303	10/3		RDATA0	3C6
	I		10/2			
SCSC0000	OT	304	10/3		ACDFGIJ0	2D7
	I		10/1			
SCSC0010	OT	305	10/3		ABDEGHJ0	2D7
	I		10/1			
SCSC0020	OT	205	10/3		ABCEFHI0	2D7
	I		10/1			
SCSC0030	OT	206	10/3		BCD0	2C7
	I		10/1			
SCSC0040	OT	007	10/3		EFG0	2A7
	I		10/1			
SCSC0050	OT	311	10/3		HIJ0	2F7
	I		10/1			
SC00R10P	I	103	TO CONN CKT		RSCJP	3F2
SC00R11P	I	312	TO CONN CKT		RSCIP	3E2
SC00R12P	I	102	TO CONN CKT		RSCHP	3E2
SC00R13P	I	316	TO CONN CKT		RSCFP	3D2
SC00R14P	I	201	TO CONN CKT		RSCEP	3D2
SC00R15P	I	109	TO CONN CKT		RSCBP	3B2
SC00R16P	I	110	TO CONN CKT		RSCCP	3B2
SC00R17P	I	104	TO CONN CKT		RSCDP	3C2
SC00R18P	I	313	TO CONN CKT		RSCAP	3A2
SC00R19P	I	101	TO CONN CKT		RSCGP	3D2
SC00S10P	O	114	TO CONN CKT		SSCJP	2E7
SC00S11P	O	113	TO CONN CKT		SSCIP	2F7
SC00S12P	O	112	TO CONN CKT		SSCHP	2G7
SC00S13P	O	317	TO CONN CKT		SSCFP	2H7
SC00S14P	O	118	TO CONN CKT		SSCEP	2B7
SC00S15P	O	115	TO CONN CKT		SSCBP	2C7
SC00S16P	O	116	TO CONN CKT		SSCCP	2C7
SC00S17P	O	117	TO CONN CKT		SSCDP	2B7
SC00S18P	O	318	TO CONN CKT		SSCAP	2D7
SC00S19P	O	111	TO CONN CKT		SSCGP	2G7
SDATA000	I	108	10/2		SDATA0	2C3
SHIFT000	OT	204	10/3		SHFT0	3B6
	I		10/2			
3T062C	GRD	0G0		203	GRD	
	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1006B	I	001			RSCGN	3E2
	I	002			RSCHN	3E2
	I	003			RSCJN	3F2
	I	004			RSCDN	3C2
	I	009			RSCBN	3B2
	I	301			RSCEN	3D2
	GRD	200			GRD	
3VG1006T	OT	011			SSCGN	2G7
	OT	012			SSCHN	2F7
	OT	013			SSCIN	2F7
	OT	014			SSCJN	2E7
	OT	015			SSCBN	2C7
	OT	016			SSCCN	2B7
	OT	017			SSCDN	2B7
	OT	018			SSCEN	2A7
	OT	217			SSCFN	2H7
	OT	218			SSCAN	2D7
	I	010			RSCCN	3C2
	I	212			RSCIN	3F2

SYMBOL NO. 4 (CONT)

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IO00SCB	10-06	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG1006T	I	213			RSCAN	3B2
	I	216			RSCFN	3D2
	GRD	319			GRD	
3V062C	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 10
SYMBOL(S) 2 3 4

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	5A

BELL LABORATORIES | SD-1C900-01 | B10CB

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06/10/77

PART OF FS 10

I/O CHANNELS

SYMBOL NO. 5

IOS01

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS01	10-07	FA1038	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		211			CTLST251	6G8
		215			TRANRECO	6G8
ADVST010	I	305	10/6		ADVSTA0	5A2
CSB000	OT	111	10/1	202	MCSRA0	2H1
CSB010	OT	307	10/1	202	MCSRC0	2H0
CST01231	0	314	10/6		CTLST231	6G4
CST01261	0	011	10/6		CTLST261	6G7
CST01311	0	315	10/6		CTLST311	6G7
CST01341	0	115	10/6		CTLST341	6G6
ESC01000	0	203	10/7		ESC00.0	7G9
ESC01010	0	007	10/7		ESC01.0	7G9
ESC01020	0	207	10/7		ESC02.0	7G9
ESC01030	0	008	10/7		ESC03.0	7G8
ESC01040	0	003	10/7		ESC04.0	7G8
ESC01050	0	202	10/7		ESC05.0	7G8
ESC01060	0	002	10/7		ESC06.0	7G7
ESC01070	0	206	10/7		ESC07.0	7G7
ESC01080	0	103	10/7		ESC08.0	7G7
ESC01090	0	004	10/7		ESC09.0	7G6
ESC01100	0	105	10/8		ESC10.0	7G6
ESC01110	0	304	10/8		ESC11.0	7G6
ESC01120	0	104	10/8		ESC12.0	7G5
ESC01130	0	106	10/8		ESC13.0	7G5
ESC01140	0	010	10/8		ESC14.0	7G5
ESC01150	0	306	10/8		ESC15.0	7G4
ESC01160	0	006	10/8		ESC16.0	7G4
ESC01170	0	210	10/8		ESC17.0	7G4
ESC01180	0	204	10/8		ESC18.0	7G3
ESC01190	0	303	10/8		ESC19.0	7G3
IOLE010	0	110	10/6,10/7 10/8		XIDLEOA	2H4
IOL01A0	0	310	10/6		IOLEA0	2H5
IODSIOL0	OT	014	10/1	202	IOLFLG0	6G1
IOD000	OT	301	10/1	202	IOS.000	5H6
IOD010	OT	101	10/1	202	IOS.010	5H4
IOD020	OT	201	10/1	202	IOS.020	5H2
IOD030	OT	001	10/1	202	IOS.030	4H4
IOD040	OT	300	10/1	202	IOS.040	4H2
IOD050	OT	100	10/1	202	IOS.050	4H1
IOD060	OT	218	10/1	202	IOS.060	3G6
IOD070	OT	018	10/1	202	IOS.070	3G6
IOD080	OT	219	10/1	202	IOS.080	3G4
IOD090	OT	019	10/1	202	IOS.090	3G4
IOD100	OT	318	10/1	202	IOS.100	3G3
IOD110	OT	118	10/1	202	IOS.110	3G2
MCS010	I	309	10/6		MCS0	2A1
MD0IOCH0	I	213	1/9		IOLXPT0	2A4
MD1CHTN0	I	312	1/9		TNXPT0	2A3
MD2CHTM0	I	013	1/9		TMXPT0	2A3
MD3CHC0	I	112	1/9		R9XIOS0	2A2
MD5EIOS0	I	012	1/9		IOSX10B0	2A6
MSGCM010	0	114	10/6		MSGCMP0	6G3
REC010	0	015	10/6		REC0	6G3
R9.000	I	113	3/9	202	R9.B000	5A8
R9.010	I	313	3/8	202	R9.B010	5A5
R9.020	I	016	3/7	202	R9.B020	5A3
R9.030	I	216	3/6	202	R9.B030	4A6
R9.040	I	116	3/5	202	R9.B040	3A6

SYMBOL NO. 5 (CONT)

IOS01

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS01	10-07	FA1038	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R9.050	I	316	3/4	202	R9.B050	3A6
R9.060	I	017	3/3	202	R9.B060	3A4
R9.070	I	217	3/2	202	R9.B070	3A4
R9.080	I	112	3/9	202	R9.B080	3A3
R9.090	I	317	3/8	202	R9.B090	3A2
SCSC0100	I	208	10/8		SCSCC00	8A2
SCSC0110	I	108	10/8		SCSCC10	8A2
SCSC0120	I	308	10/8		SCSCC20	8A1
SCSC0130	I	009	10/8		SCSCC30	8A1
SCSC0140	I	209	10/8		SCSCC40	8A0
SCSC0150	I	109	10/8		SCSCC50	8A0
SG0011	I	212	10/6		SG01	2A5
TMNIR011	0	311	10/6		TMTNIR1A	2H6
T36ER010	0	214	10/6		T3.6ERR0	8H7
3T058D	GRD	0G0		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1007B	GRD	005			GRD005	2B9
	GRD	102			GRD102	2B9
	GRD	107			GRD107	2B9
	GRD	200			GRD	
	GRD	205			GRD205	2B9
	GRD	302			GRD302	2C9
3V058D	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 6

IOD01

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD01	10-08	FA1039	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADVST010	0	001	10/5		ADVSTA0	11H4
CSB030	OT	202	10/10	202	MCSRB0	5H0
	I		6/5 TO CONN CKT			
CST01231	I	207	10/5		CTLST231	2A6
CST01261	I	108	10/5		CTLST261	2A8
CST01311	I	208	10/5		CTLST311	2A4
CST01341	I	008	10/5		CTLST341	2A5
ER.IOH0	OT	301	2/9		ERROR0	2G2
GO.010A	0	201	10/7		GO.OLY0A	3H4
GO.010B	0	302	10/8		GO.OLY0B	3H4
IOLE010	I	112	10/5		XIOLE0A	3A6
IOL01A0	I	113	10/5		IDLEA0	10A1
INTRPID0	OT	101	10/2		INTRPT0	11H7
IO.P11	I	106	8/3		P11	3A4
IO.P21	I	304	8/5		P21	4A6
IO.P31	I	103	8/5		P31	3A4
IODPH0	OT	013	10/2	202	IODPHG10	5H4
IODPL0	OT	009	10/2	202	IODPLG10	7G7
IOD000	OT	219	10/1	202	IOD00G10	9G7

SYMBOL NO. 6 (CONT)

IOD01

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD01	10-08	FA1039	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IOD010	OT	019	10/1	202	IOD01G10	9G5
IOD020	OT	318	10/1	202	IOD02G10	9G3
IOD030	OT	118	10/1	202	IOD03G10	9G1
IOD040	OT	218	10/1	202	IOD04G10	8G7
IOD050	OT	018	10/1	202	IOD05G10	8G5
IOD060	OT	317	10/1	202	IOD06G10	8G3
IOD070	OT	117	10/1	202	IOD07G10	8G1
IOD080	OT	310	10/1	202	IOD08G10	7G5
IOD090	OT	110	10/1	202	IOD09G10	7G3
IOD100	OT	210	10/1	202	IOD10G10	7G1
IOD110	OT	010	10/1	202	IOD11G10	6G6
IOD120	OT	309	10/2	202	IOD12G10	6G5
IOD130	OT	109	10/2	202	IOD13G10	6G3
IOD140	OT	209	10/2	202	IOD14G10	6G1
IOD150	OT	213	10/2	202	IOD15G10	5H6
IOTR1N0	OT	002	10/2		NORMSG0	11H5
IOTR2M0	OT	003	10/2	202	MTCMSG0	11H6
LOFF0A	I	102	7/20		IOCINH0	3A3
MCS010	0	306	10/5		MCS0	5H3
MD4STCH0	I	312	1/9		GOXPT0	3A5
MD6RAI00	I	311	1/9		R10XIDD0	5A3
MSGCM010	I	308	10/5		MSGCMP0	2A8
RDATA010	I	004	10/8		RDATA0	5A5
REC010	I	007	10/5		REC0	2A7
R10.PH0	I	111	3/1	202	R10.BPH0	5A6
R10.PL0	I	116	3/1	202	R10.BPL0	7A8
R10.000	I	114	3/9	202	R10.B000	9A8
R10.010	I	214	3/8	202	R10.B010	9A6
R10.020	I	014	3/7	202	R10.B020	9A4
R10.030	I	313	3/6	202	R10.B030	9A2
R10.040	I	115	3/5	202	R10.B040	8A8
R10.050	I	215	3/4	202	R10.B050	8A6
R10.060	I	015	3/3	202	R10.B060	8A4
R10.070	I	314	3/2	202	R10.B070	8A2
R10.080	I	216	3/9	202	R10.B080	7A6
R10.090	I	016	3/8	202	R10.B090	7A4
R10.100	I	315	3/7	202	R10.B100	7A2
R10.110	I	011	3/6	202	R10.B110	6A8
R10.120	I	217	3/5	202	R10.B120	6A6
R10.130	I	017	3/4	202	R10.B130	6A4
R10.140	I	316	3/3	202	R10.B140	6A2
R10.150	I	211	3/2	202	R10.B150	5A8
R9.100	I	204	3/7	202	MCSA0	2A4
R9.110	I	104	3/6	202	MCSB0	2A3
R9.130	I	105	3/4	202	MCSC0	2A3
SDATA010	0	100	10/7,10/8		SDATA0	10G8
SG0011	0	300	10/5		SG01	3H6
SHIFT010	I	303	10/8		SHFT0	4A4
TMNIR011	I	203	10/5		TMTNIR1A	2A1
T36ER010	I	206	10/5		T3.6ERR0	2A2
3T0580	GRD	0GD		203	GRD	
	GRD	2G0		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1008B	GRD	005			GRD005	2G0
	GRD	107			GRD107	2G1
	GRD	200			GRD	
	GRD	205			GRD205	2G1
	GRD	307			GRD307	2G1
3VG1008T	GRD	012			GRD012	2G0

SYMBOL NO. 6 (CONT)

IOD01

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD01	10-08	FA1039	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG1008T	GRD	212			GRD212	2G1
	GRD	319			GRD	
3V0580	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 10
SYMBOL(S) 5 6

3A CENTRAL CONTROL

DWG SIZE C2
ISSUE 5A

BELL LABORATORIES
SD-1C900-01
B10CC

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06/10/77

PART OF FS 10

I/O CHANNELS

SYMBOL NO. 7

I/O SUBCHANNELS 00-09

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
I001SCA	10-09	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
ESC01000	I	207	10/5		ESCD0	2B3
ESC01010	I	209	10/5		ESCJ0	2E3
ESC01020	I	310	10/5		ESCI0	2F3
ESC01030	I	211	10/5		ESCH0	2F3
ESC01040	I	306	10/5		ESCC0	2C3
ESC01050	I	208	10/5		ESCB0	2D3
ESC01060	I	308	10/5		ESCA0	2D3
ESC01070	I	105	10/5		ESCG0	2G3
ESC01080	I	005	10/5		ESCF0	2H3
ESC01090	I	008	10/5		ESCE0	2B3
GO.010A	I	006	10/6		GO.DLY0	2B3
IDLE010	I	203	10/5		INIT0	3A2
IO.P21	I	106	8/5		P21	2C3
IO.P31	I	307	8/5		P31	2C3
RDATA010	OT	303	10/8		RDATA0	3C6
SCSC0100	OT	311	10/8		HIJ0	2F7
SCSC0110	OT	007	10/8		EFG0	2A7
SCSC0120	OT	206	10/8		BCD0	2C7
SCSC0130	OT	205	10/8		ABCEFHI0	2D7
SCSC0140	OT	305	10/8		ABDEGHJ0	2D7
SCSC0150	OT	304	10/8		ACDFGIJ0	2D7
SC01R00P	I	104	TO CONN CKT		RSCDP	3C2
SC01R01P	I	103	TO CONN CKT		RSCJP	3F2
SC01R02P	I	312	TO CONN CKT		RSCIP	3E2
SC01R03P	I	102	TO CONN CKT		RSCHP	3E2
SC01R04P	I	110	TO CONN CKT		RSCCP	3B2
SC01R05P	I	109	TO CONN CKT		RSCBP	3B2
SC01R06P	I	313	TO CONN CKT		RSCAP	3A2
SC01R07P	I	101	TO CONN CKT		RSCGP	3D2
SC01R08P	I	316	TO CONN CKT		RSCFP	3D2
SC01R09P	I	201	TO CONN CKT		RSCEP	3D2
SC01S00P	O	117	TO CONN CKT		SSCDP	2B7
SC01S01P	O	114	TO CONN CKT		SSCJP	2E7
SC01S02P	O	113	TO CONN CKT		SSCIP	2F7
SC01S03P	O	112	TO CONN CKT		SSCHP	2G7
SC01S04P	O	116	TO CONN CKT		SSCCP	2C7
SC01S05P	O	115	TO CONN CKT		SSCBP	2C7
SC01S06P	O	318	TO CONN CKT		SSCAP	2D7
SC01S07P	O	111	TO CONN CKT		SSCGP	2G7
SC01S08P	O	317	TO CONN CKT		SSCFP	2H7
SC01S09P	O	118	TO CONN CKT		SSCEP	2B7
SDATA010	I	108	10/6		SDATA0	2C3
SHIFT010	OT	204	10/8		SHFT0	3B6
3T058D	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1009B	I	001			RSCGN	3E2
	I	002			RSCHN	3E2
	I	003			RSCJN	3F2
	I	004			RSCDN	3C2
	I	009			RSCBN	3B2
	I	301			RSCEN	3D2
	GRD	200			GRD	
3VG1009T	OT	011			SSCGN	2G7
	OT	012			SSCHN	2F7
	OT	013			SSCIN	2F7
	OT	014			SSCJN	2E7
	OT	015			SSCBN	2C7
	OT	016			SSCCN	2B7

SYMBOL NO. 7 (CONT)

I/O SUBCHANNELS 00-09

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
I001SCA	10-09	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
3VG1009T	OT	017			SSCDN	2B7
	OT	018			SSCEN	2A7
	OT	217			SSCFN	2H7
	OT	218			SSCAN	2D7
	~~I~~	~~010~~			~~RSCCN~~	~~3E2~~
	I	212			RSCIN	3F2
	I	213			RSCAN	3B2
	I	216			RSCFN	3D2
	GRD	319			GRD	
3V0580	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 8

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
I001SCB	10-10	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
ESC01100	I	209	10/5		ESCJ0	2E3
ESC01110	I	310	10/5		ESCI0	2F3
ESC01120	I	211	10/5		ESCH0	2F3
ESC01130	I	005	10/5		ESCF0	2H3
ESC01140	I	008	10/5		ESCE0	2B3
ESC01150	I	208	10/5		ESCB0	2D3
ESC01160	I	306	10/5		ESCC0	2C3
ESC01170	I	207	10/5		ESCD0	2B3
ESC01180	I	308	10/5		ESCA0	2D3
ESC01190	I	105	10/5		ESCG0	2G3
GO.010B	I	006	10/6		GO.DLY0	2B3
IDLE010	I	203	10/5		INIT0	3A2
IO.P21	I	106	8/5		P21	2C3
IO.P31	I	307	8/5		P31	2C3
RDATA010	OT	303	10/7		RDATA0	3C6
	I		10/6			
SCSC0100	OT	304	10/7		ACDFGIJ0	2D7
	I		10/5			
SCSC0110	OT	305	10/7		ABDEGHJ0	2D7
	I		10/5			
SCSC0120	OT	205	10/7		ABCEFHI0	2D7
	I		10/5			
SCSC0130	OT	206	10/7		BCD0	2C7
	I		10/5			
SCSC0140	OT	007	10/7		EFG0	2A7
	I		10/5			
SCSC0150	OT	311	10/7		HIJ0	2F7
	I		10/5			
SC01R10P	I	103	TO CONN CKT		RSCJP	3F2
SC01R11P	I	312	TO CONN CKT		RSCIP	3E2
SC01R12P	I	102	TO CONN CKT		RSCHP	3E2
SC01R13P	I	316	TO CONN CKT		RSCFP	3D2
SC01R14P	I	201	TO CONN CKT		RSCEP	3D2
SC01R15P	I	109	TO CONN CKT		RSCBP	3B2

SYMBOL NO. 8 (CONT)

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
I001SCB	10-10	FC201	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
FS INFO					CP INFO	
SC01R16P	I	110	TO CONN CKT		RSCCP	3B2
SC01R17P	I	104	TO CONN CKT		RSCDP	3C2
SC01R18P	I	313	TO CONN CKT		RSCAP	3A2
SC01R19P	I	101	TO CONN CKT		RSCGP	3D2
~~SC01S10P~~	~~O~~	~~114~~	~~TO CONN CKT~~		~~SSCJP~~	2E7
SC01S11P	O	113	TO CONN CKT		SSCIP	2F7
SC01S12P	O	112	TO CONN CKT		SSCHP	2G7
SC01S13P	O	317	TO CONN CKT		SSCFP	2H7
SC01S14P	O	118	TO CONN CKT		SSCEP	2B7
SC01S15P	O	115	TO CONN CKT		SSCBP	2C7
SC01S16P	O	116	TO CONN CKT		SSCCP	2C7
SC01S17P	O	117	TO CONN CKT		SSCDP	2B7
SC01S18P	O	318	TO CONN CKT		SSCAP	2D7
SC01S19P	O	111	TO CONN CKT		SSCGP	2G7
SDATA010	I	108	10/6		SDATA0	2C3
SHIFT010	OT	204	10/7		SHFT0	3B6
	I		10/6			
3T0580	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1010B	I	001			RSCGN	3E2
	I	002			RSCHN	3E2
	I	003			RSCJN	3F2
	I	004			RSCDN	3C2
	I	009			RSCBN	3B2
	I	301			RSCEN	3D2
	GRD	200			GRD	
3VG1010T	OT	011			SSCGN	2G7
	OT	012			SSCHN	2F7
	OT	013			SSCIN	2F7
	OT	014			SSCJN	2E7
	OT	015			SSCBN	2C7
	OT	016			SSCCN	2B7
	OT	017			SSCDN	2B7
	OT	018			SSCEN	2A7
	OT	217			SSCFN	2H7
	OT	218			SSCAN	2D7
	I	010			RSCCN	3C2
	I	212			RSCIN	3F2
	I	213			RSCAN	3B2
	I	216			RSCFN	3D2
	GRD	319			GRD	
3V0580	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 10
SYMBOL(S) 7 8

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B10CD

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06/10/77

PART OF FS 10

I/O CHANNELS

SYMBOL NO. 9

IOS02

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS02	10-11	FA1038	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		211			CTLST251	6G8
		215			TRANRECO	6G8
ADVST020	I	305	10/10		ADVSTA0	5A2
CSB000	OT	111	10/1	202	MCSRA0	2H1
CSB020	OT	307	10/2	202	MCSRC0	2H0
CST02231	O	314	10/10		CTLST231	6G4
CST02261	O	011	10/10		CTLST261	6G7
CST02311	O	315	10/10		CTLST311	6G7
CST02341	O	115	10/10		CTLST341	6G6
ESC02000	O	203	10/11		ESC00.0	7G9
ESC02010	O	007	10/11		ESC01.0	7G9
ESC02020	O	207	10/11		ESC02.0	7G9
ESC02030	O	008	10/11		ESC03.0	7G8
ESC02040	O	003	10/11		ESC04 0	7G8
ESC02050	O	202	10/11		ESC05.0	7G8
ESC02060	O	002	10/11		ESC06.0	7G7
ESC02070	O	206	10/11		ESC07.0	7G7
ESC02080	O	103	10/11		ESC08.0	7G7
ESC02090	O	004	10/11		ESC09.0	7G6
ESC02100	O	105	10/12		ESC10.0	7G6
ESC02110	O	304	10/12		ESC11.0	7G6
ESC02120	O	104	10/12		ESC12.0	7G5
ESC02130	O	106	10/12		ESC13.0	7G5
ESC02140	O	010	10/12		ESC14.0	7G5
ESC02150	O	306	10/12		ESC15.0	7G4
ESC02160	O	006	10/12		ESC16.0	7G4
ESC02170	O	210	10/12		ESC17.0	7G4
ESC02180	O	204	10/12		ESC18.0	7G3
ESC02190	O	303	10/12		ESC19.0	7G3
IOLE020	O	110	10/10,10/11 10/12		XIOLE0A	2H4
IOL02A0	O	310	10/10		IOLEA0	2H5
IODSIOL0	OT	014	10/1	202	IOLFLG0	6G1
IOD000	OT	301	10/1	202	IOS.000	5H6
IOD010	OT	101	10/1	202	IOS.010	5H4
IOD020	OT	201	10/1	202	IOS.020	5H2
IOD030	OT	001	10/1	202	IOS.030	4H6
IOD040	OT	300	10/1	202	IOS.040	4H2
IOD050	OT	100	10/1	202	IOS.050	4H1
IOD060	OT	218	10/1	202	IOS.060	3G6
IOD070	OT	018	10/1	202	IOS.070	3G6
IOD080	OT	219	10/1	202	IOS.080	3G4
IOD090	OT	019	10/1	202	IOS.090	3G4
IOD100	OT	318	10/1	202	IOS.100	3G3
IOD110	OT	118	10/1	202	IOS.110	3G2
MCS020	I	309	10/10		MCS0	2A1
M00IOCH0	I	213	1/9		IOLXPT0	2A4
M01CHTN0	I	312	1/9		TNXPT0	2A3
MD2CHTM0	I	013	1/9		TMXPT0	2A3
M03CHC0	I	112	1/9		R9XIOS0	2A2
M05EIOS0	I	012	1/9		IOSXIOB0	2A6
MSGCM020	O	114	10/10		MSGCMP0	6G3
REC020	O	015	10/10		REC0	6G5
R9.000	I	113	3/9	202	R9.B000	5A8
R9.010	I	313	3/8	202	R9.B010	5A5
R9.020	I	016	3/7	202	R9.B020	5A3
R9.030	I	216	3/6	202	R9.B030	4A6
R9.040	I	116	3/5	202	R9.B040	3A6

SYMBOL NO. 9 (CONT)

IOS02

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOS02	10-11	FA1038	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R9.050	I	316	3/4	202	R9.B050	3A6
R9.060	I	017	3/3	202	R9.B060	3A4
R9.070	I	217	3/2	202	R9.B070	3A4
R9.080	I	112	3/9	202	R9.B080	3A3
R9.090	I	317	3/8	202	R9.B090	3A2
SCSC0200	I	208	10/12		SCSCC00	8A2
SCSC0210	I	108	10/12		SCSCC10	8A2
SCSC0220	I	308	10/12		SCSCC20	8A1
SCSC0230	I	009	10/12		SCSCC30	8A1
SCSC0240	I	209	10/12		SCSCC40	8A0
SCSC0250	I	109	10/12		SCSCC50	8A0
SG0021	I	212	10/10		SG01	2A5
TMNIR021	O	311	10/10		TMTNIR1A	2H6
T36ER020	O	214	10/10		T3.6ERR0	8H7
3T0580	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1011B	GRD	005			GRD005	2B9
	GRD	102			GRD102	2B9
	GRD	107			GRD107	2B9
	GRD	200			GRD	
	GRD	205			GRD205	2B9
	GRD	302			GRD302	2C9
3V0580	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 10

IOD02

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD02	10-12	FA1039	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ADVST020	O	001	10/9		ADVSTA0	11H4
CSB030	OT	202	10/6	202	MCSRB0	5H0
CST02231	I	207	10/9		CTLST231	2A6
CST02261	I	108	10/9		CTLST261	2A8
CST02311	I	208	10/9		CTLST311	2A4
CST02341	I	008	10/9		CTLST341	2A5
ER.IOH0	OT	301	2/9		ERROR0	2G2
GO.020A	O	201	10/11		GO.OLY0A	3H4
GO.020B	O	302	10/12		GO.OLY0B	3H4
IOLE020	I	112	10/9		XIOLE0A	3A6
IOL02A0	I	113	10/9		IOLEA0	10A1
INTRPIOC	GT	101	10/2		INTRPT0	11H7
IO.P11	I	106	8/3		P11	3A4
IO.P21	I	304	8/5		P21	4A6
IO.P31	I	103	8/5		P31	3A4
IODPH0	OT	013	10/2	202	IODPHG10	5H4
IODPL0	OT	009	10/2	202	IODPLG10	7G7
IOD000	OT	219	10/1	202	IOD00G10	9G7

SYMBOL NO. 10 (CONT)

IOD02

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD02	10-12	FA1039	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
IOD010	OT	019	10/1	202	IOD01G10	9G5
IOD020	OT	318	10/1	202	IOD02G10	9G3
IOD030	OT	118	10/1	202	IOD03G10	9G1
IOD040	OT	218	10/1	202	IOD04G10	8G7
IOD050	OT	018	10/1	202	IOD05G10	8G5
IOD060	OT	317	10/1	202	IOD06G10	8G3
IOD070	OT	117	10/1	202	IOD07G10	8G1
IOD080	OT	310	10/1	202	IOD08G10	7G5
IOD090	OT	110	10/1	202	IOD09G10	7G3
IOD100	OT	210	10/1	202	IOD10G10	7G1
IOD110	OT	010	10/1	202	IOD11G10	6G6
IOD120	OT	309	10/2	202	IOD12G10	6G5
IOD130	OT	109	10/2	202	IOD13G10	6G3
IOD140	OT	209	10/2	202	IOD14G10	6G1
IOD150	OT	213	10/2	202	IOD15G10	5H6
IOTR1N0	OT	002	10/2		NORMSG0	11H5
IOTR2M0	OT	003	10/2	202	MTCMSG0	11H6
LOFF0A	I	102	7/20		IOCINH0	3A3
MCS020	O	306	10/9		MCS0	5H3
MD4STCH0	I	312	1/9		GOXPT0	3A5
MD6RAI00	I	311	1/9		R10XIOD0	5A3
MSGCM020	I	308	10/9		MSGCMP0	2A8
RDATA020	I	004	10/12		RDATA0	5A5
REC020	I	007	10/9		REC0	2A7
R10.PH0	I	111	3/1	202	R10.BPH0	5A6
R10.PL0	I	116	3/1	202	R10.BPL0	7A8
R10.000	I	114	3/9	202	R10.B000	9A8
R10.010	I	214	3/8	202	R10.B010	9A6
R10.020	I	014	3/7	202	R10.B020	9A4
R10.030	I	313	3/6	202	R10.B030	9A2
R10.040	I	115	3/5	202	R10.B040	8A8
R10.050	I	215	3/4	202	R10.B050	8A6
R10.060	I	015	3/3	202	R10.B060	8A4
R10.070	I	314	3/2	202	R10.B070	8A2
R10.080	I	216	3/9	202	R10.B080	7A6
R10.090	I	016	3/8	202	R10.B090	7A4
R10.100	I	315	3/7	202	R10.B100	7A2
R10.110	I	011	3/6	202	R10.B110	6A8
R10.120	I	217	3/5	202	R10.B120	6A6
R10.130	I	017	3/4	202	R10.B130	6A4
R10.140	I	316	3/3	202	R10.B140	6A2
R10.150	I	211	3/2	202	R10.B150	5A8
R9.100	I	204	3/7	202	MCSA0	2A4
R9.120	I	104	3/5	202	MCSB0	2A3
R9.130	I	105	3/4	202	MCSC0	2A3
SDATA020	O	100	10/11,10/12		SDATA0	10G8
SG0021	O	300	10/9		SG01	3H6
SHIFT020	I	303	10/12		SHFT0	4A4
TMNIR021	I	203	10/9		TMTNIR1A	2A1
T36ER020	I	206	10/9		T3.6ERR0	2A2
3T058E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1012B	GRD	005			GRD005	2G0
	GRD	107			GRD107	2G1
	GRD	200			GRD	
	GRD	205			GRD205	2G1
	GRD	307			GRD307	2G1
3VG1012T	GRD	012			GRD012	2G0

SYMBOL NO. 10 (CONT)

IOD02

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
IOD02	10-12	FA1039	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG1012T	GRD	212			GRD212	2G1
	GRD	319			GRD	
3V058E	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 10
SYMBOL(S) 9 10

3A CENTRAL CONTROL

DWG SIZE C2
ISSUE 5A

BELL LABORATORIES
SD-1C900-01
B10CE

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06/10/77

PART OF FS 10

I/O CHANNELS

SYMBOL NO. 11

I/O SUBCHANNELS 00-09

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
1002SCA	10-13	FC201	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ESC02000	I	207	10/9		ESCD0	2B3
ESC02010	I	209	10/9		ESCJ0	2E3
ESC02020	I	313	10/9		ESCI0	2F3
ESC02030	I	211	10/9		ESCH0	2F3
ESC02040	I	306	10/9		ESCC0	2C3
ESC02050	I	208	10/9		ESCB0	2D3
ESC02060	I	308	10/9		ESCA0	2D3
ESC02070	I	105	10/9		ESCG0	2G3
ESC02080	I	005	10/9		ESCF0	2H3
ESC02090	I	008	10/9		ESCE0	2B3
GO.020A	I	006	10/10		GO.DLY0	2B3
IOLE020	I	203	10/9		INIT0	3A2
IO.P21	I	106	8/5		P21	2C3
IO.P31	I	307	8/5		P31	2C3
RDATA020	OT	303	10/12		RDATA0	3C6
SCSC0200	OT	311	10/12		HIJ0	2F7
SCSC0210	OT	007	10/12		EFG0	2A7
SCSC0220	OT	206	10/12		BCD0	2C7
SCSC0230	OT	205	10/12		ABCEFHI0	2D7
SCSC0240	OT	305	10/12		ABDEGHJ0	2D7
SCSC0250	OT	304	10/12		ACDFGIJ0	2D7
SC02R00P	I	104	TO CONN CKT		RSCOP	3C2
SC02R01P	I	103	TO CONN CKT		RSCJP	3F2
SC02R02P	I	312	TO CONN CKT		RSCIP	3E2
SC02R03P	I	102	TO CONN CKT		RSCHP	3E2
SC02R04P	I	110	TO CONN CKT		RSCCP	3B2
SC02R05P	I	109	TO CONN CKT		RSCBP	3B2
SC02R06P	I	313	TO CONN CKT		RSCAP	3A2
SC02R07P	I	101	TO CONN CKT		RSCGP	3D2
SC02R08P	I	316	TO CONN CKT		RSCFP	3D2
SC02R09P	I	201	TO CONN CKT		RSCEP	3D2
SC02S00P	O	117	TO CONN CKT		SSCDP	2B7
SC02S01P	O	114	TO CONN CKT		SSCJP	2E7
SC02S02P	O	113	TO CONN CKT		SSCIP	2F7
SC02S03P	O	112	TO CONN CKT		SSCHP	2G7
SC02S04P	O	116	TO CONN CKT		SSCCP	2C7
SC02S05P	O	115	TO CONN CKT		SSCBP	2C7
SC02S06P	O	318	TO CONN CKT		SSCAP	2D7
SC02S07P	O	111	TO CONN CKT		SSCGP	2G7
SC02S08P	O	317	TO CONN CKT		SSCFP	2H7
SC02S09P	O	118	TO CONN CKT		SSCEP	2B7
SDATA020	I	108	10/10		SDATA0	2C3
SHIFT020	OT	204	10/12		SHFT0	3B6
3T058E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1013B	I	001			RSCGN	3E2
	I	002			RSCHN	3E2
	I	003			RSCJN	3F2
	I	004			RSCDN	3C2
	I	009			RSCBN	3R2
	I	301			RSCEN	3D2
	GRD	200			GRD	
3VG1013T	OT	011			SSCGN	2G7
	OT	012			SSCHN	2F7
	OT	013			SSCIN	2F7
	OT	014			SSCJN	2E7
	OT	015			SSCBN	2C7
	OT	016			SSCCN	2B7

SYMBOL NO. 11 (CONT)

I/O SUBCHANNELS 00-09

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
1002SCA	10-13	FC201	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG1013T	OT	017			SSCDN	2B7
	OT	018			SSCEN	2A7
	OT	217			SSCFN	2H7
	OT	218			SSCAN	2D7
	I	010			RSCCN	3C2
	I	212			RSCIN	3F2
	I	213			RSCAN	3B2
	I	216			RSCFN	3D2
	GRD	319			GRD	
3V058E	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 12

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
1002SCB	10-14	FC201	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
ESC02100	I	209	10/9		ESCJ0	2E3
ESC02110	I	310	10/9		ESCI0	2F3
ESC02120	I	211	10/9		ESCH0	2F3
ESC02130	I	005	10/9		ESCF0	2H3
ESC02140	I	008	10/9		ESCE0	2B3
ESC02150	I	208	10/9		ESCB0	2D3
ESC02160	I	306	10/9		ESCC0	2C3
ESC02170	I	207	10/9		ESCD0	2B3
ESC02180	I	308	10/9		ESCA0	2D3
ESC02190	I	105	10/9		ESCG0	2G3
GO.020B	I	006	10/10		GO.DLY0	2B3
IOLE020	I	203	10/9		INIT0	3A2
IO.P21	I	106	8/5		P21	2C3
IO.P31	I	307	8/5		P31	2C3
RDATA020	OT	303	10/11		RDATA0	3C6
	I		10/10			
SCSC0200	OT	304	10/11		ACDFGIJ0	2D7
	I		10/9			
SCSC0210	OT	305	10/11		ABDEGHJ0	2D7
	I		10/9			
SCSC0220	OT	205	10/11		ABCEFHI0	2D7
	I		10/9			
SCSC0230	OT	206	10/11		BCD0	2C7
	I		10/9			
SCSC0240	OT	007	10/11		EFG0	2A7
	I		10/9			
SCSC0250	OT	311	10/11		HIJ0	2F7
	I		10/9			
SC02R10P	I	103	TO CONN CKT		RSCJP	3F2
SC02R11P	I	312	TO CONN CKT		RSCIP	3E2
SC02R12P	I	102	TO CONN CKT		RSCHP	3E2
SC02R13P	I	316	TO CONN CKT		RSCFP	3D2
SC02R14P	I	201	TO CONN CKT		RSCEP	3D2
SC02R15P	I	109	TO CONN CKT		RSCBP	3B2

SYMBOL NO. 12 (CONT)

I/O SUBCHANNELS 10-19

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
1002SCB	10-14	FC201	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SC02R16P	I	110	TO CONN CKT		RSCCP	3B2
SC02R17P	I	104	TO CONN CKT		RSCDP	3C2
SC02R18P	I	313	TO CONN CKT		RSCAP	3A2
SC02R19P	I	101	TO CONN CKT		RSCGP	3D2
SC02S10P	O	114	TO CONN CKT		SSCJP	2E7
SC02S11P	O	113	TO CONN CKT		SSCIP	2F7
SC02S12P	O	112	TO CONN CKT		SSCHP	2G7
SC02S13P	O	317	TO CONN CKT		SSCFP	2H7
SC02S14P	O	118	TO CONN CKT		SSCEP	2B7
SC02S15P	O	115	TO CONN CKT		SSCBP	2C7
SC02S16P	O	116	TO CONN CKT		SSCCP	2C7
SC02S17P	O	117	TO CONN CKT		SSCDP	2B7
SC02S18P	O	318	TO CONN CKT		SSCAP	2D7
SC02S19P	O	111	TO CONN CKT		SSCGP	2G7
SDATA020	I	108	10/10		SDATA0	2C3
SHIFT020	OT	204	10/11		SHFT0	3B6
	I		10/10			
3T058E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG1014B	I	001			RSCGN	3E2
	I	002			RSCHN	3E2
	I	003			RSCJN	3F2
	I	004			RSCDN	3C2
	I	009			RSCBN	3B2
	I	301			RSCEN	3D2
	GRD	200			GRD	
3VG1014T	OT	011			SSCGN	2G7
	OT	012			SSCHN	2F7
	OT	013			SSCIN	2F7
	OT	014			SSCJN	2E7
	OT	015			SSCBN	2C7
	OT	016			SSCCN	2B7
	OT	017			SSCDN	2B7
	OT	018			SSCEN	2A7
	OT	217			SSCFN	2H7
	OT	218			SSCAN	2D7
	I	010			RSCCN	3C2
	I	212			RSCIN	3F2
	I	213			RSCAN	3B2
	I	216			RSCFN	3D2
	GRD	319			GRD	
3V058E	PWR	000		203	+3	
	PWR	119		203	+3	

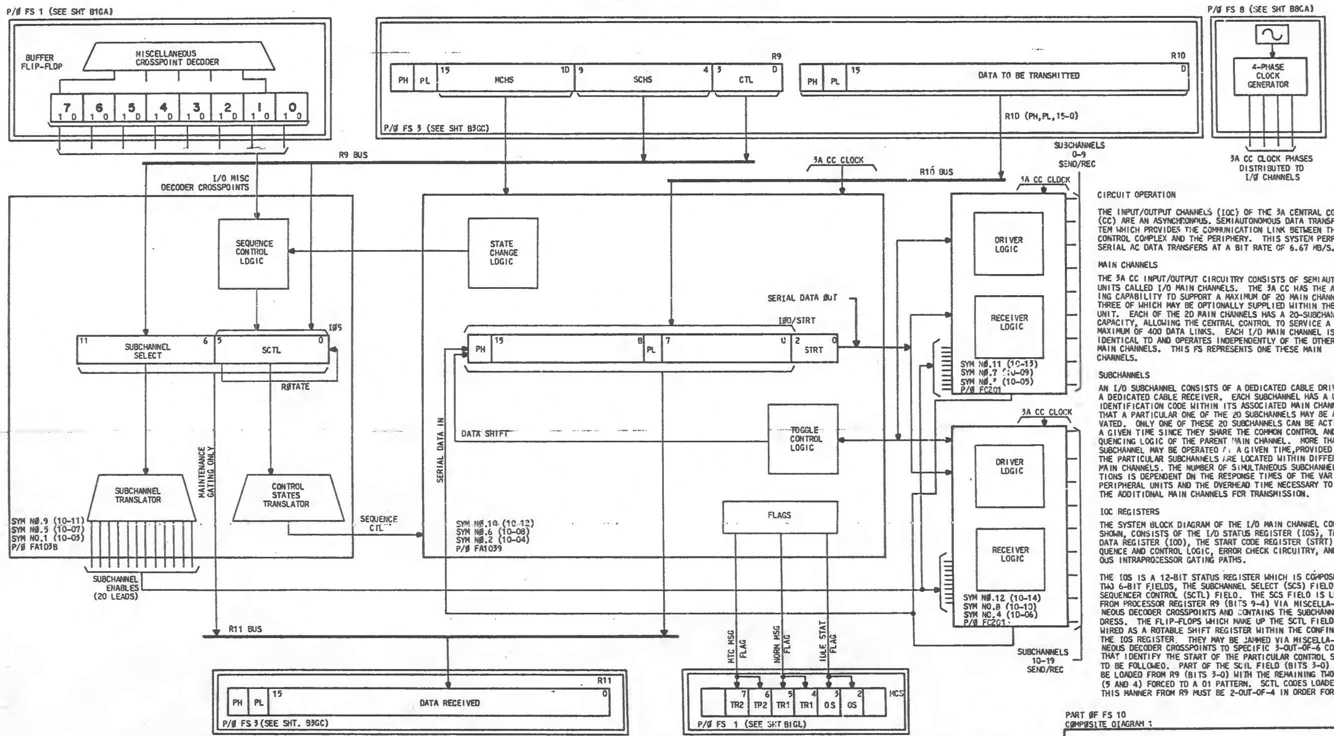
PART OF FS 10
SYMBOL(S) 11 12

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	B10CF

PRINTED IN U. S. A.
06/10/77

PART OF FS 10
I/Ø CHANNELS

COMPOSITE DIAGRAM 1
FUNCTIONAL PARTITIONING OF I/Ø CHANNEL



CIRCUIT OPERATION

THE INPUT/OUTPUT CHANNELS (IOC) OF THE 3A CENTRAL CONTROL (CC) ARE AN ASYNCHRONOUS. SEMIAUTONOMOUS DATA TRANSFER SYSTEM WHICH PROVIDES THE COMMUNICATION LINK BETWEEN THE 3A CONTROL COMPLEX AND THE PERIPHERY. THIS SYSTEM PERFORMS SERIAL AC DATA TRANSFERS AT A BIT RATE OF 6.67 MB/S.

MAIN CHANNELS

THE 3A CC INPUT/OUTPUT CIRCUITRY CONSISTS OF SEMIAUTONOMOUS UNITS CALLED I/O MAIN CHANNELS. THE 3A CC HAS THE ADDRESSING CAPABILITY TO SUPPORT A MAXIMUM OF 20 MAIN CHANNELS, THREE OF WHICH MAY BE OPTIONALLY SUPPLIED WITHIN THE UNIT. EACH OF THE 20 MAIN CHANNELS HAS A 20-SUBCHANNEL CAPACITY, ALLOWING THE CENTRAL CONTROL TO SERVICE A MAXIMUM OF 400 DATA LINKS. EACH I/O MAIN CHANNEL IS IDENTICAL TO AND OPERATES INDEPENDENTLY OF THE OTHER MAIN CHANNELS. THIS FS REPRESENTS ONE THESE MAIN CHANNELS.

SUBCHANNELS

AN I/O SUBCHANNEL CONSISTS OF A DEDICATED CABLE DRIVER AND A DEDICATED CABLE RECEIVER. EACH SUBCHANNEL HAS A UNIQUE IDENTIFICATION CODE WITHIN ITS ASSOCIATED MAIN CHANNEL SO THAT A PARTICULAR ONE OF THE 20 SUBCHANNELS MAY BE ACTIVATED. ONLY ONE OF THESE 20 SUBCHANNELS CAN BE ACTIVE AT A GIVEN TIME SINCE THEY SHARE THE COMMON CONTROL AND SEQUENCING LOGIC OF THE PARENT MAIN CHANNEL. MORE THAN ONE SUBCHANNEL MAY BE OPERATED AT A GIVEN TIME, PROVIDED THAT THE PARTICULAR SUBCHANNELS ARE LOCATED WITHIN DIFFERENT MAIN CHANNELS. THE NUMBER OF SIMULTANEOUS SUBCHANNEL OPERATIONS IS DEPENDENT ON THE RESPONSE TIMES OF THE VARIOUS PERIPHERAL UNITS AND THE OVERHEAD TIME NECESSARY TO SET UP THE ADDITIONAL MAIN CHANNELS FOR TRANSMISSION.

IOC REGISTERS

THE SYSTEM BLOCK DIAGRAM OF THE I/O MAIN CHANNEL CONTROLLER SHOWN, CONSISTS OF THE I/O STATUS REGISTER (IOS), THE I/O DATA REGISTER (IOD), THE START CODE REGISTER (STRT), SEQUENCE AND CONTROL LOGIC, ERROR CHECK CIRCUITRY, AND VARIOUS INTRAPROCESSOR GATING PATHS.

THE IOS IS A 12-BIT STATUS REGISTER WHICH IS COMPOSED OF TWO 6-BIT FIELDS, THE SUBCHANNEL SELECT (SCS) FIELD AND THE SEQUENCER CONTROL (SCTL) FIELD. THE SCS FIELD IS LOADED FROM PROCESSOR REGISTER R9 (BITS 9-4) VIA MISCELLANEOUS DECODER CROSSPOINTS AND CONTAINS THE SUBCHANNEL ADDRESS. THE FLIP-FLOPS WHICH MAKE UP THE SCTL FIELD ARE WIRED AS A ROTABLE SHIFT REGISTER WITHIN THE CONFINES OF THE IOS REGISTER. THEY MAY BE JAMMED VIA MISCELLANEOUS DECODER CROSSPOINTS TO SPECIFIC 3-OUT-OF-6 CONSTANTS THAT IDENTIFY THE START OF THE PARTICULAR CONTROL SEQUENCE TO BE FOLLOWED. PART OF THE SCTL FIELD (BITS 3-0) MAY ALSO BE LOADED FROM R9 (BITS 3-0) WITH THE REMAINING TWO BITS (5 AND 4) FORCED TO A 01 PATTERN. SCTL CODES LOADED IN THIS MANNER FROM R9 MUST BE 2-OUT-OF-4 IN ORDER FOR THE

CIRCUIT OPERATION (CONT)

6-BIT SCTL FIELD TO CONTAIN THE VALID 3-OUT-OF-6 CONFIGURATION. THE SCTL FIELD FUNCTIONS AS THE SEQUENCE CODE GENERATOR WITHIN THE OPERATION OF THE IOC SEQUENCER. FOR MAINTENANCE PURPOSES, THE IOS MAY BE UNLOADED TO PROCESSOR REGISTER R11 (OUTPUT BUFFER) VIA THE R11 GATING BUS.

THE IOD IS AN 18-BIT SHIFT REGISTER WHICH FUNCTIONS AS A TRANSMIT/RECEIVE BUFFER FOR THE DATA PORTION OF AN I/D

CIRCUIT OPERATION (CONT)

MESSAGE. THIS REGISTER MAY BE PARALLEL LOADED VIA A SPECIAL R1D GATING BUS FROM CC REGISTER R1D AND UNLOADED VIA THE R11 GATING BUS TO THE CC REGISTER R11.

STRT IS A 3-BIT SHIFT REGISTER APPENDED TO THE LOW END OF THE IOD TO ACCOMODATE THE START CODES. IT MAY BE FORCED TO SPECIFIC BIT CONFIGURATIONS BY PARTICULAR CONTROL SIGNALS. THIS REGISTER CANNOT BE GATED INTO OR GATED FROM;

CIRCUIT OPERATION (CONT)

IT IS STRICTLY AN INTERNAL IOC REGISTER.

THE IOD TOGETHER WITH THE STRT MAKES UP THE SINGLE 21-BIT IOC SHIFT REGISTER.

PART ØF FS 10
CØMPØSITE DIAGRAM 1

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

BIOGA

E-7021 (12-73)

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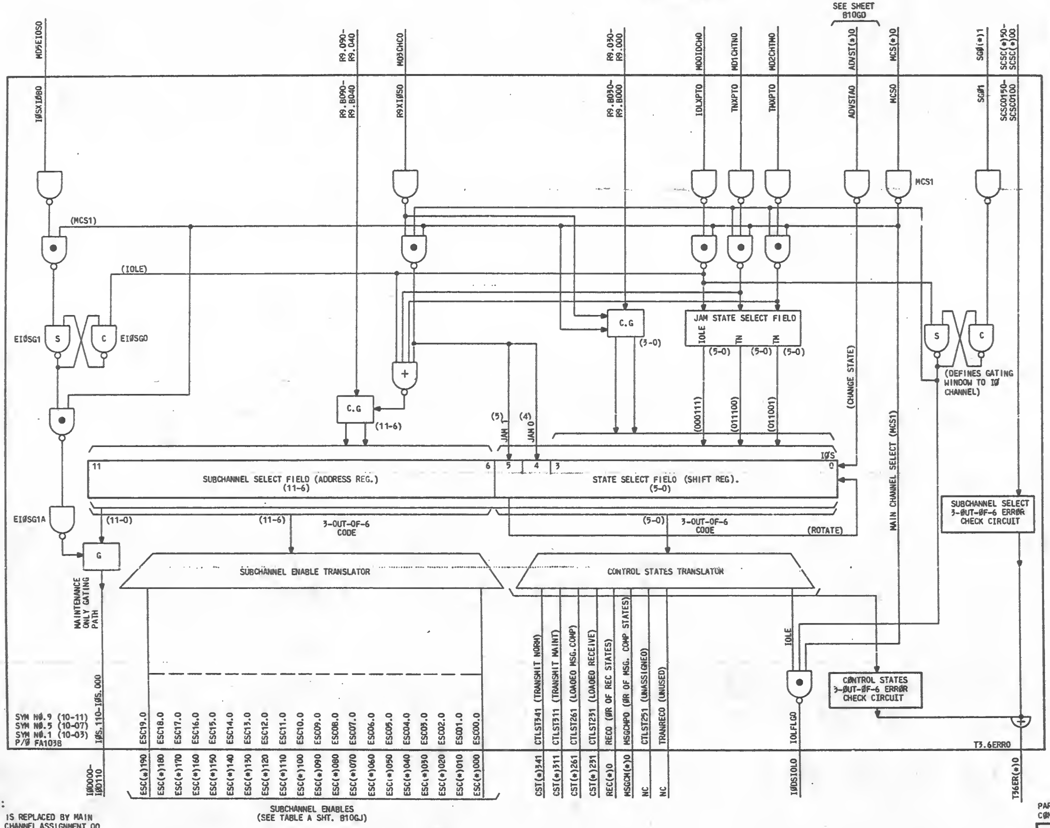
PART OF FS 10

I/Ø CHANNELS

COMPOSITE DIAGRAM 2

I/Ø STATUS REGISTER



NOTE:

(*) IS REPLACED BY MAIN CHANNEL ASSIGNMENT 00, 01,02,ETC.

CIRCUIT OPERATION

3A CC/IOC INTERFACE

THE 3A CC PROCESSOR INTERFACES WITH THE I/O CIRCUITRY AT THE MAIN CHANNEL LEVEL. EACH MAIN CHANNEL IS ASSIGNED A UNIQUE 3-OUT-OF-6 IDENTIFICATION CODE, THE MAIN CHANNEL SELECT (MCS) CODE. USING THIS CODE IN COMBINATION WITH A PARTICULAR MISCELLANEOUS DECODER SIGNAL THE DESIRED CONTROL OR GATING FUNCTION IS PERFORMED ON THE SELECTED MAIN CHANNEL. DATA IS TRANSFERRED TO AND FROM THE MAIN CHANNELS OVER SPECIAL PARALLEL GATING BUSES VIA THREE OF THE 16 GENERAL REGISTERS IN THE PROCESSOR, R9, R10, AND R11. R9 IS THE I/O CONTROL BUFFER AND CONTAINS THE MAIN CHANNEL AND SUBCHANNEL ADDRESS INFORMATION TOGETHER WITH A 4-BIT CONTROL FIELD. THE MCS ADDRESS INFORMATION (BITS 15-10) IS DECODED ON THE PROCESSOR BACKPLANE BY SELECTIVELY WIRING A UNIQUE COMBINATION OF THREE OF SIX MCS LEADS TO EACH MAIN CHANNEL (SEE SHEET B10GC). THESE THREE LEADS ARE THEN ANDED WITHIN EACH MAIN CHANNEL TO PRODUCE A SINGLE ENABLE SIGNAL. ONLY THE SELECTED MAIN CHANNEL SIMULTANEOUSLY RECEIVES ALL THREE OF ITS MCS LEADS ACTIVE. THIS SELECTIVE ENABLE IS THEN USED TO STEER CONTROL AND DATA INFORMATION TO AND FROM THE COMMON I/O CHANNEL INTERFACE REGISTERS WITHIN THE 3A CC TO THE ADDRESSED MAIN CHANNEL.

THREE SPECIAL PARALLEL GATING BUSES HANDLE ALL THE DATA COMMUNICATION BETWEEN THE 3A CC AND THE I/O MAIN CHANNEL REGISTERS.

THE CONTENTS OF REGISTERS R9, R10, AND THE SELECTED IOD ARE ALWAYS PRESENT ON THEIR RESPECTIVE OUTGOING GATING BUSES. ALL GATING CONTROL IS PERFORMED AT THE DESTINATION REGISTERS BY THE APPROPRIATE GATING COMMANDS. THIS ALLOWS SUFFICIENT TIME FOR THE DATA ON THE BUSES TO REACH STEADY STATE PRIOR TO THE EXECUTION OF THE GATING COMMAND.

AN EXCEPTION TO THE AFOREMENTIONED GATING PROCEDURE EXISTS IN THAT TWO REGISTERS PER I/O MAIN CHANNEL (THE IOS AND THE IOD) ARE BOTH PERMITTED ACCESS TO THE R11 GATING BUS. ONE REGISTER, THE IOD, IS NORMALLY CONNECTED TO THIS BUS SUBJECT ONLY TO THE MCS ENABLE SIGNAL DISCUSSED EARLIER. FOR THE IOS TO GAIN ACCESS, THE FOLLOWING SEQUENCE OF MICROINSTRUCTIONS MUST BE PERFORMED. (NOTE THAT THIS FUNCTION IS RESTRICTED, AND IS USED ONLY FOR MAINTENANCE PURPOSES.)

- A) ZERO THE IOD - ZEROING THE IOD ALLOWS THE I/Ø R11 BUS TO BE DRIVEN HIGH (LOGICAL 1=GROUND,LOGICAL 0=HIGH).
- B) EXECUTE THE MD5EIOS MICROINSTRUCTION WHICH ALLOWS THE CONTENTS OF THE IOS TO "OR" WITH THE OUTPUTS OF THE IOD ON THE R11 BUS, WITH THE LOGICAL 1 (GROUND LEVEL)THE DOMINENT SIGNAL. [THE IOS OUTPUTS WILL REMAIN 'ORED' TO THE I/O RETURN DATA BUS UNTIL THE EXECUTION OF THE MICROINSTRUCTION WHICH IDLES THE CHANNEL (MD0IDCH).]
- C) EXECUTE THE IODXR11 MICROINSTRUCTION WHICH GATES THE DATA FROM THE I/O RETURN DATA BUS INTO R11.
- D) EXECUTE THE MD0IDCH MICROINSTRUCTION WHICH INITIALIZES THE CHANNEL AND REMOVES THE "OR" FUNCTION SET UP ABOVE.

I/O CHANNEL CONTROL SIGNALS

THE 3A CC CONTROL OF THE I/O CHANNELS IS ACCOMPLESHED VIA A DEDICATED SUBSET OF NINE MISCELLANEOUS DECODER CONTROL SIGNALS THESE SIGNALS ONLY AFFECT THE MAIN CHANNEL ADDRESSED BY THE MCS FIELD (BITS 15-10) OF REGISTER R9. THESE CONTROL SIGNALS MAY ONLY BE ISSUED AT THE MICROINSTRUCTION LEVEL.

1. MD0IDCH - LOADS THE SCS FIELD IN THE IOS FROM R9 (BITS 9-4). PLACES THE CHANNEL SEQUENCER INTO THE IDLE STATE, INITIALIZES THE IOC, AND OPENS THE GATING WINDOW,
2. MD1CHTN - LOADS THE SCS FIELD IN THE IOS FROM R9 (BITS 9-4) AND SETS UP THE SCTL FIELD IN THE IOS FOR THE TRANSMIT NORMAL SEQUENCE.
3. MD2CHTM - LOADS THE SCS FIELD IN THE IOS FROM R9 (BITS 9-4) AND SETS UP THE SCTL FIELD IN THE IOS FOR THE TRANSMIT MAINTENANCE SEQUENCE.
4. MD3CHC - LOADS THE SCS FIELD IN THE IOS FROM R9 (BITS 9-4) AND LOADS THE SCTL FIELD FROM R9 (BITS 3-0). MD3CHC ALSO JAMS A 01 PATTERN INTO IOS BITS 5 AND 4, RESPECTIVELY.
5. MD4STCH - STARTS THE MAIN CHANNEL SEQUENCER AND CLOSES THE GATING WINDOW.
6. MD5EIOS - ENABLES GATING FROM THE IOS TO THE R11 GATING BUS. THIS SIGNAL IS FOR MAINTENANCE USE ONLY.
7. MD6RAIO - GATES THE ENTIRE CONTENTS OF R10, INCLUDING THE PARITY BITS, TO THE IOD REGISTER.
8. IODXR11 - GATES THE ENTIRE CONTENTS OF THE IOD REGISTER, INCLUDING THE PARITY BITS, TO R11 VIA THE R11 BUS.
9. TCH (TEST I/O CHANNEL) - LOADS THE CC'S STATUS FLIP-FLOPS WITH THE FOLLOWING I/O CHANNEL FLAGS.
   - A) IDLE - SETS THE DS BIT.
   - B) MESSAGE COMPLETE NORMAL - SETS THE TR1 BIT.
   - C) MESSAGE COMPLETE MAINTENANCE - SETS THE TR2 BIT.

   (DS, TR1, AND TR2 ARE MICROCONTROL STATUS FLIP-FLOPS USED BY THE MICROPROGRAM AS DECISION BITS.

PART ØF FS 10
CØMPØSITE DIAGRAM 2

ISSUE
5A

3A CENTRAL CONTROL

SD-1C900-01-B10GB

BELL TELEPHONE LABORATORIES
INCORPORATED

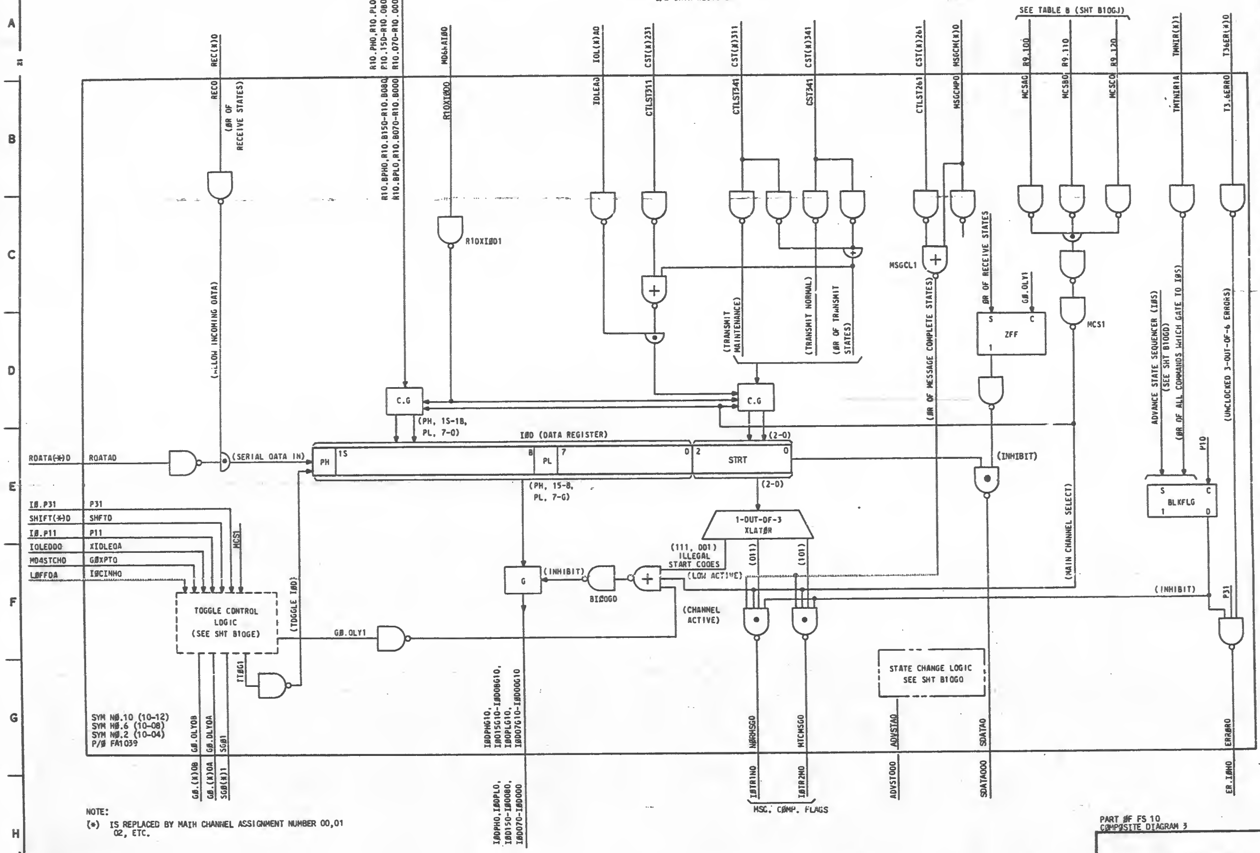
6S

PART OF FS 10

I/Ø CHANNELS

COMPOSITE DIAGRAM 3

I/Ø DATA REGISTER



SYM NØ.10 (10-12)
SYM NØ.6 (10-08)
SYM NØ.2 (10-04)
P/Ø FA1039

NOTE:
(✱) IS REPLACED BY MAIN CHANNEL ASSIGNMENT NUMBER 00,01 02, ETC.

CIRCUIT OPERATION

IOC MESSAGE FORMATS

IN THE NORMAL OPERATIONAL MODE, A 2-BIT SERIAL MESSAGE IS OUTPULSED TO THE SELECTED PERIPHERAL UNIT AND, IN RESPONSE, A 21-BIT SERIAL MESSAGE IS RETURNED FROM THAT UNIT. THE MESSAGE CONTAINS A 3-BIT START CODE AND AN 18-BIT DATA FIELD, WHICH INCLUDES TWO PARITY BITS AND TWO 8-BIT FIELDS. THE MESSAGE HAS EVEN PARITY OVERALL, WITH THE TWO PARITY BITS MAINTAINING ODD PARITY OVER THEIR RESPECTIVE 8-BIT FIELDS.

THE TWO LEGAL START CODES FOR AN I/O MESSAGE ARE 011 AND 101. THESE 3-BIT START CODES CONTAIN LEADING 1'S SO THAT THE ASYNCHRONOUS RECEIVING CONTROLLER CAN RECOGNIZE THE START OF A MESSAGE. ONE BIT MUST BE A ZERO TO INDICATE THAT THE SHIFT REGISTER CAN OUTPULSE BOTH 1'S AND 0'S. THE REMAINING BIT MUST BE A 1 TO PRESERVE PARITY OVER THE MESSAGE. NO PARITY GENERATION IS REQUIRED WITHIN THE IOC; PARITY IS CALCULATED WITHIN THE 3ACC PROCESSOR AND GATED WITH THE 16 DATA BITS TO THE IOC.

THE 011 PATTERN HAS BEEN NAMED THE "NORMAL" START CODE AND THE 101 THE "MAINTENANCE" START CODE. THE TERMS "NORMAL" AND "MAINTENANCE" HAVE BEEN ADOPTED AS SOFTWARE NAMING CONVENTIONS BUT DO NOT IMPLY ANY HARDWARE DIFFERENCES IN THE WAY THESE TWO START CODES ARE TREATED.

THE START CODE OF AN INCOMING MESSAGE TO AN IOC MUST ALSO HAVE THE ABOVE FORMAT. THE IOC WILL RECOGNIZE EITHER OF THE TWO LEGAL START CODES AND, UPON RECEPTION, WILL RAISE SEPARATE FLAGS TO THE PROCESSOR TO DIFFERENTIATE BETWEEN THEM. ILLEGAL START CODES WILL ALSO BE RECOGNIZED AND HANDLED APPROPRIATELY (SEE SHEET B10GO).

FLIP-FLOP BLKFLG IS SET BY ALL THE FUNCTIONS WHICH CAUSE THE IØS REGISTER TO CHANGE STATE IN SOME WAY. WHEN SET, THIS FLIP-FLOP BLOCKS THE OUTPUT OF THE 3-OUT-OF-6 ERROR CIRCUITRY WHILE THESE DATA INPUTS ARE UNSTABLE (i.e. BEING PARALLEL LOADED FROM THE CC OR THE SCTL FIELD BEING TOGGLED BY THE STATE CHANGE LOGIC.) THE MESSAGE COMPLETE FLAGS ARE ALSO BLOCKED BY THIS FLIP-FLOP SO THAT THE FLAGS ARE BLOCKED FROM P3 LEADING EDGE TO P1 LEADING EDGE ONE CYCLE LATER. THIS ASSURES THAT THESE FLAGS WILL BE STABLE AND PRESENT DURING THE ENTIRE STROBE INTERVAL OF THE TEST FLAGS COMMAND (TIØ). THE COMMAND SIGNALS ACTIVATE AT THE P1 LEADING EDGE. SINCE THERE ARE TWO COPIES OF TR1 AND TR2, MARGINAL FLAGS MAY BE SEEN BY ONE COPY AND MISSED BY THE OTHER, CAUSING FAULTY OPERATION.

AFTER ENTRY INTO THE RECEIVE STATE, THE BIPOLAR INTERFACE LOGIC CONTINUES TO TRANSMIT ZERO DATA (TIMING PULSES) UNTIL THE MESSAGE COMPLETE STATE IS REACHED. FLIP-FLOP ZFF, SET BY ENTRY INTO THE RECEIVE STATE, FORCES AND HOLDS THE SERIAL DATA OUTPUT NET SDATAOOO POSITIVE (INACTIVE-ZERO DATA) THROUGHOUT THIS INTERVAL.

PART ØF FS 10
CØMPØSITE DIAGRAM 3

ISSUE 5A

3A CENTRAL CONTROL

SD-1C900-01-B10GC

BELL TELEPHONE LABORATORIES
INCORPORATED

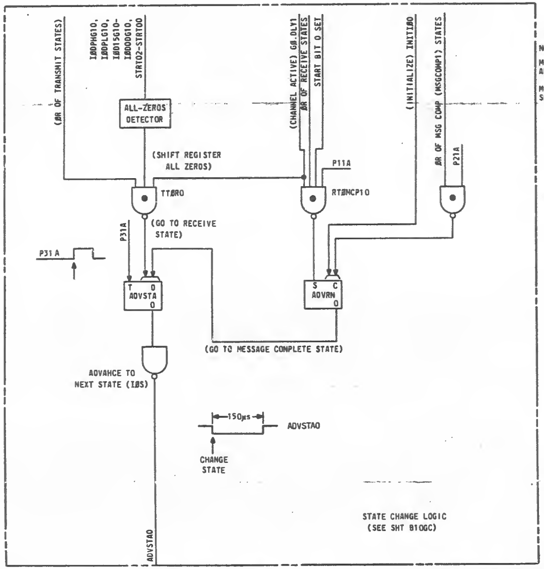
6S

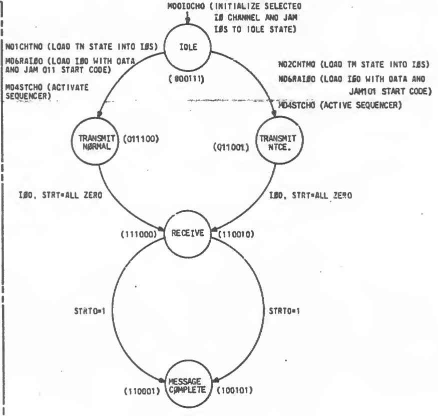
PART OF FS 10

I/Ø CHANNELS

COMPOSITE DIAGRAM 4

STATE CHANGE LOGIC




M00IOCH0 (INITIALIZE SELECTED IØ CHANNEL AND JAM IØS TO IDLE STATE)
IDLE
(000111)
N01CHTN0 (LOAD TN STATE INTO IØS)
M06RAIØ0 (LOAD IØ0 WITH DATA AND JAM 011 START CODE)
M04STCH0 (ACTIVATE SEQUENCER)
N02CHTM0 (LOAD TM STATE INTO IØS)
N06RAIØ0 (LOAD IØ0 WITH DATA AND JAM101 START CODE)
M04STCH0 (ACTIVE SEQUENCER)
TRANSMIT NØRMAL
(011100)
(011001)
TRANSMIT NTCE.
IØ0, STRT=ALL ZERO
IØ0, STRT=ALL ZERO
(111000)
RECEIVE
(110010)
STRT0=1
STRT0=1
(110001)
MESSAGE CØMPLETE
(100101)

IØ CHANNEL
SEQUENCE STATE DIAGRAM

FIG. 1

CIRCUIT OPERATION

IOC SEQUENCER

THE AUTONOMOUS CONTROL OF THE I/O MAIN CHANNEL IS PERFORMED BY THE IOC SEQUENCER. ONCE INITIATED, THIS SEQUENCER DIRECTS THE ENTIRE TRANSMIT/RECEIVE OPERATION OF THE IOC WITHOUT THE NECESSITY OF SOFTWARE INTERVENTION. THE STATE DIAGRAM OF THIS SEQUENCER IS SHOWN IN FIG. 1.

THE IOC MAY PERFORM TWO MAJOR TRANSMIT SEQUENCES: TRANSMIT NORMAL AND TRANSMIT MAINTENANCE. THE SEQUENCER CONTAINS FOUR MAJOR STATES: IDLE, TRANSMIT, RECEIVE, AND MESSAGE COMPLETE. ALTHOUGH EACH OF THE TWO SEQUENCES ARE SLIGHTLY DIFFERENT, EACH CONTAINS THE SAME MAJOR STATES. THE SEQUENCE CODES WHICH IDENTIFY THE SEQUENCE AND THE STATES WITHIN THAT SEQUECNE ARE ALL UNIQUE 3-OUT-OF-6 CODES.

THE IOC SEQUENCE LOGIC CONTAINS A 3-OUT-OF-6 STATE CODE GENERATOR, A 3-OUT-OF-6 TO 1-OUT-OF-20 STATE DECODER, AND THE LOGIC NECESSARY TO PRODUCE THE STATE CHANGE SIGNALS. THE STATE CODE GENERATOR FOR THE IOC PHYSICALLY RESIDES IN THE LOWER SIX BITS OF THE IOS REGISTER (THE SCTL FIELD). THIS 6-BIT CODE GENERATOR IS DESIGNED AS A ROTATING SHIFT REGISTER WHICH PRODUCES SEQUENTIAL STATE CODES IN RESPONSE TO SIMPLE SHIFT PULSES. A GIVEN CONTROL SEQUENCE IS SET UP BY JAMMING THE IOS CONTROL FIELD UNDER PROGRAM CONTROL TO A UNIQUE 3-OUT-OF-6 CODE WHICH IDENTIFIES THE START OF THE DESIRED SEQUENCE. STATE CHANGES ARE ACCOMPLISHED SIMPLY BY TOGGLING THE SHIFT LEAD OF THIS CODE GENERATOR WHICH ROTATES THE PREVIOUS 3-OUT-OF-6 STATE CODE ONE BIT POSITION TO THE LEFT. THIS YIELDS A SECOND 3-OUT-OF-6 STATE CODE WHICH REPRESENTS THE NEXT STATE IN THAT PARTICULAR SEQUENCE. THIS ACTION CONTINUES UNTIL THE ENTIRE SEQUENCE HAS BEEN COMPLETED. NOTE THAT AT ANY TIME WITHIN A GIVEN SEQUENCE, THE 3ACC MAY OVERRIDE THE IOC AND ABORT THE SEQUENCE, RETURNING THE IOC TO THE IDLE STATE.

STATE CHANGE LOGIC

A BLOCK OF COMBINATIONAL LOGIC WITHIN THE IOC SEQUENCER IS DEDICATED TO THE GENERATION OF STATE CHANGE SIGNALS. SINCE EACH STATE IN EVERY SEQUENCE IS UNIQUE (A PARTICULAR 3-OUT-OF-6 CODE PER STATE PER SEQUENCE), THE CRITERION FOR ENTRY INTO THE NEXT STATE IS THE PRESENCE OF A PARTICULAR STATE CODE IN COMBINATION WITH THE CORRECT SET OF EXTERNAL CONDITIONS. HAVING NET THESE CONDITIONS, THE NEXT SEQUENTIAL STATE IS ENTERED AND THE NEXT TASK IN THE SEQUENCE IS PERFORMED.

THE ADVSTAO NODE CONTROLS THE TOGGLE TO THE STATE CODE GENERATOR (SCTL PORTION OF THE IØS). THE STATE CHANGE TAKES PLACE ON THE HIGH-TO-LOW TRANSITION OF ADVSTAO.

(1) TRANSMIT TO RECEIVE - GATE TTØRO DETECTS THIS STATE CHANGE. THE PRESENCE OF ALL ZEROS IN THE IØD/STRT SHIFT REGISTER WITH THE I/Ø CHANNEL ACTIVE AND IN THE TRANSMIT STATE, MARKS THE END OF THE TRANSMISSION FLIP-FLOP ADVSTA IS RESET BY THE LEADING EDGE OF CLOCK PHASE P31, DRIVING NODE ADVSTAO LOW. GATE TTØRO DEACTIVATES WHEN THE STATE CHANGE IS DETECTED ALLOWING THE ADVSTA FLIP-FLOP TO SET AGAIN.

(2) RECEIVE TO MESSAGE COMPLETE - THIS STATE TRANSITION IS MADE ON DATA WHICH IS ASYNCHRONOUS TO THE SYSTEM CLOCK PHASES, AND THE STATE CHANGE LOGIC IS CLOCK SYNCHRONOUS. THEREFORE, ANOTHER FLIP-FLOP IS UTILIZED TO ATTAIN CLOCK SYNCHRONISM BEFORE RESETTING ADVSTA. GATE RTØMCP10 LOOKS FOR THE IOC TO BE ACTIVE (GØ.DLY1=1) IN THE RECEIVE STATE AND THE START (STRT00) BIT SET. THIS GATE IS STROBBED BY CLOCK P1 GUARANTEEING FLIP-FLOP ADVRM BECOMING SET DURING SOME P1 (WHICH ONE IS NOT IMPORTANT), ALLOWING THE "D" INPUT TO ADVSTA TO BE STABILIZED BY THE LEADING EDGE OF P31. ADVRM IS CLEARED AT P2 WHEN THE MESSAGE COMPLETE STATE IS ACTIVATED WHICH IN TURN ALLOWS ADVSTA TO CLEAR ON THE FOLLOWING P3.

TRANSMIT/RECEIVE SEQUENCER

THE SEND IO (SIO) MAIN MEMORY INSTRUCTION INITIATES A SERIES OF MICROPROGRAM INSTRUCTIONS WHICH INITIALIZES THE MAIN CHANNEL SPECIFIED BY THE MCS FIELD OF R9. THIS INITIALIZATION MICROINSTRUCTION (M00IDCH) ALSO JAMS THE IDLE STATE IN THE CONTROL FIELD OF THE IOS, AND PLACES THE MAIN CHANNEL IN A MODE WHICH ENABLES IT TO RESPOND TO ADDITIONAL MICROINSTRUCTIONS DIRECTED TO IT. (SEE SHEET B10GB.) NEXT THE MICROPROGRAM GATING COMMANDS ARE USED TO GATE R9 AND R10 INTO IOS AND IOD, RESPECTIVELY, AND ALSO TO PERFORM THE DATA LOOP-AROUND TO CHECK THE DATA PATHS FROM R10 TO IOD AND FROM IOD TO R11. THE ISSUANCE OF THE START CHANNEL MICROINSTRUCTION (MD4STCH) CLOSES THE GATING WINDOW OPENED BY THE IDLE MICROINSTRUCTION, JAMS THE NORMAL 3-BIT START CODE (011) INTO THE START REGISTER, AND RELEASES THE SEQUENCER (SGØ1).

CIRCUIT OPERATION (CONT)

THE SEQUENCER. IN THE TRANSMIT STATE, SYNCRONIZES WITH THE 3A CC CLOCK AND BEGINS TO OUTPULSE THE SERIAL MESSAGE CONTAINED IN THE IOD/STRT REGISTER. (THE IOD TOGETHER WITH STRT MAKES UP THE SINGLE 21-BIT IOD/STRT SHIFT REGISTER.) AS THIS DATA IS SERIALLY OUTPULSED TO THE RIGHT, ZEROS ARE ENTERED INTO THE VACATED BIT POSITIONS FROM THE LEFT. THIS ACTION CONTINUES UNTIL ALL ZEROS ARE DETECTED OVER THE IOD/STRT SHIFT REGISTER. THE SEQUENCER THEN ADVANCES TO THE RECEIVE STATE WHILE CONTINUING TO OUTPULSE AN ALL-ZERO DATA STREAM. THE ALL-ZEROS DATA STREAM IS USED BY THE PERIPHERAL CONTROLLER AS A TIMING SOURCE. NOTE THAT THE SEQUENCER MAY ENTER THE RECEIVE STATE PRIOR TO OUTPULSING A COMPLETE 21-BIT MESSAGE IF THE SERIAL MESSAGE ORIGINALLY CONTAINED IN THE IOD/STRT REGISTER HAD TRAILING ZEROS. ADVANCING TO THE RECEIVE STATE PRIOR TO OUTPULSING 21-BITS IS PERMITTED SINCE THE IOC CONTINUES TO OUTPULSE ZEROS IN THE RECEIVE STATE. THE RECEIVING PERIPHERAL CONTROLLER MUST DETERMINE WHEN A COMPLETE MESSAGE HAS BEEN RECEIVED EITHER BY COUNTING THE INCOMING BITS OR BY CHECKING FOR THE PRESENCE OF A START CODE. IN EITHER CASE THE INCOMING DATA STREAM MUST BE INHIBITED TO PREVENT DATA OVERFLOW IN THE SHIFT REGISTER OF THE PERIPHERAL CONTROLLER.

ENTERING THE RECEIVE STATE, THE IOC ENABLES THE SERIAL INPUT TO THE IOD REGISTER. BY DESIGN, NO DATA MAY BE PRESENT ON THIS INCOMING LINE DURING THIS STATE CHANGE. THE STATE CHANGE IS ACCOMPLISHED IN SYNCHRONIZATION WITH THE 3A CC CLOCK AND HAS NO DEFINITE TIME RELATIONSHIP TO THE INCOMING DATA DUE TO VARIOUS TIME DELAYS INTRODUCED BY THE IOC TRANSMIT/RECEIVE LOGIC. THE PERIPHERAL CONTROLLER LOGIC, AND THE VARIABLE LINE LENGTHS ENCOUNTERED. IF THE RECEIVE STATE IS ENTERED WITH DATA PRESENT ON THE INCOMING LINE, MISSED BITS OR OUT-OF-PHASE DATA DETECTION COULD RESULT. ONCE THE RECEIVER CIRCUIT IS OUT OF

CIRCUIT DESCRIPTION (CONT)

PHASE WITH THE INCOMING BIT STREAM, THE ENTIRE MESSAGE IS LOST. FOR THIS REASON NO DATA IS PERMITTED ON THE IOC INCOMING LINE UNTIL THE COMPLETE 21-BIT MESSAGE HAS BEEN RECEIVED BY THE PERIPHERAL CONTROLLER AND 2-BIT TIMES (THE TIME IT TAKES TO OUTPULSE 2 BITS OF DATA) HAVE ELAPSED. THIS DELAY (300ns) GUARANTEES THE PRESENCE OF THE RECEIVE STATE BEFORE THE INCOMING DATA ARRIVES AT THE IOC INPUT PORT.

WHEN IN THE RECEIVE STATE, THE SEQUENCE LOGIC MONITORS THE INCOMING DATA LINE FOR THE RETURN MESSAGE. THE DATA BITS ARE DETECTED, INTERPRETED, AND SHIFTED SERIALLY INTO THE IOD, WHICH DERIVES ITS SHIFT TIMING FROM THE INCOMING DATA, UNTIL THE ENTIRE 21-BIT MESSAGE HAS BEEN RECEIVED AND THE FIRST BIT IN STRT HAS BEEN SET. WHEN THE IOC CONTROLLER DETECTS THIS BIT SET, THE STATE CHANGE LOGIC IMMEDIATELY INHIBITS FURTHER SHIFT PULSES, RESYNCHRONIZES TO THE 3A CC CLOCK TIMING, AND TOGGLES THE STATE CODE GENERATOR TO MESSAGE COMPLETE.

THE MESSAGE COMPLETE STATE CUTS OFF THE ZERO TIMING SIGNALS TO THE PERIPHERAL CONTROLLER, DECODES THE FULL 3-BIT START CODE OF THE RETURNED MESSAGE, AND RAISES THE APPROPRIATE FLAG.

CIRCUIT DESCRIPTION (CONT)

START CODE	FLAG	CONDITION
011	NORMAL	NORMAL MESSAGE PRESENT
101	MAINTENANCE	MAINTENANCE MESSAGE PRESENT
XX1	NORMAL	ILLEAGAL START CODE PRESENT

UPON COMPLETION OF THIS TRANSMIT NORMAL/RECEIVE SEQUENCE, THE IOC REMAINS IN THE MESSAGE COMPLETE STATE UNITL THE IOD IS UNLOADED AND INITIALIZED BY PROGRAM ACTION.

THE SEND MAINTENANCE (SMIO) MAIN MEMORY COMMAND INITIATES THE SAME FUNCTIONAL SEQUENCE EXCEPT THE START CODE JAMMED INTO THE STRT AT THE BEGINNING OF THE SEQUENCE IS THE MAINTENANCE START CODE (101). NOTE THAT IN EITHER CASE, THE START CODE OF THE RETURN MESSAGE IS INDEPENDENT OF THE TYPE OF MESSAGE SENT.

ISSUE
5A

PART ØF FS 10
CØMPØSITE DIAGRAM 4

3A CENTRAL CONTROL

SD-1C900-01-B10GD

BELL TELEPHONE LABORATORIES
INCORPORATED

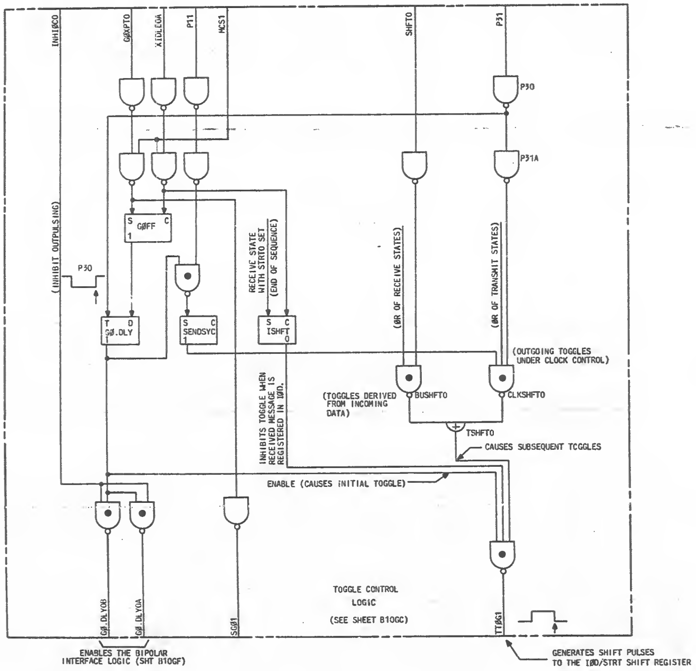
6S

PART OF FS 10

I/O CHANNELS

COMPOSITE DIAGRAM 5

TOGGLE CONTROL LOGIC


INHI0CO
G0XPTO
XIDLEOA
P11
MCS1
SHFTO
P31
P30
P31A
S
C
G0FF
1
(INHIBIT OUTPULSING)
P30
T
D
G0.DLY
1
S
C
SENDSYC
1
RECEIVE STATE WITH STRTO SET (END OF SEQUENCE)
S
C
ISHFT
0
(OR OF RECEIVE STATES)
(OR OF TRANSMIT STATES)
(OUTGOING TOGGLES UNDER CLOCK CONTROL)
(TOGGLES DERIVED FROM INCOMING DATA)
BUSHFTO
CLKSHFTO
TSHFTO
CAUSES SUBSEQUENT TOGGLES
INHIBITS TOGGLE WHEN RECEIVED MESSAGE IS REGISTERED IN I0D.
ENABLE (CAUSES INITIAL TOGGLE)
TOGGLE CONTROL LOGIC
(SEE SHEET B10GC)
G0.DLY0B
G0.DLY0A
SG01
TT0G1
ENABLES THE BIPOLAR INTERFACE LOGIC (SHT B10GF)
GENERATES SHIFT PULSES TO THE I0D/STRT SHIFT REGISTER

CIRCUIT OPERATION

TOGGLE CONTROL LOGIC (SEE SHEET B10GH FOR TIMING DIAGRAM)

TRANSMIT - THE INITIALIZATION MICROINSTRUCTION IS ISSUED FIRST IN THE TRANSMIT SEQUENCE (XIDLECA), INITIALIZING THE CONTROL FLIP-FLOPS. TOGGLE NODE TT0G1 IS DRIVEN POSITIVE, HOLDING THE TOGGLE INPUTS TO THE I0D/STRT SHIFT REGISTER LOW, IN PREPARATION FOR THE PARALLEL LOAD TO FOLLOW. G0.DLY RESET IS THE CONTROLLING SIGNAL. AFTER THE I0S AND I0D ARE LOADED WITH THE CONTROL STATE, THE SUBCHANNEL CODE AND THE DATA, THE START CHANNEL MICROINSTRUCTION IS ISSUED. INPUT G0XPTO (MISCELLANEOUS DECODER CROSSPOINT MOSTCHO) SETS FLIP-FLOPS G0FF, WHICH IN TURN CAUSES THE EDGE TRIGGERED G0.DLY FLIP-FLOP TO SET ON THE TRAILING EDGE OF THE NEXT P3 CLOCK PHASE. G0.DLY1 GOING POSITIVE SATISFIES THE GATE CONTROLLING THE TOGGLE NODE TT0G1, DRIVING IT LOW CAUSING THE INITIAL TOGGLE TO TAKE PLACE, ACCOMPLISHING FINAL DATA REGISTRATION OF THE MESSAGE PRIOR TO OUTPULSING. A BUFFER FLIP-FLOP (SSDATA) IN THE BIPOLAR INTERFACE LOGIC (SHEET B10GF) HAS BEEN LOADED WITH THE FIRST BIT TO BE SENT AND THE REMAINDER OF THE MESSAGE IS NOW REGISTERED WITH IT. G0.DLY1 IS STROBBED BY P1 SETTING SENDSYNC ALLOWING GATE CLKSHFTO TO TAKE CONTROL OF THE TOGGLE NODE. CLKSHFTO, CLOCKED AT P3, WILL GENERATE A SERIES OF TOGGLES AT THE TRAILING EDGE OF P3. THE BIPOLAR PULSE IS FORMED ON FC201 (SEE SHEET B10GF). CLKSHFT CONTINUES TO GENERATE TOGGLES UNTIL THE TRANSMIT STATE IS ABANDONED.

RECEIVE - ONCE THE RECEIVE STATE IS ENTERED, IT ALLOWS THE I0C TO MONITOR THE INCOMING SERIAL BUS FOR A REPLY MESSAGE. INPUT LEAD SHFTO, SYCHRONIZED WITH THE INCOMING DATA, TAKES OVER CONTROL OF THE TOGGLE NET. THIS SHIFTING ACTION CONTINUES UNTIL A COMPLETE MESSAGE HAS BEEN RECEIVED, WITH THE START BIT OF THE INCOMING MESSAGE REGISTERED IN THE LEAST SIGNIFICANT BIT POSITION OF THE SHIFT REGISTER (I.E. ~~STRTO-1).~~ STRTO BEING SET IN THE RECEIVE STATE SETS THE ISHFT FLIP-FLOP, INHIBITING FURTHER TOGGLES PREVENTING OVERSHIFTING OF THE DATA. THE MESSAGE COMPLETE STATE IS NOW ENTERED.

PART 0F FS 10
C0MP0SITE DIAGRAM 5

3A CENTRAL CONTROL	SD-1C900-01-B10GE
BELL TELEPHONE LABORATORIES INCORPORATED	6S

ISSUE 3A

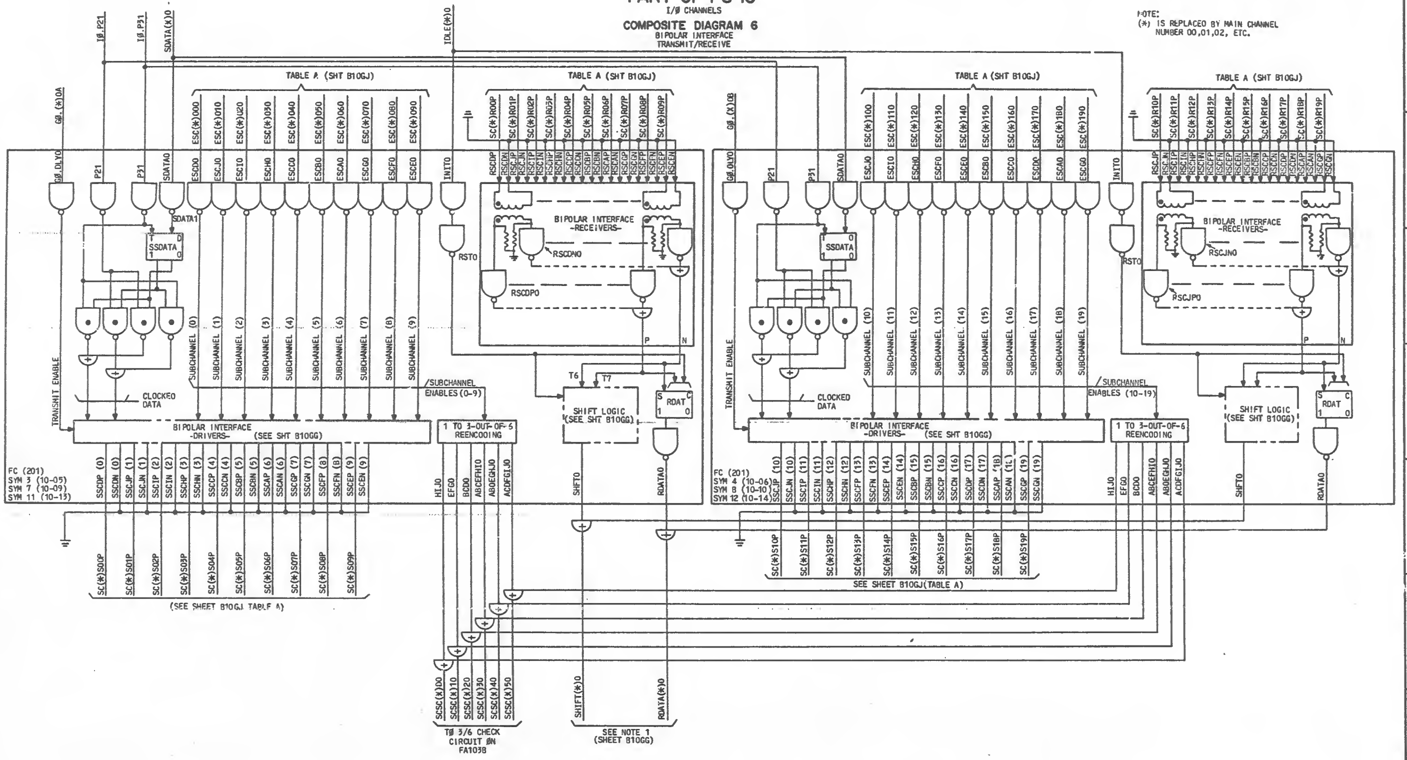
PART OF FS 10

I/Ø CHANNELS

COMPOSITE DIAGRAM 6

BIPOLAR INTERFACE
TRANSMIT/RECEIVE

NOTE:
(*) IS REPLACED BY MAIN CHANNEL
NUMBER 00,01,02, ETC.



PART ØF FS 10
CØMPØSITE DIAGRAM 6

ISSUE
5A

3A CENTRAL CONTROL

SD-1C900-01-B10GF

BELL TELEPHONE LABORATORIES
INCORPORATED

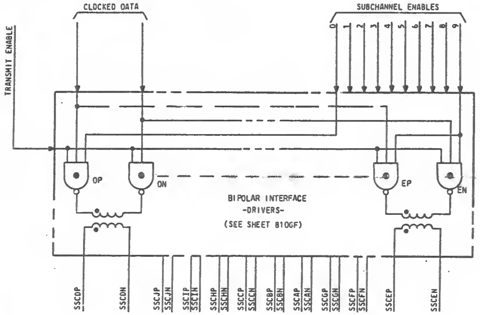
6S

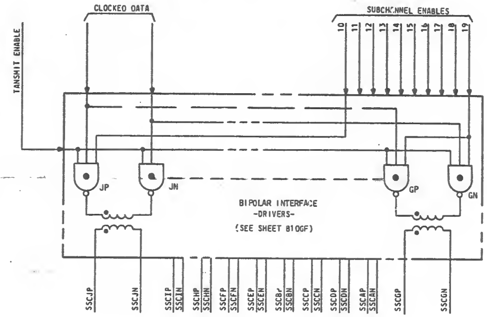
PART OF FS 10

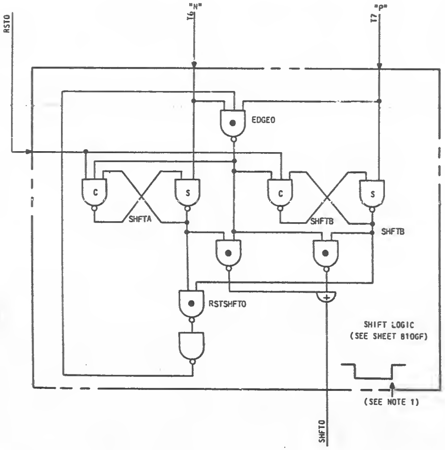
I/Ø CHANNELS

COMPOSITE DIAGRAM 7

BIPOLAR INTERFACE TRANSMIT/RECEIVE

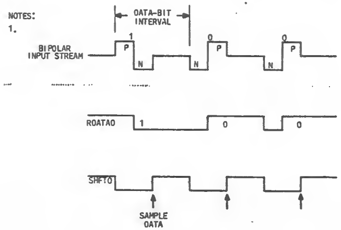






NOTES:

1.



CIRCUIT OPERATION

DRIVER CIRCUITRY

TO MINIMIZE THE TRANSMIT AND RECEIVE CIRCUITRY AND TO MAKE THE TRANSMISSION SCHEME INSENSITIVE TO THE TRANSMITTED DATA PATTERNS, TWO BIPOLAR PULSES ARE USED TO REPRESENT A SINGLE BIT OF DATA. EACH SERIAL BIT OF INFORMATION IS ENCODED INTO A DATA-BIT PAIR (SEE NOTE 1). THIS DATA-BIT PAIR CONSISTS OF TWO ADJACENT PULSES OF EQUAL AMPLITUDE BUT OF OPPOSITE POLARITY. PULSING THE TRANSMISSION LINE WITH TWO EQUAL AND OPPOSITE PULSES RESULTS IN MAINTAINING A ZERO VOLTAGE SHIFT IN THE GROUND REFERENCE LEVEL OVER THE LENGTH OF THE MAESAGE. EACH DATA-BIT, THEREFORE, PULSES AND FORCEFULLY RECOVERS THE LINE PRIOR TO THE NEXT DATA-BIT INTERVAL, REGARDLESS OF THE CHARACTERISTICS OF THE TRANSMISSION MEDIA.

TO FORM THE DATA-BIT PAIR, TWO HIGH FANOUT GATES ARE USED (OP,ON). THEIR TOTEM POLE OUTPUTS ARE CONNECTED IN A PUSH-PULL CONFIGURATION WITH THE PRIMARY OF THE DRIVER TRANSFORMER. THE SEQUENCE IN WHICH THESE DRIVER GATES ARE PULSED DETERMINES THE PHASE RELATIONSHIP, AND THEREFORE THE DATA CONTENT, OF THE DATA-BIT PAIR. (SEE SHEET B10GF)

THE DRIVER GATES ARE ENABLED BY INPUT GØ.OLYO WHICH IS ACTIVATED ON THE TRAILING EDGE OF CLOCK PHASE P3. FOUR DATA ENCODING GATES ARE DRIVEN FROM BUFFER FLIP-FLOP SSDATA, AND CLOCKED ACCORDINGLY BY P2 AND P3. THE NEXT DATA BIT TO BE TRANSMITTED IS STROBBED INTO THE BUFFER ON THE TRAILING EDGE OF P3 AND SENT DURING THE FOLLOWING P2/P3 INTERVAL.

RECEIVE CIRCUITRY

THE RECEIVER GATES RSCDPO AND RSCDNO ETC. (SEE SHEET B10GF) HAVE CLIPPING CIRCUITS ON THEIR INPUTS. THE BIPULAR PULSE IS PRESENTED TO BOTH INPUT GATES FROM THE SECONDARY OF THE TRANSFORMER 180° OUT OF PHASE WITH EACH OTHER. THE NEGATIVE PORTIONS OF EACH ARE REMOVED BY THE CLIPPING CIRCUITRY TO PREVENT THE GATE INPUTS FROM BEING DRIVEN BELOW GROUND. THE POSITIVE PORTIONS OF THE BIPOLAR WAVEFORMS THEN SEQUENTIALLY DRIVE THE RECEIVER GATES. THEIR ORDER REFLECTS THE DATA CONTENT OF THE BIPOLAR WAVEFORM. THESE GATES DRIVE DIRECTLY INTO THE RDAT FLIP-FLOP WHERE THE DATA CONTENT IS STORED. THE SHIFT LOGIC DETECTS THE PRESENCE OF THE DATA-BIT PAIR AND GENERATES A SHIFT PULSE (SHFTO) IN SYNCHRONISM (SEE NOTE 1) WITH THE RECONSTITUTED DATA (RDATA).

THE SHIFT PULSE, SHFTO, IS GENERATED BY THE SHFT FLIP-FLOPS AND ASSOCIATED GATES. THE QUIESCENT STATE OF THESE FLIP-FLOPS ARE RESET, WITH SHFTO POSITIVE (INACTIVE). THE FIRST LOBE OF A DATA-BIT PAIR ACTIVATES EITHER GATE RSCDPO OR RSCDNO DEPENDING ON ITS DATA CONTENT. ASSUME A "ONE" IS ENTERING, GATE RSCDPO RESPONDS TO THE FIRST LOBE OF THE DATA BIT PAIR SETTING THE SHFT "B" FLIP-FLOP, DRIVING THE SHFTO COLLECTOR TIE TO GROUND. THE SECOND LOBE DRIVES GATE RSCDNO SETTING THE SHFT "A" FLIP-FLOP. GATE RSTSHFTO ACTIVATES, REMOVING THE INHIBIT FROM GATE EDGEO. RSCDNO, STILL GROUND, PREVENTS EDGEO FROM ACTIVATING UNTIL THIS SECOND LOBE OF THE DATA-BIT PAIR IS PASSED. EDGEO, THEREFORE ACTIVATES ON THE TRAILING EDGE OF THE DATA-BIT PAIR. EDGEO RESETS BOTH SHFT FLIP-FLOPS AND ALSO CAUSES SHFTO TO PULSE POSITIVE WITHIN ONE GATE DELAY DUE TO EDGEO DIRECTLY INHIBITING THE SHIFT OUTPUT GATES. WITHOUT THIS INHIBIT CONNECTION IT WOULD REQUIRE THREE GATE DELAYS AFTER EDGEO ACTIVATES TO TURN OFF THE SHFTO PULSE. THIS LOW-TO-HIGH TRANSITION ON OUTPUT LEAD SHFTO CAUSES A DATA SHIFT IN THE IØD/STRT SHIFT REGISTER.

PART ØF FS 10
CØMPØSITE DIAGRAM 7

ISSUE
5A

3A CENTRAL CONTROL

SD-1C900-01-B10GG

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

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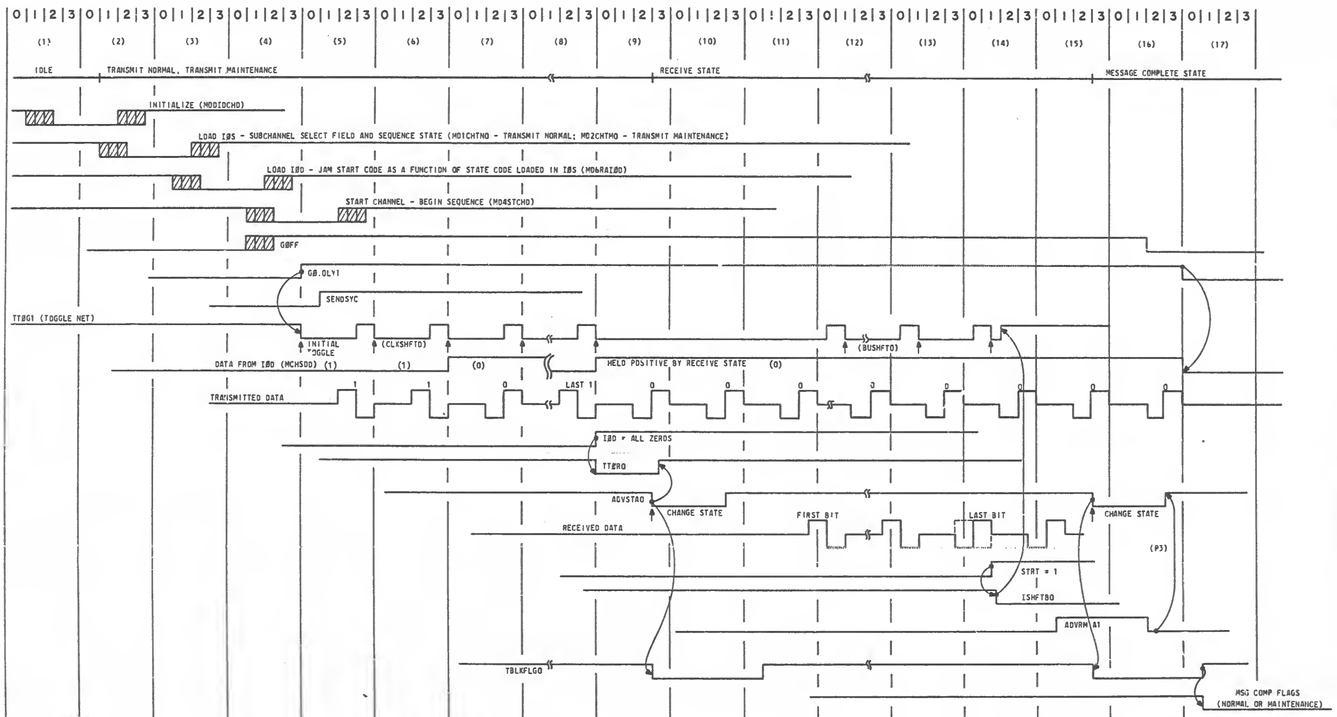
PART OF FS 10
I/O CHANNELS

COMPOSITE DIAGRAM 8
SERIAL I/O CHANNEL-TIMING DIAGRAM



PART OF FS 10
COMPOSITE DIAGRAM 8

ISSUE
3A

3A CENTRAL CONTROL

SD-1C900-01-B10GH

BELL TELEPHONE LABORATORIES
INCORPORATED

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PART OF FS 10

I/O CHANNELS

COMPOSITE DIAGRAM 9

BIPOLAR INTERFACE
TRANSMIT/RECEIVE

TABLE A

SERIAL I/O SUBCHANNEL ASSIGNMENTS

SUBCHANNEL SELECT		SUBCHANNEL ENABLES (GRD ACTIVE)				I/O TRANSMIT		I/O RECEIVE	
				FC201					
			FA1038 TERM NO.		TERM NO.	(OUTPUT PORT) TERM NO.		(INPUT PORT) TERM NO.	
SUB-CHANNEL	3-OUT-OF-6 CODE					P	N(GRD)	P	N(GRD)
0	000111	SYM(S) 1(10-03),5(10-07),9(10-11)	203	SYM(S) 3(10-05),7(10-9),11(10-13)	207	117	017	104	004
1	001011		007		209	114	014	103	003
2	001101		207		310	113	013	312	212
3	001110		008		211	112	012	102	002
4	010011		003		306	116	016	110	010
5	010101		202		208	115	015	109	009
6	010110		002		308	318	218	313	213
7	011001		206		105	111	011	101	001
8	011010		103		005	317	217	316	216
9	011100		004		008	118	018	201	301
10	100011		105	SYM(S) 4(10-06),8(10-10),12(10-14)	209	114	014	103	003
11	100101		304		310	113	013	312	212
12	100110		104		211	112	012	102	002
13	101001		106		005	317	217	316	216
14	101010		010		008	118	018	201	301
15	101100		306		208	115	015	109	009
16	110001		006		306	116	016	110	010
17	110010		210		207	117	017	104	004
18	110100		204		308	318	218	313	213
19	111000		303		105	111	011	101	001

TABLE B

MAIN CHANNEL	MCSCO	MCSBO	MCSAO
0	R9.120	R9.110	R9.100
1	R9.130	R9.110	R9.100
2	R9.130	R9.120	R9.100

CIRCUIT OPERATION

ERROR CIRCUITRY

TO OBTAIN SYSTEM RELIABILITY AND DEPENDABILITY, MAINTENANCE FEATURES WERE INTEGRATED INTO THE BASIC ORGANIZATION OF THE IOC. THE IOC PERFORMS THE FOLLOWING ERROR CHECKS:

(A) 3-OUT-OF-6 CODE CHECKS

(B) ILLEGAL START CODE DETECTION IN THE RECEIVED SERIAL MESSAGE.

3-OUT-OF-6 CODE CHECKS

THE MAINCHANNEL SELECT, THE SUBCHANNEL SELECT, AND THE SEQUENCER STATE CODES ARE ALL 3-OUT-OF-6 ENCODED. SELF-CHECKING 3-OUT-OF-6 CODE CHECK CIRCUITS ARE UTILIZED TO ENSURE THE CORRECT DECODING OF THESE FIELDS. EACH 6-BIT FIELD IS DECODED TO A UNIQUE OUTPUT (1-OUT-OF-20), WHICH PERFORMS AN ASSIGNED TASK. THIS SAME SINGLE OUTPUT IS THEN REENCODED TO PRODUCE AN ASSOCIATED 3-OUT-OF-6 CODE WHICH IS INPUTTED TO THE CHECK CIRCUITRY. THE CHECK CIRCUIT OPERATES ON THIS INPUT AND PROVIDES AN ERROR INDICATION WHENEVER THE INPUT IS NOT 3-OUT-OF-6, OR WHENEVER A FAULT OCCURS WITHIN THE CHECK CIRCUIT ITSELF. SINGLE FAULTS WITHIN THE DECODER CIRCUIT RESULT IN THE PRODUCTION OF EITHER A NO OUTPUT CONDITION OR A MULTIPLE OUTPUT CONDITION. THE SAME RESULT OCCURS WHEN THE CODE INPUTS PRESENTED TO THE DECODER CIRCUIT ARE NON 3-OUT-OF-6 CODES. IN EITHER CASE, UPON REENCDOING, NON 3-OUT-OF-6 CODES ARE PRODUCED AND DETECTED BY THE CHECK CIRCUIT. THIS 3-OUT-OF-6 CODE CHECK IS MADE AT THE DECODER OUTPUT TO INCLUDE THE FINAL DECODED OUTPUT STAGE IN THE CHECK SCHEME. THE RESULTING ERROR INDICATORS SET BITS IN THE ERROR REGISTER (ER) OF THE 3A CC WHICH IN TURN CAUSES PROGRAM INTERRUPTS. AN ERROR IN MAIN CHANNEL SELECTION SETS BIT 17 OF THE ER: SUBCHANNEL SELECTION ERRORS AND IOC SEQUENCE ERRORS SET BIT PL OF THE ER.

ILLEGAL START CODE DETECTION

UPON RECEPTION OF AN I/O RETURN MESSAGE, THE IOC CONTROLLER DECODES THE 3-BIT START CODE, RAISING EITHER THE NORMAL OR MAINTENANCE MESSAGE COMPLETE FLAG. IF START CODES OTHER THAN 011 (NORMAL) OR 101 (MAINTENANCE) ARE ENCOUNTERED, THE NORMAL FLAG IS RAISED TO THE PROCESSOR, AND UPON EXECUTION OF THE TIO INSTRUCTION, ALL 18 BITS (DATA PLUS PARITY) OF THE R11 BUS ARE FORCED TO ZERO (SEE SHEET B10GC). WHEN PARITY OF THE RETURNED MESSAGE IS CHECKED (ALSO BY THE TIO INSTRUCTION), A NONFATAL I/O PARITY ERROR WILL BE ENCOUNTERED, SETTING THE PROGRAM INTERRUPT. THE ACTION TAKEN BY THIS INTERRUPT IS USER-DEPENDENT.

PARITY CHECK

PARITY IS MAINTAINED OVER THE I/O MESSAGE AND IS CHECKED VIA THE NORMAL PARITY CHECK CIRCUITRY IN THE CC WHEN THE DATA FIELD IS GATED TO THE CC GATING BUS ALONG WITH THE CORRESPONDING PARITY BITS. THIS PARITY ERROR IS CLASSIFIED AS NONFATAL AND IS DIVERTED TO ERROR REGISTER BIT PH, RESULTING IN A PROGRAM INTERRUPT.

I/O MICROSEQUENCE

THE FOLLOWING SEQUENCE OF MICROINSTRUCTIONS IS NECESSARY IN ORDER TO SEND A MESSAGE VIA AN I/O CHANNEL TO A PERIPHERAL UNIT.

1. LOAD R9 WITH THE DESIRED MCS AND SCS AND, IF NECESSARY, THE 4-BIT CONTROL FIELD.
2. LOAD R10 WITH THE DATA TO BE TRANSMITTED.
3. EXECUTE A SEND I/O (SIO) [OR SEND MAINTENANCE I/O (SMIO)] MAIN MEMORY OPERATION CODE. THIS OPERATION CODE:
    - A. IDLES THE I/O CHANNEL DEFINED BY THE MCS FIELD IN R9 (BITS 15-10). (MD0IDCH)
    - B. LOADS THE IOS OF THE SELECTED MAIN CHANNEL (BITS 11-6) WITH THE SCS CODE FROM (BITS 9-4) AND JAMS THE PROPER TRANSMIT CONTROL STATE INTO IOS BITS (5-0). (MD1CHTN/MD2CHTM)
    - C. LOADS THE DATA TO BE TRANSMITTED FROM R10 INTO THE IOD OF THE SELECTED MAIN CHANNEL (MD6RAI0)
    - D. LOADS R11 FROM THE IOD OF THE SELECTED MAIN CHANNEL. PERFORMS A MATCH BETWEEN R10 AND R11 VERIFYING THE GATING PATHS INTO AND OUT OF THE SELECTED IOD PRIOR TO TRANSMISSION. (I0DXR11)
    - E. OPERATES THE START CROSSPOINT (THE SIGNAL TO THE IOC SEQUENCER TO BEGIN TRANSMISSION). (MD4STCH)

CIRCUIT OPERATION (CONT)

AT THIS POINT THE IOC SEQUENCER IS ENABLED AND PERFORMS THE TRANSMIT/RECEIVE FUNCTION UNATTENDED. UPON RECEIVING THE RETURN MESSAGE, THE IOC SETS THE APPROPRIATE FLAGS AND PASSES CONTROL TO THE 3A CC. AFTER A SUFFICIENT TIME INTERVAL, DETERMINED BY THE RESPONSE TIMES OF THE PARTICULAR PERIPHERAL UNIT, THE 3A CC MUST INTERROGATE THE ACTIVE CHANNELS LOOKING FOR MESSAGE COMPLETE FLAGS.

4. EXECUTE A TEST I/O (TIO) [OR TEST MAINTENANCE I/O (TMIO)] OPERATION CODE. THIS OPERATION CODE LOOKS FOR THE NORMAL (OR MAINTENANCE) MESSAGE COMPLETE FLAG OF THE MAIN CHANNEL SPECIFIED BY THE MCS FIELD OF R9.
    - A. IF THE FLAG IS PRESENT, THE PROCESSOR SETS THE CONDITION FLIP-FLOP (CF) EQUAL TO 1, GATES THE IOD TO R11, PERFORMS A PARITY CHECK ON THE MESSAGE, AND INITIALIZES THE MAIN CHANNEL. (THE CF IS A DECISION BIT IN THE CC MICROPROGRAM CONTROL).
    - B. IF THE FLAG IS NOT PRESENT, SET CF EQUAL TO 0 AND LEAVE R11 AND THE MAIN CHANNEL UNCHANGED.

PART OF FS 10
COMPOSITE DIAGRAM 9

ISSUE
5A

3A CENTRAL CONTROL

SD-1C900-01-B10GJ

BELL TELEPHONE LABORATORIES
INCORPORATED

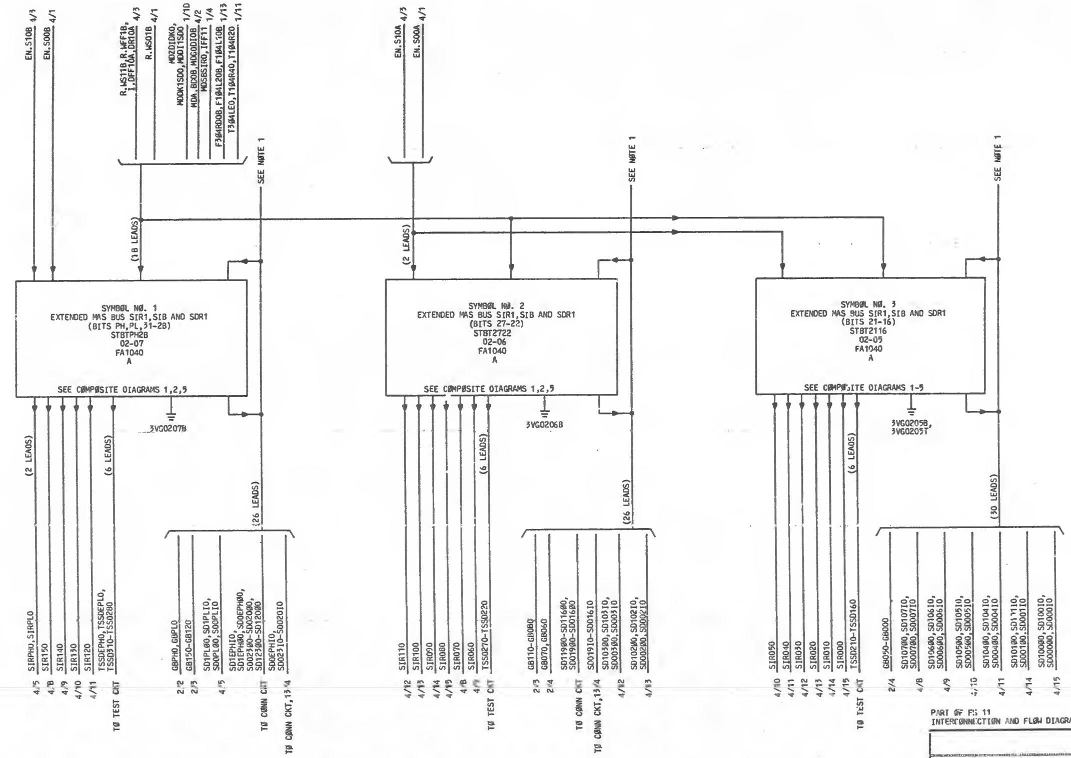
6S

PART OF FS 11

EXTENDED MAIN MEMORY INTERFACE
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS SHOWN COULD FUNCTION AS EITHER OUTPUTS OR INPUTS (OI). ALL OFF-PAGE REFERENCING WILL BE SHOWN ON OUTPUT LEAD.
2. FOR TO- AND FROM-FIELD DECODING ASSIGNMENTS SEE NOTE 312.


EN.S10B 4/3
EN.S00B 4/1
R.WS11B,R.WFF1B,I,DFF10A,DR10A 4/3
R.WS01B 4/1
MDZDIDK0,MDDK1SD0,MDDI1SD0 1/1D
MDA,BD0B,MDGODI0B 4/2
MDSBSIR0,IFF11 1/4
F304RD0B,F104L20B,F104L10B 1/13
T304LE0,T104R40,T104R20 1/11
SEE NOTE 1
(18 LEADS)
SYMBOL NO. 1
EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS PH,PL,31-28)
STBTPH28
02-07
FA1040
A
SEE COMPOSITE DIAGRAMS 1,2,5
3VG02078
(2 LEADS)
(6 LEADS)
(26 LEADS)
SIRPH0,SIRPL0 4/5
SIR150 4/8
SIR140 4/9
SIR130 4/10
SIR120 4/11
TSSDEPH0,TSSDEPL0,TSSD310-TSSD280 TO TEST CKT
GBPH0,GBPL0 2/2
GB150-GB120 2/3
SD1PL00,SD1PLI0,SD0PL00,SD0PLI0 4/5
SD1EPHI0,SD1EPH00,SD0EPH00,SD02300-SD02000,SD12300-SD12000 TO CONN CKT
SD0EPHI0,SD02310-SD02010 TO CONN CKT,13/4
EN.S10A 4/3
EN.S00A 4/1
SEE NOTE 1
(2 LEADS)
SYMBOL NO. 2
EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS 27-22)
STBT2722
02-06
FA1040
A
SEE COMPOSITE DIAGRAMS 1,2,5
3VG02068
(6 LEADS)
(26 LEADS)
SIR110 4/12
SIR100 4/13
SIR090 4/14
SIR080 4/15
SIR070 4/8
SIR060 4/9
TSSD270-TSSD220 TO TEST CKT
GB110-GB080 2/3
GB070,GB060 2/4
SD11900-SD11600,SD01900-SD01600 TO CONN CKT
SD01910-SD01610 TO CONN CKT,13/4
SD10300,SD10310,SD00300,SD00310 4/12
SD10200,SD10210,SD00200,SD00210 4/13
SEE NOTE 1
SYMBOL NO. 3
EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS 21-16)
STBT2116
02-05
FA1040
A
SEE COMPOSITE DIAGRAMS 1-5
3VG02058,
3VG0205T
(6 LEADS)
(30 LEADS)
SIR050 4/10
SIR040 4/11
SIR030 4/12
SIR020 4/13
SIR010 4/14
SIR000 4/15
TSSD210-TSSD160 TO TEST CKT
GB050-GB000 2/4
SD10700,SD10710,SD00700,SD00710 4/8
SD10600,SD10610,SD00600,SD00610 4/9
SD10500,SD10510,SD00500,SD00510 4/10
SD10400,SD10410,SD00400,SD00410 4/11
SD10100,SD10110,SD00100,SD00110 4/14
SD10000,SD10010,SD00000,SD00010 4/15

PART OF FS 11
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES | SD-1C900-01 | B11AA

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PART OF FS 11

EXTENDED MAIN MEMORY INTERFACE

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
DR10A	DATA READY FLIP-FLOP (COPY 1)
EN.SD0(A,B)	ENABLE MY STORE
EN.S10(A,B)	ENABLE OTHER STORE
GBPH0	PARITY HIGH OF THE GATING BUS
GBPLD	PARITY LOW OF THE GATING BUS
GB000-GB150	BITS 0-15 OF THE GATING BUS
I.OFF10A	OUTPUT OF THE INSTRUCTION OR DATA FLIP-FLOP (COPY 1)
IFF11	I FLIP-FLOP (COPY 1)
MDA.BD0B	ENABLE GATING OF THE BAD DATA AND THE ADDRESS OF A DOUBLE STORE READ OPERATION TO THE DK AND AK REGISTERS RESPECTIVELY
MDOI1SDO	MISC. DECODER, GATE OI1 INTO THE SDR
MODK1SDO	MISC. DECODER, GATE OK1 INTO THE SDR
MDGDDI0B	ENABLE GATING OF THE GOOD DATA OF THE DOUBLE STORE READ OPERATION TO THE OI REGISTER
MDSBSIRO	MISC. DECODER, GATE SIB TO SIR1
MDZOIDKO	MISC. DECODER, CLEAR THE DI1 AND OK1 REGISTERS
R.WFF1B	READ/WRITE FLIP-FLOP (COPY 1)
R.WS01B	READ OR WRITE FUNCTION FOR MAIN STORE 0 (DEFINED BY SC300)
R.WS11B	READ OR WRITE FUNCTION OF MAIN STORE 1 (DEFINED BY SC310)
SD0EPHID	MY MAIN STORE DATA BUS EXTENDED PARITY HIGH INPUT
SD0EPH00	MY MAIN STORE DATA BUS EXTENDED PARITY HIGH OUTPUT
SD0PLI0	MY MAIN STORE DATA BUS PARITY LOW INPUT (FUSED)
SD0PL00	MY MAIN STORE DATA BUS PARITY LOW OUTPUT
SD000I0-S00071I0	MY MAIN STORE DATA BUS INPUT LEADS 0-7 (FUSED)
SD016ID-SD0231D	MY MAIN STORE DATA BUS INPUT LEADS 16-23 (FUSED)
SD00000-SD00700	MY MAIN STORE DATA BUS OUTPUT LEADS 0-7
S001600-SD02300	MY MAIN STORE DATA BUS OUTPUT LEADS 16-23
SO1EPHI0	OTHER MAIN STORE DATA BUS EXTENDED PARITY HIGH INPUT
SO1EPH00	OTHER MAIN STORE DATA BUS EXTENDED PARITY HIGH OUTPUTS
SO1PLI0	OTHER MAIN STORE DATA BUS PARITY LOW INPUT
SD1PL00	OTHER MAIN STORE DATA BUS PARITY HIGH INPUT
SD100I0-SD10710	OTHER MAIN STORE DATA BUS INPUT LEADS 0-15
S01161O-SD12310	OTHER MAIN STORE DATA BUS INPUT LEADS 16-23
S010000-SD10700	OTHER MAIN STORE DATA BUS OUTPUT LEADS 0-15

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SD11600-SD12300	OTHER MAIN STORE DATA BUS OUTPUT LEADS 16-23
SIRPH0	PARITY HIGH OF SIR'S (SIR0 IF IFF=0, SIR1 IF IFF=1)
SIRPLD	PARITY LOW OF SIR'S (SIR0 IF IFF=0, SIR1 IF IFF=1)
SIR000-SIR150	BITS 0-15 OF THE SIRS (SIR0 IF IFF=0, SIR1 IF IFF=1)
TSS0EPH0	TEST SET ACCESS, EXTENDED PARITY HIGH ON THE STORE DATA BUS
TSSDEPL0	TEST SET ACCESS, EXTENDED PARITY LOW ON THE STORE DATA BUS
TSSD16D-TSS0310	TEST SET ACCESS, BITS 16-31 ON THE STORE DATA BUS

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 4A
BELL LABORATORIES	SD-1C900-01	B11AB

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PART OF FS 11

EXTENDED MAIN MEMORY INTERFACE

SYMBOL NO. 1

EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS PH,PL,31-28)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBTPH28	02-07	FA1040	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		009			DISWR1X0	11A1
		012			DISWR1Y0	10A1
		103			DISWR0Y0	7A1
		107			DISWR0X0	8A1
		109			DISWB820	6A3
DR10A	I	011	4/3		DRI0	5A2
EN.S00B	I	010	4/1		REQS0I0	5A4
EN.S10B	I	110	4/3		REQS1I0	5A4
F1D4L10B	I	114	1/13		F1D4L10	3A0
F1D4L20B	I	015	1/13		F1D4L20	2A0
F3D4RD0B	I	307	1/13		F3D4RD0	2A1
GBPH0	DI	205	2/2		GB.ZBS10	3H2
GBPL0	DI	005	2/2		GB.ZAS10	3H3
GB120	DI	303	2/3		GB.XAS10	3H6
GB130	DI	004	2/3		GB.XBS10	3H5
GB140	DI	104	2/3		GB.YAS10	3H5
GB150	DI	304	2/3		GB.YBS10	3H3
I.DFF10A	I	211	4/3		I.DFFI0	5A2
IFF11	I	214	1/4		IFF1	3A7
MDA.BD0B	I	100	4/2		SDB.DK10	12A1
MDDI1SD0	I	206	1/10		DI1.SDR0	13A1
MDDK1SD0	I	106	1/10		DK1.SDR0	12A1
MDGDDI0B	I	001	4/2		SDG.DI10	13A1
MDSBSIR0	I	314	1/4		GSIBSIR0	3A1
MDZDIDK0	I	300	1/10		CLDIDK0	12A2
R.WFF1B	I	204	4/3		R.WFFI1	5A1
R.WS01B	I	210	4/1		R.WS0I1	5A3
R.WS11B	I	310	4/3		R.WS1I1	5A4
SD0EPHI0	DI	302	13/4 TO CONN CKT		SD02BR0	6H4
SD0EPH00	DI	209	TO CONN CKT		TSD02BW0	6H3
SD0PLI0	DI	208	4/		SD0ZAR0	6H7
SD0PLD0	DI	108	4		TSD0ZAW0	6H6
SD02010	DI	006	13/4 TO CONN CKT		SD0XAR0	8H5
SD020D0	DI	007	TO CONN CKT		TSD0XAW0	8H4
SD02110	DI	008	13/4 TO CONN CKT		SD0XBR0	8H2
SD021D0	DI	207	TO CONN CKT		TSD0XBW0	8H1
SD02210	DI	003	13/4 TO CONN CKT		SD0YAR0	7H5
SD02200	DI	203	TO CONN CKT		TSD0YAW0	7H4
SD02310	DI	105	13/4 TO CONN CKT		SD0YBR0	7H2
SD023D0	DI	305	TO CONN CKT		TSD0YBW0	7H1
SD1EPHI0	DI	212	TO CONN CKT		SD12BR0	9H4
SD1EPH00	DI	112	TO CONN CKT		TSD12BW0	9H3
SD1PLI0	DI	115	4/5		SD1ZAR0	9H7
SD1PLD0	DI	315	4/5		TSD1ZAW0	9H6
SD12010		313			SD1XAR0	11H5
SD12000	DI	014	TO CONN CKT		TSD1XAW0	11H4
SD12110		102			SD1XBR0	11H2
SD12100	DI	308	TO CONN CKT		TSD1XBW0	11H1
SD12210		312			SD1YAR0	10H5
SD122D0	DI	013	TO CONN CKT		TSD1YAW0	10H4
SD12310		213			SD1YBR0	10H2
SD123D0	DI	113	TO CONN CKT		TSD1YBW0	10H1
SIRPH0	D	016	4/5	202	SIR1.ZB0	3H2
SIRPL0	D	216	4/5	202	SIR1.ZA0	3H2

SYMBOL NO. 1 (CONT)

EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS PH,PL,31-28)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBTPH28	02-07	FA1040	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SIR120	D	217	4/11	202	SIR1.XA0	3H6
SIR130	D	017	4/10	202	SIR1.XB0	3H6
SIR140	D	316	4/9	202	SIR1.YA0	3H4
SIR150	D	116	4/8	202	SIR1.YB0	3H4
TSSDEPH0	D	117			SD02B0	6H4
TSSDEPL0	D	317			SD0ZA0	6H6
TSSD280	D	201			SD0XA0	8H5
TSSD290	D	306			SD0XB0	8H2
TSSD300	D	202			SD0YA0	7H5
TSSD310	D	002			SD0YB0	7H2
T1D4R20	I	311	1/11		T1D4R20	4A0
T1D4R40	I	215	1/11		T1D4R40	2A1
T3D4LE0	I	111	1/11		T3D4LE0	4A1
3T058E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0207B	I	309			DISWBA20	9A5
	GRD	200			GRD	
3V058E	PWR	000		203	+3	
	PWR	119		203	+3	

SYMBOL NO. 2

EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS 27-22)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT2722	02-06	FA1040	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		012			DISWR1Y0	10A1
		103			DISWR0Y0	7A1
		109			DISWB820	6A3
		309			DISWBA20	9A5
DR10A	I	011	4/3		DRI0	5A2
EN.S00A	I	010	4/1		REQS0I0	5A4
EN.S10A	I	110	4/3		REQS1I0	5A4
F1D4L10B	I	114	1/13		F1D4L10	3A0
F1D4L20B	I	015	1/13		F1D4L20	2A0
F3D4RD0B	I	307	1/13		F3D4RD0	2A1
GB060	DI	303	2/4		GB.XAS10	3H6
GB070	DI	004	2/4		GB.XBS10	3H5
GB080	DI	104	2/3		GB.YAS10	3H5
GB090	DI	304	2/3		GB.YBS10	3H3
GB100	DI	005	2/3		GB.ZAS10	3H3
GB110	DI	205	2/3		GB.ZBS10	3H2
I.DFF10A	I	211	4/3		I.DFFI0	5A2
IFF11	I	214	1/4		IFF1	3A7
MDA.BD0B	I	100	4/2		SDB.DK10	12A1
MDDI1SD0	I	206	1/10		DI1.SDR0	13A1
MDDK1SD0	I	106	1/10		DK1.SDR0	12A1
MDGDDI0B	I	001	4/2		SDG.DI10	13A1
MDSBSIRD	I	314	1/4		GSIBSIR0	3A1
MDZDIDK0	I	300	1/10		CLDIDK0	12A2

SYMBOL NO. 2 (CONT)

EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS 27-22)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
STBT2722	02-06	FA1040	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
R.WFF1B	I	204	4/3		R.WFFI1	5A1
R.WS01B	I	210	4/1		R.WS0I1	5A3
R.WS11B	I	310	4/3		R.WS1I1	5A4
SD00210	DI	006	4/13		SD0XAR0	8H5
SD00200	DI	007	4/13		TSD0XAW0	8H4
SD00310	DI	008	4/12		SD0XBR0	8H2
SD00300	DI	207	4/12		TSD0XBW0	8H1
SD01610	DI	003	13/4 TO CONN CKT		SD0YAR0	7H5
SD016D0	DI	203	TO CONN CKT		TSD0YAW0	7H4
SD01710	DI	105	13/4 TO CONN CKT		SD0YBR0	7H2
SD01700	DI	305	TO CONN CKT		TSD0YBW0	7H1
SD01810	DI	208	13/4 TO CONN CKT		SD0ZAR0	6H7
SD018D0	DI	108	TO CONN CKT		TSD0ZAW0	6H6
SD01910	DI	302	13/4 TO CONN CKT		SD02BR0	6H4
SD01900	DI	209	TO CONN CKT		TSD02BW0	6H3
SD10210	DI	313	4/13		SD1XAR0	11H5
SD10200	DI	014	4/13		TSD1XAW0	11H4
SD10310	DI	102	4/12		SD1XBR0	11H2
SD103D0	DI	308	4/12		TSD1XBW0	11H1
SD11610		312			SD1YAR0	10H5
SD11600	DI	013	TO CONN CKT		TSD1YAW0	10H4
SD11710		213			SD1YBR0	10H2
SD117D0	DI	113	TO CONN CKT		TSD1YBW0	10H1
SD11810		115			SD12AR0	9H7
SD118D0	DI	315	TO CONN CKT		TSD1ZAW0	9H6
SD11910		212			SD12BR0	9H4
SD119D0	DI	112	TO CONN CKT		TSD12BW0	9H3
SIR060	D	217	4/9	202	SIR1.XA0	3H6
SIR070	D	017	4/8	202	SIR1.XB0	3H6
SIR080	D	316	4/15	202	SIR1.YA0	3H4
SIR090	D	116	4/14	202	SIR1.YB0	3H4
SIR100	D	216	4/13	202	SIR1.ZA0	3H2
SIR110	D	016	4/12	202	SIR1.Z30	3H2
TSSD220	D	201			SD0XA0	8H5
TSSD230	D	306			SD0XB0	8H2
TSSD240	D	202			SD0YA0	7H5
TSSD250	D	002			SD0YB0	7H2
TSSD260	D	317			SD0ZA0	6H6
TSSD270	D	117			SD02B0	6H4
T1D4R20	I	311	1/11		T1D4R20	4A0
T1D4R40	I	215	1/11		T1D4R40	2A1
T3D4LE0	I	111	1/11		T3D4LE0	4A1
3T058E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0206B	I	009			DISWR1X0	11A1
	I	107			DISWR0X0	8A1
	GRD	200			GRD	
3V058E	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 11
SYMBOL(S) 1 2

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01		B11CA

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PART OF FS 11

EXTENDED MAIN MEMORY INTERFACE

SYMBOL NO. 3

EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS 21-16)

DESIG	EOPT LOC	CODE	ELEM IDENT	OPT
STBT2116	02-05	FA1040	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
DR10A	I	011	4/3		OR10	5A2
EN.S00A	I	010	4/1		REDS010	5A4
EN.S10A	I	110	4/3		REDS110	5A4
F104L10B	I	114	1/13		F104L10	3A0
F104L20B	I	015	1/13		F104L20	2A0
F3D4RD0B	I	307	1/13		F3O4R00	2A1
GB000	OI	303	2/4		GB.XAS10	3H6
GB010	DI	004	2/4		GB.XBS10	3H5
GB020	OI	104	2/4		GB.YAS10	3H5
GB030	OI	304	2/4		GB.YBS10	3H3
GB040	OI	005	2/4		GB.ZAS10	3H3
GB050	OI	205	2/4		GB.ZBS10	3H2
I.OFF10A	I	211	4/3		I.OFFI0	5A2
IFF11	I	214	1/4		IFF1	3A7
MDA.BD0B	I	100	4/2		SDB.DK10	12A1
MDDI1SD0	I	206	1/10		OI1.SDR0	13A1
MDDK1SD0	I	106	1/10		OK1.SDR0	12A1
MDGD0I0B	I	001	4/2		SDG.DI10	13A1
MDSBSIR0	I	314	1/4		GSIBSIR0	3A1
MD2DIDK0	I	300	1/10		CLDIDK0	12A2
R.WFF1B	I	204	4/3		R.WFFI1	5A1
R.WS01B	I	210	4/1		R.WS0I1	5A3
R.WS11B	I	310	4/3		R.WS1I1	5A4
SD000I0	OI	208	4/15		SD0ZAR0	6H7
S0000D0	DI	108	4/15		TS0OZAW0	6H6
S0001I0	OI	302	4/14		SD0ZBR0	6H4
S0001D0	OI	209	4/14		TSD0ZBW0	6H3
SD004I0	OI	006	4/11		SD0XAR0	8H5
SD004D0	OI	007	4/11		TS00XAW0	8H4
SD005I0	OI	008	4/10		S00XBR0	8H2
S0005D0	DI	207	4/10		TSD0XBW0	8H1
S0006I0	OI	003	4/9		SD0YAR0	7H5
SD006D0	DI	203	4/9		TSD0YAW0	7H4
SD007I0	DI	105	4/8		S00YBR0	7H2
SD00700	OI	305	4/8		TSD0YBW0	7H1
SD100I0	OI	115	4/15		SD1ZAR0	9H7
SD10000	OI	315	4/15		TSD1ZAW0	9H6
SD101I0	DI	212	4/14		SD1ZBR0	9H4
SD10100	OI	112	4/14		TSD1ZBW0	9H3
SD104I0	OI	313	4/11		SD1XAR0	11H5
SD104D0	DI	014	4/11		[illegible]1XAW0	11H4
SD105I0	OI	102	4/10		S[illegible].XBR0	11H2
SD105D0	OI	308	4/10		TSD1XBW0	11H1
SD106I0	DI	312	4/9		SD1YAR0	10H5
SD106D0	DI	013	4/9		TSD1YAW0	10H4
SD107I0	DI	213	4/8		SD1YBR0	10H2
SD10700	DI	113	4/8		TSD1YBW0	10H1
SIR000	O	217	4/15	202	SIR1.XA0	3H6
SIR010	O	017	4/14	202	SIR1.XB0	3H6
SIR020	O	316	4/13	202	SIR1.YA0	3H4
SIR030	D	116	4/12	202	SIR1.YB0	3H4
SIR040	O	216	4/11	202	SIR1.ZA0	3H2
SIR050	O	016	4/10	202	SIR1.ZB0	3H2
TSSD160	O	201			SD0XA0	8H5
TSS0170	O	306			SD0XB0	8H2
TSSD180	O	202			SD0YA0	7H5
TSSD190	O	002			SD0YB0	7H2
TSSD200	O	317			SD0ZA0	6H6
TSSD210	D	117			SD0ZB0	6H4
T1D4R20	I	311	1/11		T1D4R20	4A0

SYMBOL NO. 3 (CONT)

EXTENDED MAS BUS SIR1,SIB AND SDR1
(BITS 21-16)

DESIG	EDPT LOC	CODE	ELEM IDENT	OPT
STBT2116	02-05	FA1040	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
T104R40	I	215	1/11		T104R40	2A1
T3D4LE0	I	111	1/11		T3D4LE0	4A1
3T058E	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0205B	I	009			DISWR1X0	11A1
	I	103			DISWR0Y0	7A1
	I	107			DISWR0X0	8A1
	I	109			DISWBB20	6A3
	I	309			DISWBAZ0	9A5
	GRD	200			GRD	
3VG0205T	I	012			DISWR1Y0	10A1
	GRD	319			GRD	
3V058E	PWR	000		203	+3	
	PWR	119		203	+3	

PART OF FS 11
SYMBOL(S) 3

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 5A
BELL LABORATORIES	SD-1C900-01		B11CB

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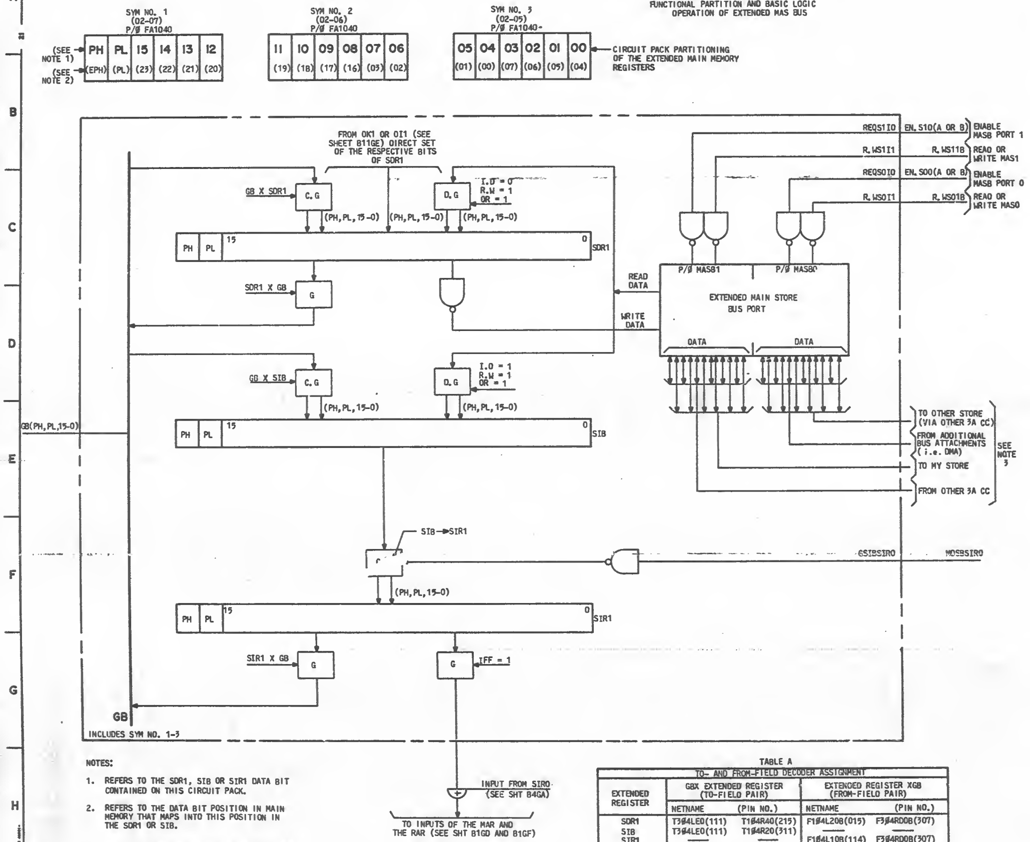
PART OF FS II

EXTENDED MAIN MEMORY INTERFACE

COMPOSITE DIAGRAM I

FUNCTIONAL PARTITION AND BASIC LOGIC
OPERATION OF EXTENDED MAS BUS



NOTES:

1. REFERS TO THE SDR1, SIB OR SIR1 DATA BIT CONTAINED ON THIS CIRCUIT PACK.
2. REFERS TO THE DATA BIT POSITION IN MAIN MEMORY THAT MAPS INTO THIS POSITION IN THE SDR1 OR SIB.
3. SEE SHT B11GB FOR MAPPING BETWEEN EXTENDED MAIN STORE DATA BITS INTO 3A CC DATA BITS.

TABLE A

TO- AND FROM-FIELD DECODER ASSIGNMENT

EXTENDED REGISTER	GBX EXTENDED REGISTER (TO-FIELD PAIR)		EXTENDED REGISTER XGB (FROM-FIELD PAIR)	
	NETNAME	(PIN NO.)	NETNAME	(PIN NO.)
SDR1	T304LE0(111)	T104R40(215)	F104L20B(015)	F304RD0B(307)
SIB	T304LE0(111)	T104R20(311)	—	—
SIR1	—	—	F104L10B(114)	F304RD0B(307)

CIRCUIT OPERATION

FS 11 PROVIDES THE CAPABILITY OF EXTENDING THE WIDTH OF THE MAIN STORE BUS (MASB). THE EXTENDED MASB INTERFACE IS USED FOR THE 2B ESS APPLICATION TO PROVIDE THE ABILITY TO INTERFACE TO A 26-BIT MEMORY WITH 24 DATA BITS AND TWO PARITY BITS THIS IS COMPARED TO THE NORMAL 16 DATA BITS AND 2 PARITY BITS. THE INTERFACE WITHIN THE 3A CC PROVIDES AN EXPANSION OF 18 ADDITIONAL BIT POSITIONS (16 DATA AND TWO PARITY FOR THIS INTERFACE). BY ADDING AN 18-BIT (INSTEAD OF AN 8-BIT) INTERFACE, THE IMPLEMENTATION IS MADE MORE REGULAR. HENCE, IT IS MUCH MORE COMPATIBLE WITH THE OPERATION OF THE MICROCODE AS WELL AS PROVIDING THE FLEXIBILITY, IF REQUIRED IN THE FUTURE, TO INTERFACE TO A 36-BIT MEMORY (32 DATA BITS AND FOUR PARITY BITS). IF THE EXTENDED MASB INTERFACE IS USED, THREE OPTIONALLY PROVIDED CIRCUIT PACKS MUST BE PLACED IN THE INDICATED CIRCUIT PACK POSITIONS.

THE OPERATION OF THE EXTENDED MASB CAN BE VIEWED AS EXTENSIONS TO THE NORMAL MEMORY INTERFACE REGISTERS AS DESCRIBED IN FS 4. THEREFORE, WHEN DATA IS ACCESSED FROM THE MAS, THE DATA IS PLACED INTO SDR0 AS WELL AS SDR1. WHEN INSTRUCTIONS ARE ACCESSED FROM THE MAS, THEY ARE PLACED IN THE SIB. THE PURPOSE OF THE SIB REGISTER IS TO IMPROVE THE EFFICIENCY OF MAS OPERATIONS WHEN USING THE EXTENDED MASB INTERFACE FOR THE EMULATION OF THE NO. 2 ESS HALF-WORD COMMAND STRUCTURE. FOR EXAMPLE, WHEN AN INSTRUCTION IS LOADED INTO THE SIR0 AND THE SIB REGISTER, THE FIRST HALF OF A DOUBLE-WORD INSTRUCTION IS EXECUTED AND THIS FIRST HALF COMES FROM THE SIR0 REGISTER. BY GATING THE SIB REGISTER TO SIR1 WHEN THIS FIRST HALF-WORD INSTRUCTION IS INITIATED (i.e. GATED FROM SIR0) THE PROCESSOR BUS CONTROLLER (PBC) IS FREE TO ISSUE THE NEXT MAS REQUEST FOR AN INSTRUCTION READ SINCE BOTH THE SIR0 REGISTER AND THE SIB ARE AVAILABLE.

THE OPERATION OF THE EXTENDED MASB PORT AND SDR1 AND SIB IN TERMS OF THEIR INTERFACE TO THE MAIN STORE BUS ARE EXACTLY AS DESCRIBED FOR FS 4. . THE ONE EXCEPTION IS THAT WHEN SDR1 IS GATED INTO, THE PBC IS NOT PUT INTO THE WRITE STATE. THE CONTROL TO LOAD THE SIB REGISTER INTO SIR1 ORIGINATES FROM THE MICRO-CONTROL VIA THE LOAD NEW OP CODE (LNØP) FUNCTION AND THE FACT THAT THE IFF=0 AS DESCRIBED ON SHEET B1GH. THIS MODIFIED LNØP (i.e. CONDITIONED ON IFF=0) CONTROL OR'ES ONTO THE NET MOSBSIRO IN COMPOSITE DIAGRAM 1. THE TWO SIR'S, SIR0 AND SIR1, OR TOGETHER ON A BIT-BY-BIT BASIS. THEREFORE, AS DESCRIBED IN FS 1, WHEN THE LNØP FUNCTION FIRES, THE SIR THAT IS USED AS THE SOURCE OF INSTRUCTION IS DETERMINED BY THE I FLIP-FLOP: THAT IS, IF THE I FLIP-FLOP IS IN THE 0 STATE SIR0 IS USED, AND IF THE I FLIP-FLOP IS IN THE 1 STATE SIR1 IS USED. EACH TIME A LNØP FUNCTION OCCURS IT TOGGLES THE I BIT SO THAT ALTERNATE HALF-WORD INSTRUCTIONS COME FROM THE ALTERNATE COPIES OF THE SIR REGISTER. NOTE THAT THIS ALSO MEANS THAT IN THE NO. 2 COMMAND STRUCTURE, IF A FULL-WORD COMMAND OCCURS SUCH THAT THERE IS AN OPCODE IN SIR0 AND 16 BITS OF DATA IN SIR1, IT IS NECESSARY FOR THE MICROCODE TO TOGGLE THE I FLIP-FLOP BACK INTO THE 0 STATE BEFORE THE NEXT INSTRUCTION IS EXECUTED.

THE ABILITY TO GATE THE SDR1 REGISTER TO AND FROM THE GB IS PROVIDED. HOWEVER, FOR THE SIB REGISTER, CONTROL IS ONLY PROVIDED TO GATE INTO IT FROM THE GB, AND FOR THE SIR1 REGISTER, CONTROL IS ONLY PROVIDED TO GATE OUT OF IT TO THE GB. TO PROVIDE THE NEEDED MAINTENANCE ACCESS, THE ABILITY TO GATE THE SIR0 TO THE SIR1 REGISTER IS PROVIDED BY A MISCELLANEOUS DECODER CROSSPOINT THAT INPUTS ON THE NETNAME MOSBSIRO. NOTE THAT THIS IS THE SAME INPUT FOR THE MODIFIED LNOP FUNCTION THAT LOADS THE SIB TO THE SIR1 REGISTER.

PART OF FS 11
COMPOSITE DIAGRAM 1

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

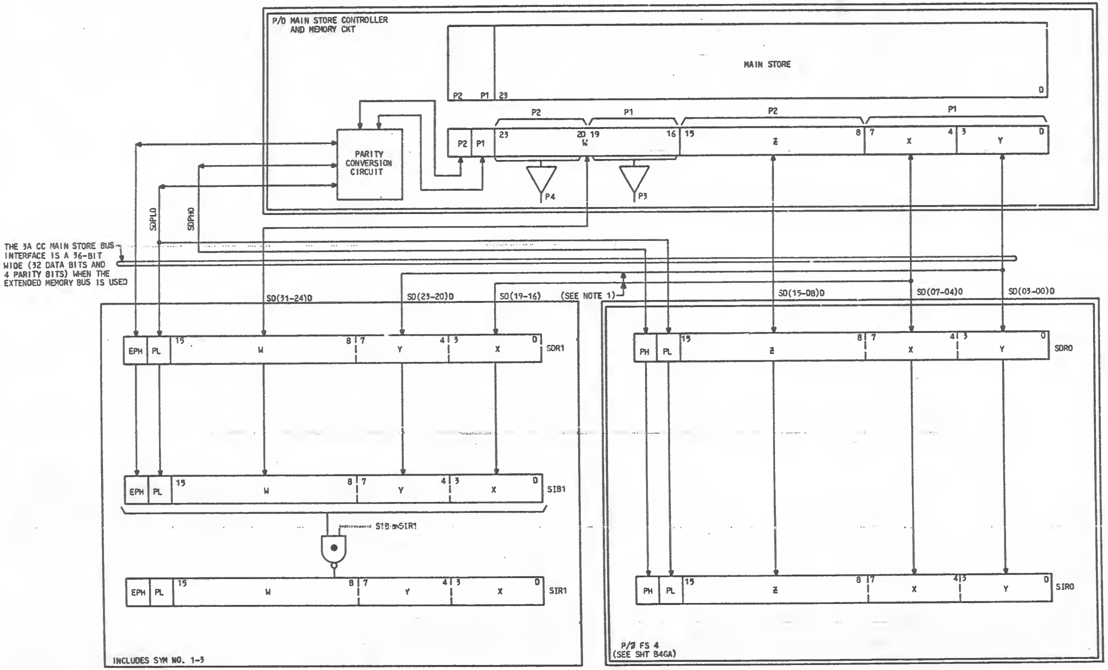
SD-1C900-01

PART OF FS II

EXTENDED MAIN MEMORY INTERFACE

COMPOSITE DIAGRAM 2

3A CC MAS MAPPING OF DATA BITS WHEN AN EXTENDED MAS INTERFACE IS USED



NOTES:

1. THE X AND Y FIELDS ARE DUPLICATED IN REGISTERS SDRO AND SDR1 FOR DATA READ COMMANDS. FOR INSTRUCTIONS READ THESE FIELDS ARE DUPLICATED IN SIRO AND SIR1. IN WRITE COMMANDS ONLY THE X AND Y FIELDS OF SDRO OUTPUT INTO THE MAS BUS TOGETHER WITH THE Z FIELD FROM SDRO AND W FIELD FROM SDR1.

CIRCUIT OPERATION

COMPOSITE DIAGRAM 2 SHOWS THE MAPPING OF DATA BITS CONTAINED IN THE MAS TO THE DATA BITS THAT ARE CONTAINED IN THE INTERFACE REGISTERS WITHIN THE 3A CC. NOTE THAT THE LOW 16 BITS OF THE MAS MAP DIRECTLY INTO THE LOW 16 BITS OF THE MASB INTERFACE. THIS IS REQUIRED TO KEEP THE COMPATIBILITY BETWEEN A 3A CC THAT USES AN EXTENDED MASB AND A 3A CC THAT HAS A NORMAL MASB OF 18 BITS. THE EXTENDED MASB INTERFACE AT THE 3A CC IS 36 BITS WIDE. FOR THE NO. 2B ESS APPLICATION THE MAS HAS 24 DATA BITS PLUS TWO PARITY BITS. AS INDICATED, THE W FIELD, WHICH IS BITS 16-23 OF THE MAS, IS MAPPED INTO BITS 24-31 IN THE 3A CC OR IN OTHER WORDS INTO BITS 8-15 OF SDR1. THE MAPPING INTO THE SDR1 REGISTER ALSO APPLIES TO THE SIR1 AND THE SIB. NOTE THAT THE W FIELD IN SDR1 CORRESPONDS TO THE Z FIELD IN SDRO: THAT IS, IT IS THE OP CODE FIELD. IN EXECUTING NO. 3A CC CODE, THE X AND Y FIELDS ARE TYPICALLY TWO 4-BIT OPERAND FIELDS. THESE TWO OPERAND FIELDS, X AND Y, ARE ALSO MAPPED INTO THE SDR1 BUT THEY ARE EXCHANGED IN THEIR RELATIVE POSITIONS. THE LATTER PROVIDES EFFICIENT HANDLING OF THE EMULATION OF THE NO. 2 COMMAND STRUCTURE; THAT IS, FOR THE HALF-WORD NO. 2B COMMANDS, THE Z FIELD AND ITS CORRESPONDING OPERAND FIELD, THE Y FIELD, ARE USED FOR THE RIGHT-HALF INSTRUCTION WITH THE X FIELD IN SDRO NOT NORMALLY USED. SIMILARLY IN SDR1 THE W FIELD IS THE OP CODE FIELD AND THE X FIELD IS THE OPERAND FOR THE W OP CODE. NOTE THAT IN RESPECT TO THEIR RESPECTIVE SDR REGISTERS THE Y OPERAND FIELD IS IN THE SAME RELEVENT POSITION AS THE X OPERAND FIELD.

FOR FULL-WORD COMMANDS IN THE NO. 2 EMULATION, THE Z FIELD CONTAINS THE OP CODE AND THE X AND Y FIELDS IN SDRO ARE NOT USED. INSTEAD, THE X, Y, AND W FIELDS IN SDR1 PROVIDE A 16-BIT DATA FIELD. NOTE THAT IN THIS INSTANCE THE CONTENTS OF MEMORY WILL BE ARRANGED SO THAT SDR1 WILL CONTAIN THE DATA IN A FORM THAT CAN BE USED DIRECTLY BY THE 3A CC. THE MAPPING OF THE DATA BITS FROM THE MAS TO THE 3A CC REQUIRES ONLY BACKPLANE WIRING TO IMPLEMENT. THE MAPPING OF THE PARITY BITS ON THAT DATA, HOWEVER, REQUIRES A SPECIAL PARITY CONVERSION CIRCUIT; THAT IS, THERE ARE TWO PARITY BITS OVER THE 24 DATA BITS IN MEMORY WITH THE PARITY BIT P1 OVER BITS 0-7 AND BITS 16-19. EVERYONE OF THESE BITS IS ON A SEPARATE BIT SLICED CIRCUIT PACK. SIMILARLY, P2 COVERS BITS 8-15 AND BITS 20-23, AND EACH OF THESE BITS IS ALSO ON A SEPARATE BIT SLICED CIRCUIT PACK. FOR THE NORMAL WIDTH STORE THERE ARE TWO PARITY BITS (PL AND PH). PL COVERS THE X AND Y FIELDS OR BITS 0-7 OF SDRO AND PH COVERS THE Z FIELD OR BITS 8-15 OF SDRO. THEREFORE, THE X AND Y FIELDS IN SDR1, WHICH ARE THE EXACT CONTENTS OF THE BITS 0-7 OF SDRO EXCEPT THEIR BIT POSITIONS ARE EXCHANGED REQUIRES THAT PL FOR SDR1 BE THE SAME AS PL FOR SDRO. THE W FIELD IN BITS 8-15 OF SDR1 IS A COMPLETELY SEPARATE DATA FIELD AND HENCE REQUIRES A NEW PARITY BIT CALLED EXTENDED PH (EPH). EXTENDED PH AS WELL AS PL AND PH MUST BE GENERATED BY A PARITY CONVERSION CIRCUIT. THE PARITY CONVERSION CIRCUIT USES AS ITS INPUTS P1 AND P2, WHICH ARE THE ACTUAL PARITY BITS STORED IN THE MAIN STORE TOGETHER WITH THE OUTPUT OF TWO PARITY TREES P3 AND P4, ATTACHED TO THE OUTPUT OF THE UPPER EIGHT BITS 16-23 OF THE MAS AS SHOWN IN COMPOSITE DIAGRAM 2. THE P3 GENERATES PARITY OVER BITS 16-19, P4 GENERATES PARITY OVER BITS 20-23 OF MAS. THEREFORE, WITH THESE FOUR INPUTS THE PARITY CONVERSION CIRCUIT CAN COMPUTE THE THREE REQUIRED PARITY BITS USED BY 3A CC. THE EQUATIONS FOR THESE INPUTS ARE: (1) PL=P1+P3, (2) PH=P2+P4, AND (3) EPH=P3+P4. THIS SAME PARITY CONVERSION CIRCUIT MUST ALSO PERFORM THE INVERSE FUNCTION WHEN A WRITE OPERATION IS PERFORMED. NOTE THAT FOR WRITE COMMANDS, ONLY THE X AND Y FIELDS OF SDRO ARE PLACED ON THE STORE DATA BUS AND THE X AND Y FIELDS OF SDR1 HAVE NO EFFECT ON THE DATA IN THE STORE DATA BUS.

PART OF FS 11
COMPOSITE DIAGRAM 2

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES
SD-1C900-01
B11GB

PART OF FS II

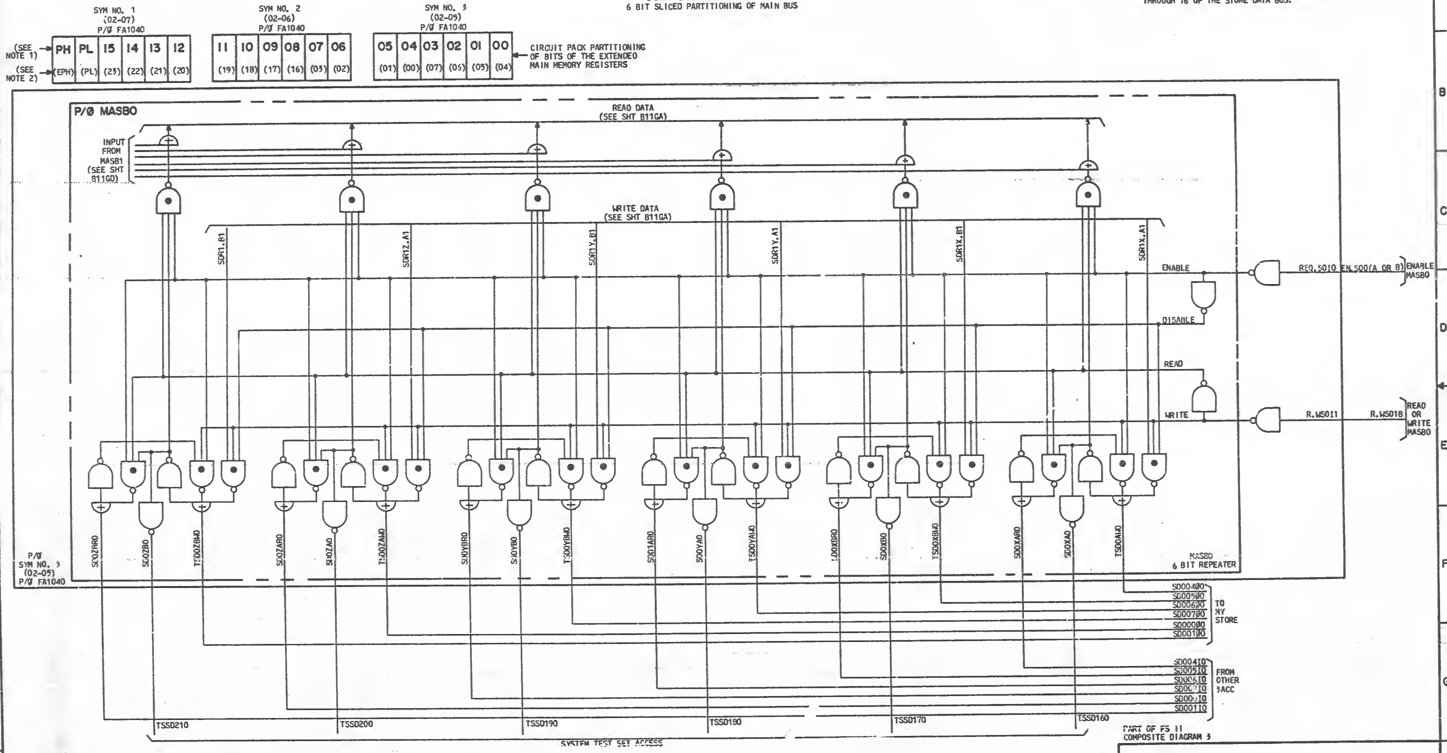
EXTENDED MAIN MEMORY INTERFACE

COMPOSITE DIAGRAM 3

6 BIT SLICED PARTITIONING OF MAIN BUS

CIRCUIT OPERATION

COMPOSITE DIAGRAM 3 SHOWS THE DETAILED LOGIC DESCRIPTION OF THE 6-BIT MASB REPEATER CIRCUIT FOR EXTENDED MASB FOR SYMBOL NO. 3. NOTE THAT SYMBOL NO. 1 AND SYMBOL NO. 2 HAVE THE IDENTICAL LOGIC OPERATIONS AS SYMBOL NO. 3. THE OPERATION OF THE EXTENDED MASBO REPEATER CIRCUIT FOR BITS 16-23 IS IDENTICAL TO THAT DESCRIBED IN FS 4 FOR BITS 0 THROUGH 16 OF THE STORE DATA BUS.



NOTES:

1. REFERS TO THE SDR1,SIB OR SIR1 DATA BIT CONTAINED ON THIS CIRCUIT PACK.
2. REFERS TO THE DATA BIT POSITION IN MAIN MEMORY THAT MAPS INTO THIS POSITION IN THE SDR1 OR SIB.

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	B11GC

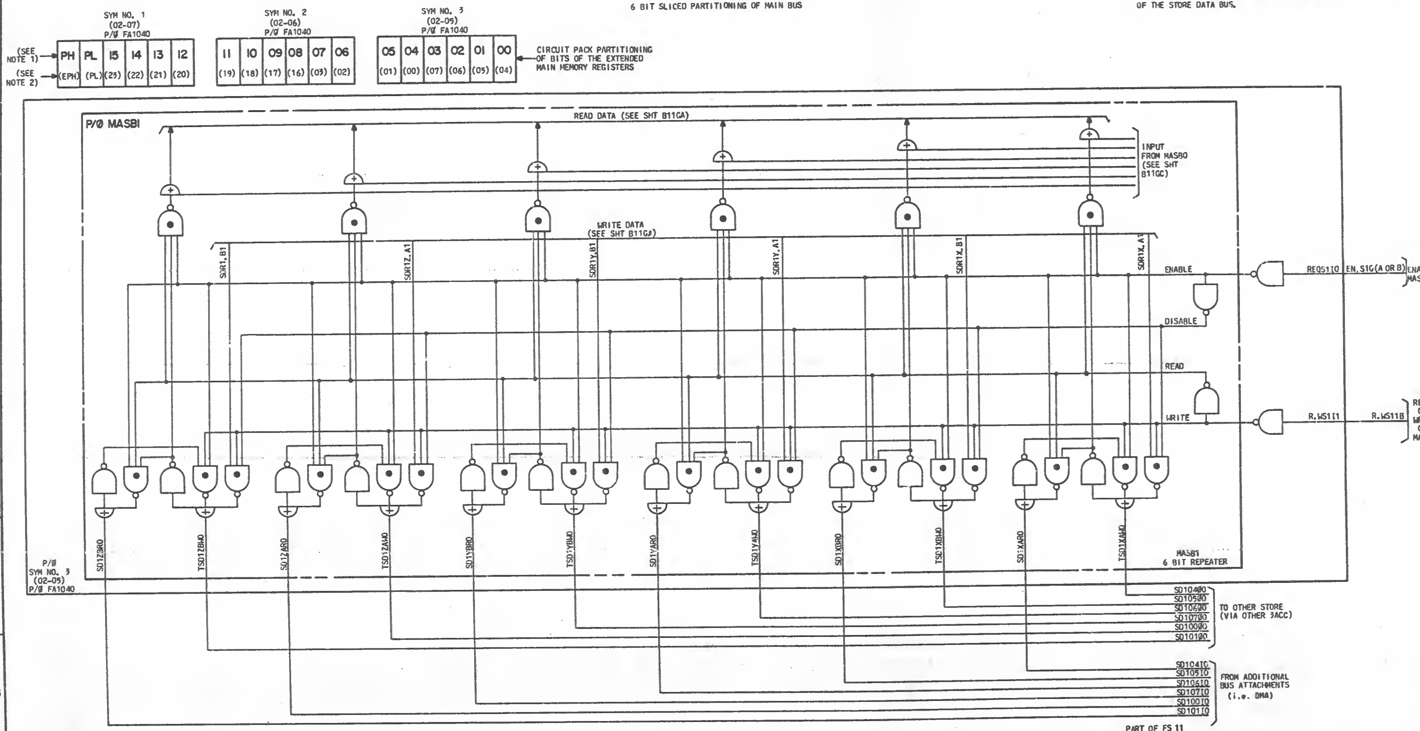
PRINTED IN U.S.A.

PART OF FS 11
EXTENDED MAIN MEMORY INTERFACE

COMPOSITE DIAGRAM 4
6 BIT SLICED PARTITIONING OF MAIN BUS

CIRCUIT OPERATION

COMPOSITE DIAGRAM 4 SHOWS THE DETAILED LOGIC DESCRIPTION OF THE 6-BIT MAS. REPEATER CIRCUIT FOR EXTENDED MASB FOR SYMBOL NO. 3. NOTE THAT SYMBOL NO. 2 AND SYMBOL NO. 1 HAVE THE IDENTICAL LOGIC OPERATIONS. THE OPERATION OF THE EXTENDED MASB1 REPEATER CIRCUIT FOR BITS 16-23 IS IDENTICAL TO THAT DESCRIBED IN FS 4 FOR BITS 0 THROUGH 16 OF THE STORE DATA BUS.



PART OF FS 11
COMPOSITE DIAGRAM 4

NOTES:

1. REFERS TO THE SDR1, SIB OR SIR1 DATA BIT CONTAINED ON THIS CIRCUIT PACK.
2. REFERS TO THE DATA BIT POSITION IN MAIN MEMORY THAT MAPS INTO THIS POSITION IN THE SDR1 OR SIB.

3A CENTRAL CONTROL ②		DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01		B11GD

E - 7421 (12 - 73)

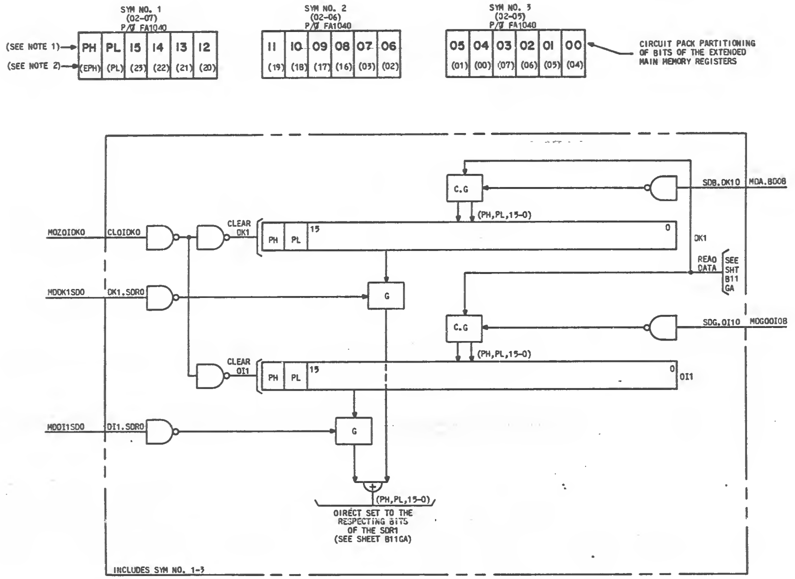
PRINTED IN U.S.A.

PART OF FS 11

EXTENDED MAIN MEMORY INTERFACE

COMPOSITE DIAGRAM 5

DOUBLE STORE READ ASSOCIATED
DATA REGISTERS



NOTES:

1. REFERS TO THE SDR1, SIB OR SIR1 DATA BITS CONTAINED ON THIS CIRCUIT PACK.
2. REFERS TO THE DATA BIT POSITION IN MAIN MEMORY THAT MAPS INTO THIS POSITION IN THE SDR1 OR SIB.

CIRCUIT OPERATION

THE DOUBLE STORE READ (DSR) ASSOCIATED DATA REGISTERS DESIGNED TO COLLECT DATA TO AID IN THE ANALYSIS OF MEMORY LOCATIONS THAT FAILED AND HENCE REQUIRED AN AUTOMATIC REREAD OF THE OFF-LINE-STORE TO ACCESS A CORRECT COPY OF DATA.

THE REGISTERS ARE DESIGNATED DK1 AND DI1 BECAUSE OF THEIR RELATIONSHIP TO DK AND DI REGISTERS; THAT IS, WHEN THESE REGISTERS ARE USED IN CONJUNCTION WITH THE DSR TECHNIQUE AND AN UNSUCCESSFUL READ OF THE ON-LINE MEMORY OCCURRED. THE BAD DATA IS GATED (LOW ORDER 16 BITS PLUS THE CORRESPONDING PARITY BITS) INTO THE DK REGISTER AND THE UPPER BITS 16-24 IS GATED INTO DK1. IN ADDITION THE 0-7 BITS OF THE MASB ARE ALSO GATED INTO DK1 AS INDICATED IN THE MAPPING TECHNIQUE ON SHEET B11GB. THIS GATING IS ENABLED WITH THE SIGNAL INDICATED WITH THE TERMINAL MODIFIER SDB. DKBIO. (SEE SHT B4GM). SIMILARLY, WHEN THE GOOD DATA IS RETURNED FROM THE OFF-LINE MAS ON THE SECOND HALF OF THE DSR OPERATION, IT IS GATED, IN ADDITION TO THE SDR OR THE SIR WHERE IT IS TO BE USED, INTO THE DI AND THE DI1 REGISTERS. IN THIS WAY A COPY OF THE GOOD AND BAD DATA IS SAVED IN THESE REGISTERS SO THAT THE SOFTWARE CAN PERFORM ERROR ANALYSIS. NOTE ALSO THAT THE AK IS USED TO SAVE THE ADDRESS AT WHICH THE BAD DATA IS LOCATED.

A MISCELLANEOUS DECODER CROSSPOINT CONTROL IS PROVIDED TO CLEAR THE DK1 AND DI1 SIMULTANEOUSLY AND ALSO TO GATE THE DK TO SDR1. NOTE THAT THE CONTROL SIGNAL THAT GATES THE DK1 INTO THE SDR REGISTER DOES NOT DO A CLEAR AND GATE FUNCTION; THEREFORE, THE SOFTWARE MUST FIRST CLEAR THE SDRO BEFORE GATING THE DK1 TO IT TO OBTAIN VALID RESULTS. SIMILARLY, THE DI1 REGISTER CAN BE GATED TO THE SDR1 WITH THE MISCELLANEOUS DECODER CROSSPOINT.

PART OF FS 11
COMPOSITE DIAGRAM 5

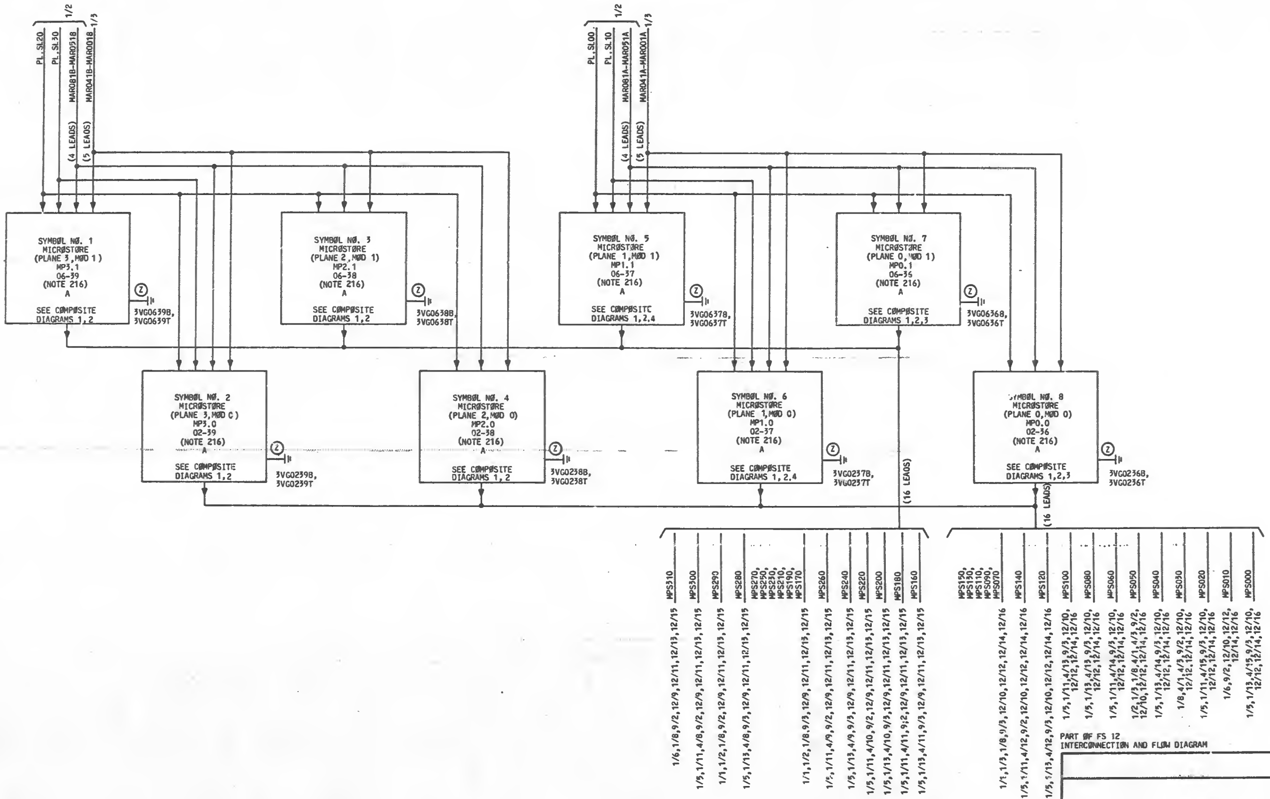
3A CENTRAL CONTROL ②

DWG SIZE	ISSUE
6S	4A

BELL LABORATORIES | SD-1C900-01 | B11GE

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)
INTERCONNECTION AND FLOW DIAGRAM


1/2
1/3
PL.SL20
PL.SL30
MAR081B-MAR051B
MAR041B-MAR001B
(4 LEADS)
(5 LEADS)
PL.SL00
PL.SL10
MAR081A-MAR051A
MAR041A-MAR001A
SYMBØL NØ. 1 MICRØSTØRE (PLANE 3,MØD 1) MP3.1 06-39 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1,2
3VG0639B, 3VG0639T
SYMBØL NØ. 3 MICRØSTØRE (PLANE 2,MØD 1) MP2.1 06-38 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1,2
3VG0638B, 3VG0638T
SYMBØL NØ. 5 MICRØSTØRE (PLANE 1,MØD 1) MP1.1 06-37 (NOTE 216) A SEE CØMPØSITC DIAGRAMS 1,2,4
3VG0637B, 3VG0637T
SYMBØL NØ. 7 MICRØSTØRE (PLANE 0,MØD 1) MP0.1 06-36 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1,2,3
3VG0636B, 3VG0636T
SYMBØL NØ. 2 MICRØSTØRE (PLANE 3,MØD C) MP3.0 02-39 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1,2
3VG0239B, 3VG0239T
SYMBØL NØ. 4 MICRØSTØRE (PLANE 2,MØD 0) MP2.0 02-38 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0238B, 3VG0238T
SYMBØL NØ. 6 MICRØSTØRE (PLANE 1,MØD 0) MP1.0 02-37 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2,4
3VG0237B, 3VG0237T
SYMBØL NØ. 8 MICRØSTØRE (PLANE 0,MØD 0) MP0.0 02-36 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1,2,3
3VG0236B, 3VG0236T
Z
(16 LEADS)
(16 LEADS)
MPS310 1/6,1/8,9/2,12/9,12/11,12/13,12/15
MPS300 1/5,1/11,4/8,9/2,12/9,12/11,12/13,12/15
MPS290 1/1,1/2,1/8,9/2,12/9,12/11,12/13,12/15
MPS280 1/5,1/13,4/8,9/3,12/9,12/11,12/13,12/15
MPS270, MPS250, MPS230, MPS210, MPS190, MPS170 1/1,1/2,1/8,9/3,12/9,12/11,12/13,12/15
MPS260 1/5,1/11,4/9,9/2,12/9,12/11,12/13,12/15
MPS240 1/5,1/13,4/9,9/3,12/9,12/11,12/13,12/15
MPS220 1/5,1/11,4/10,9/2,12/9,12/11,12/13,12/15
MPS200 1/5,1/13,4/10,9/3,12/9,12/11,12/13,12/15
MPS180 1/5,1/11,4/11,9;2,12/9,12/11,12/13,12/15
MPS160 1/5,1/13,4/11,9/3,12/9,12/11,12/13,12/15
MPS150, MPS130, MPS110, MPS090, MPS070 1/1,1/3,1/8,9/3,12/10,12/12,12/14,12/16
MPS140 1/5,1/11,4/12,9/2,12/10,12/12,12/14,12/16
MPS120 1/5,1/13,4/12,9/3,12/10,12/12,12/14,12/16
MPS100 1/5,1/11,4/13,9/3,12/10, 12/12,12/14,12/16
MPS080 1/5,1/13,4/13,9/3,12/10, 12/12,12/14,12/16
MPS060 1/5,1/11,4/14,9/3,12/10, 12/12,12/14,12/16
MPS050 1/2,1/3,1/8,4/1,4/3,9/2, 12/10,12/12,12/14,12/16
MPS040 1/5,1/13,4/14,9/3,12/10, 12/12,12/14,12/16
MPS030 1/8,4/1,4/3,9/2,12/10, 12/12,12/14,12/16
MPS020 1/5,1/11,4/15,9/3,12/10, 12/12,12/14,12/16
MPS010 1/6,9/2,12/10,12/12, 12/14,12/16
MPS000 1/5,1/13,4/15,9/3,12/10, 12/12,12/14,12/16

PART ØF FS 12
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL

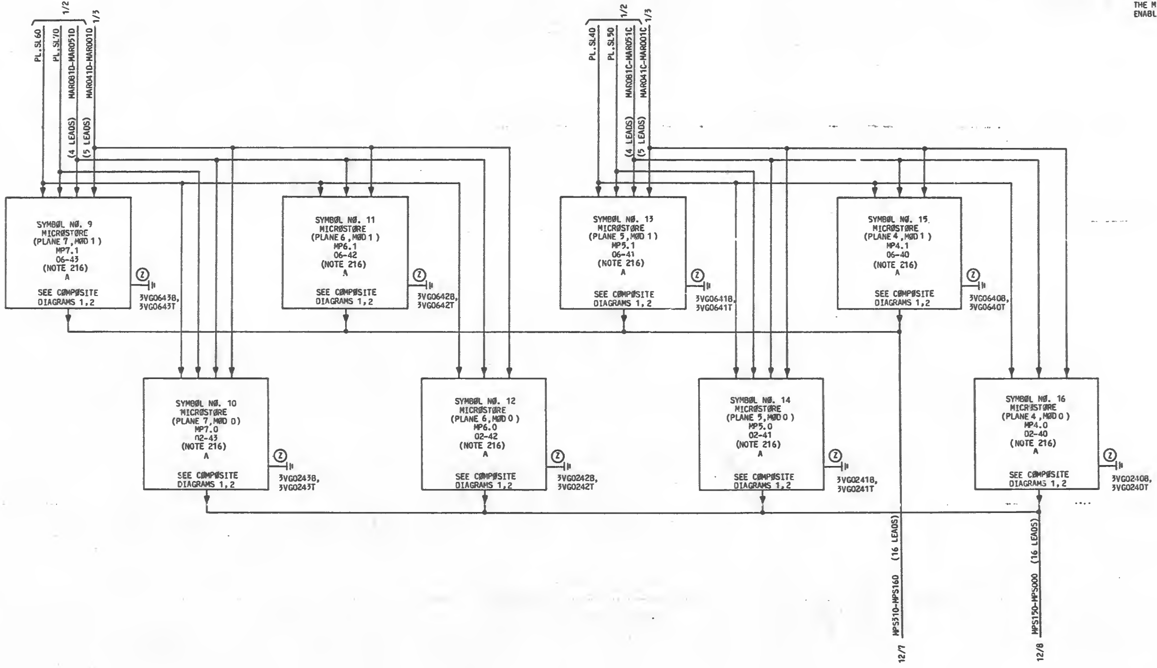
DWG SIZE 6S
ISSUE 6D
BELL LABORATORIES
SD-1C900-01
B12AA

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)
INTERCONNECTION AND FLOW DIAGRAM

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
MAR001(A-D)- MAR081(A-D)	OUTPUTS OF THE MAR REGISTER BITS 0-8 (INPUTS TO MICROSTORE)
MPS000-MPS310	BITS 0-31 OF THE MICROPROCESSOR STORE OUTPUT
PL.SL00-PL.SL70	BIT 0-7 OF THE PLANE SELECT LEADS FOR THE MICROSTORE (EACH PLANE SELECT ENABLES A 512 BY 32-WORD BLOCK)


PL.SL60
PL.SL70
MAR081D-MAR051D
MAR041D-MAR001D
1/2
1/3
(4 LEADS)
(5 LEADS)
PL.SL40
PL.SL50
MAR081C-MAR051C
MAR041C-MAR001C
1/2
1/3
(4 LEADS)
(5 LEADS)
SYMBØL NØ. 9 MICRØSTØRE (PLANE 7, MØD 1) MP7.1 06-43 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0643B, 3VG0643T
SYMBØL NØ. 11 MICRØSTØRE (PLANE 6, MØD 1) MP6.1 06-42 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0642B, 3VG0642T
SYMBØL NØ. 13 MICRØSTØRE (PLANE 5, MØD 1) MP5.1 06-41 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0641B, 3VG0641T
SYMBØL NØ. 15 MICRØSTØRE (PLANE 4, MØD 1) MP4.1 06-40 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0640B, 3VG0640T
SYMBØL NØ. 10 MICRØSTØRE (PLANE 7, MØD 0) MP7.0 02-43 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0243B, 3VG0243T
SYMBØL NØ. 12 MICRØSTØRE (PLANE 6, MØD 0) MP6.0 02-42 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0242B, 3VG0242T
SYMBØL NØ. 14 MICRØSTØRE (PLANE 5, MØD 0) MP5.0 02-41 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0241B, 3VG0241T
SYMBØL NØ. 16 MICRØSTØRE (PLANE 4, MØD 0) MP4.0 02-40 (NOTE 216) A SEE CØMPØSITE DIAGRAMS 1, 2
3VG0240B, 3VG0240T
Z
MPS310-MPS160 (16 LEADS)
12/7
MPS150-MPS000 (16 LEADS)
12/8

PART ØF FS 12
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENT 'I CØNTRØL

DWG SIZE	ISSUE	
65	6D	
BELL LABORATORIES	SD-1C900-01	812AB

E - 7421 (12 - 73)

PRINTED IN U.S.A.

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 1

MICROSTORE
(PLANE 3,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP3.1	06-39	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MAR001B	I	208	1/3		A0	
MAR011B	I	308	1/3		A1	
MAR021B	I	111	1/3		A2	
MAR031B	I	110	1/3		A3	
MAR041B	I	309	1/3		A4	
MAR051B	I	010	1/2		A5	
MAR061B	I	011	1/2		A6	
MAR071B	I	209	1/2		A7	
MAR081B	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL20	I	312	1/2		PSL	
PL.SL30	I	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0639B	GRD	004	(2)12/1			
	GRD	007	(2)12/1			
	GRD	008	(2)12/1			
	GRD	102	(2)12/1			
	GRD	103	(2)12/1			
	GRD	105	(2)12/1			
	GRD	106	(2)12/1			
	GRD	202	(2)12/1			
	GRD	204	(2)12/1			
	GRD	205	(2)12/1			
	GRD	207	(2)12/1			
	GRD	303	(2)12/1			
	GRD	306	(2)12/1			
	GRD	307	(2)12/1			
	GRD	200			GRD	
3VG0639T	GRD	014	(2)12/1			
	GRD	017	(2)12/1			
	GRD	019	(2)12/1			
	GRD	113	(2)12/1			
	GRD	114	(2)12/1			
	GRD	115	(2)12/1			
	GRD	116	(2)12/1			
	GRD	118	(2)12/1			
	GRD	212	(2)12/1			
	GRD	213	(2)12/1			
	GRD	214	(2)12/1			
	GRD	217	(2)12/1			
	GRD	218	(2)12/1			
	GRD	314	(2)12/1			

SYMBOL NO. 1 (CONT)

MICROSTORE
(PLANE 3,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP3.1	06-39	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0639T	GRD	316	(2)12/1			
	GRD	318	(2)12/1			
	GRD	319	(2)12/1		GRD	
	GRD	215				
3V058C	PWR	000	(2)14/6	203	+3	
	PWR	119	(2)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001	14/23	203	+5	
	PWR	100	14/23	203	+5	
	PWR	101	14/23	203	+5	
	PWR	201	14/23	203	+5	
	PWR	300	14/23	203	+5	
	PWR	301	14/23	203	+5	
5V061B	PWR	001	(2)14/25	203	+5	
	PWR	100	(2)14/25	203	+5	
	PWR	101	(2)14/25	203	+5	
	PWR	201	(2)14/25	203	+5	
	PWR	300	(2)14/25	203	+5	
	PWR	301	(2)14/25	203	+5	

SYMBOL NO. 2

MICROSTORE
(PLANE 3,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP3.0	02-39	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MAR001B	I	208	1/3		A0	
MAR011B	I	308	1/3		A1	
MAR021B	I	111	1/3		A2	
MAR031B	I	110	1/3		A3	
MAR041B	I	309	1/3		A4	
MAR051B	I	010	1/2		A5	
MAR061B	I	011	1/2		A6	
MAR071B	I	209	1/2		A7	
MAR081B	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	
MPS140	OT	018	12/8		B14N	

SYMBOL NO. 2 (CONT)

MICROSTORE
(PLANE 3,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP3.0	02-39	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MPS150	OT	219	12/8		B15N	
PL.SL20	I	312	1/2		PSL	
PL.SL30	I	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0239B	GRD	004	(2)12/2			
	GRD	007	(2)12/2			
	GRD	008	(2)12/2			
	GRD	102	(2)12/2			
	GRD	103	(2)12/2			
	GRD	105	(2)12/2			
	GRD	106	(2)12/2			
	GRD	200	(2)12/2		GRD	
	GRD	202	(2)12/2			
	GRD	204	(2)12/2			
	GRD	205	(2)12/2			
	GRD	207	(2)12/2			
	GRD	306	(2)12/2			
	GRD	307	(2)12/2			
	GRD	303				
3VG0239T	GRD	017	(2)12/2			
	GRD	019	(2)12/2			
	GRD	113	(2)12/2			
	GRD	114	(2)12/2			
	GRD	115	(2)12/2			
	GRD	116	(2)12/2			
	GRD	118	(2)12/2			
	GRD	212	(2)12/2			
	GRD	213	(2)12/2			
	GRD	214	(2)12/2			
	GRD	215	(2)12/2			
	GRD	217	(2)12/2			
	GRD	218	(2)12/2			
	GRD	314	(2)12/2			
	GRD	316	(2)12/2			
	GRD	318	(2)12/2			
	GRD	319	(2)12/2		GRD	
	GRD	014				
3V058C	PWR	000	(2)14/6	203	+3	
	PWR	119	(2)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001	14/23	203	+5	
	PWR	100	14/23	203	+5	
	PWR	101	14/23	203	+5	
	PWR	201	14/23	203	+5	
	PWR	300	14/23	203	+5	
	PWR	301	14/23	203	+5	
5V061B	PWR	001	(2)14/25	203	+5	
	PWR	100	(2)14/25	203	+5	
	PWR	101	(2)14/25	203	+5	
	PWR	201	(2)14/25	203	+5	
	PWR	300	(2)14/25	203	+5	
	PWR	301	(2)14/25	203	+5	

PART OF FS 12
SYMBOL(S) 1 2

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01	B12CA

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PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 3

MICROSTORE
(PLANE 2,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP2.1	06-38	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		312			PSL	
MAR001B	I	208	1/3		A0	
MAR011B	I	308	1/3		A1	
MAR021B	I	111	1/3		A2	
MAR031B	I	110	1/3		A3	
MAR041B	1	309	1/3		A4	
MAR051B	I	010	1/2		A5	
MAR061B	I	011	1/2		A6	
MAR071B	I	209	1/2		A7	
MAR081B	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL20	I	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0638B	GRD	004	(Z)12/3			
	GRD	007	(Z)12/3			
	GRD	008	(Z)12/3			
	GRD	102	(Z)12/3			
	GRD	103	(Z)12/3			
	GRD	105	(Z)12/3			
	GRD	106	(Z)12/3			
	GRD	202	(Z)12/3			
	GRD	204	(Z)12/3			
	GRD	205	(Z)12/3			
	GRD	207	(Z)12/3			
	GRD	303	(Z)12/3			
	GRD	306	(Z)12/3			
	GRD	307	(Z)12/3			
	GRD	200			GRD	
3VG0638T	GRD	014	(Z)12/3			
	GRD	017	(Z)12/3			
	GRD	019	(Z)12/3			
	GRD	113	(Z)12/3			
	GRD	114	(Z)12/3			
	GRD	115	(Z)12/3			
	GRD	116	(Z)12/3			
	GRD	118	(Z)12/3			
	GRD	212	(Z)12/3			
	GRD	213	(Z)12/3			
	GRD	214	(Z)12/3			
	GRD	215	(Z)12/3			
	GRD	217	(Z)12/3			
	GRD	218	(Z)12/3			

SYMBOL NO. 3 (CONT)

MICROSTORE
(PLANE 2,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP2.1	06-38	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0638T	GRD	314	(Z)12/3			
	GRD	316	(Z)12/3			
	GRD	318	(Z)12/3			
	GRD	319			GRD	
3V058C	PWR	000	(Z)14/6	203	+3	
	PWR	119	(Z)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001	14/23	203	+5	
	PWR	100	14/23	203	+5	
	PWR	101	14/23	203	+5	
	PWR	201	14/23	203	+5	
	PWR	300	14/23	203	+5	
	PWR	301	14/23	203	+5	
5V061B	PWR	001	(Z)14/25	203	+5	
	PWR	100	(Z)14/25	203	+5	
	PWR	101	(Z)14/25	203	+5	
	PWR	201	(Z)14/25	203	+5	
	PWR	300	(Z)14/25	203	+5	
	PWR	301	(Z)14/25	203	+5	

SYMBOL NO. 4

MICROSTORE
(PLANE 2,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP2.0	02-38	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		312			PSL	
MAR001B	I	208	1/3		A0	
MAR011B	I	308	1/3		A1	
MAR021B	I	111	1/3		A2	
MAR031B	I	110	1/3		A3	
MAR041B	I	309	1/3		A4	
MAR051B	I	010	1/2		A5	
MAR061B	I	011	1/2		A6	
MAR071B	I	209	1/2		A7	
MAR081B	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	

SYMBOL NO. 4 (CONT)

MICROSTORE
(PLANE 2,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP2.0	02-38	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MPS140	OT	018	12/8		B14N	
MPS150	OT	219	12/8		B15N	
PL.SL20	I	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0238B	GRD	004	(Z)12/4			
	GRD	007	(Z)12/4			
	GRD	008	(Z)12/4			
	GRD	102	(Z)12/4			
	GRD	105	(Z)12/4			
	GRD	106	(Z)12/4			
	GRD	200	(Z)12/4		GRD	
	GRD	202	(Z)12/4			
	GRD	204	(Z)12/4			
	GRD	205	(Z)12/4			
	GRD	207	(Z)12/4			
	GRD	303	(Z)12/4			
	GRD	306	(Z)12/4			
	GRD	307	(Z)12/4			
	GRD	103				
3VG0238T	GRD	014	(Z)12/4			
	GRD	017	(Z)12/4			
	GRD	019	(Z)12/4			
	GRD	113	(Z)12/4			
	GRD	114	(Z)12/4			
	GRD	116	(Z)12/4			
	GRD	118	(Z)12/4			
	GRD	212	(Z)12/4			
	GRD	213	(Z)12/4			
	GRD	214	(Z)12/4			
	GRD	215	(Z)12/4			
	GRD	217	(Z)12/4			
	GRD	218	(Z)12/4			
	GRD	314	(Z)12/4			
	GRD	316	(Z)12/4			
	GRD	318	(Z)12/4			
	GRD	319	(Z)12/4		GRD	
	GRD	115				
3V058C	PWR	000	(Z)14/6	203	+3	
	PWR	119	(Z)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001	14/23	203	+5	
	PWR	100	14/23	203	+5	
	PWR	101	14/23	203	+5	
	PWR	201	14/23	203	+5	
	PWR	300	14/23	203	+5	
	PWR	301	14/23	203	+5	
5V061B	PWR	001	(Z)14/25	203	+5	
	PWR	100	(Z)14/25	203	+5	
	PWR	101	(Z)14/25	203	+5	
	PWR	201	(Z)14/25	203	+5	
	PWR	300	(Z)14/25	203	+5	
	PWR	301	(Z)14/25	203	+5	

PART OF FS 12
SYMBOL(S) 3 4

3A CENTRAL . ITROL	DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01	B12CB

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06/10/77

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 5

MICROSTORE
(PLANE 1,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP1.1	06-37	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MAR001A	I	208	1/3		A0	
MAR011A	I	308	1/3		A1	
MAR021A	I	111	1/3		A2	
MAR031A	I	110	1/3		A3	
MAR041A	I	309	1/3		A4	
MAR051A	I	010	1/2		A5	
MAR061A	I	011	1/2		A6	
MAR071A	I	209	1/2		A7	
MAR081A	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL00	I	312	1/2		PSL	
PL.SL10	I	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0637B	GRD	004	(2)12/5			
	GRD	007	(2)12/5			
	GRD	008	(2)12/5			
	GRD	102	(2)12/5			
	GRD	103	(2)12/5			
	GRD	105	(2)12/5			
	GRD	106	(2)12/5			
	GRD	200	(2)12/5		GRD	
	GRD	202	(2)12/5			
	GRD	204	(2)12/5			
	GRD	207	(2)12/5			
	GRD	303	(2)12/5			
	GRD	306	(2)12/5			
	GRD	307	(2)12/5			
	GRD	205				
3VG0637T	GRD	014	(2)12/5			
	GRD	017	(2)12/5			
	GRD	019	(2)12/5			
	GRD	113	(2)12/5			
	GRD	114	(2)12/5			
	GRD	115	(2)12/5			
	GRD	116	(2)12/5			
	GRD	118	(2)12/5			
	GRD	212	(2)12/5			
	GRD	213	(2)12/5			
	GRD	214	(2)12/5			
	GRD	215	(2)12/5			
	GRD	217	(2)12/5			
	GRD	218	(2)12/5			

SYMBOL NO. 5 (CONT)

MICROSTORE
(PLANE 1,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP1.1	06-37	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0637T	GRD	314	(2)12/5			
	GRD	318	(2)12/5			
	GRD	319	(2)12/5		GRD	
	GRD	316				
3V058C	PWR	000	(2)14/6	203	+3	
	PWR	119	(2)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

SYMBOL NO. 6

MICROSTORE
(PLANE 1,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP1.0	02-37	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MAR001A	I	208	1/3		A0	
MAR011A	I	308	1/3		A1	
MAR021A	I	111	1/3		A2	
MAR031A	I	110	1/3		A3	
MAR041A	I	309	1/3		A4	
MAR051A	I	010	1/2		A5	
MAR061A	I	011	1/2		A6	
MAR071A	I	209	1/2		A7	
MAR081A	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	
MPS140	OT	018	12/8		B14N	
MPS150	OT	219	12/8		B15N	
PL.SL00	I	312	1/2		PSL	
PL.SL10	I	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	

SYMBOL NO. 6 (CONT)

MICROSTORE
(PLANE 1,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP1.0	02-37	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058C	GRD	319		203	GRD	
3VG0237B	GRD	004	(2)12/6			
	GRD	007	(2)12/6			
	GRD	008	(2)12/6			
	GRD	102	(2)12/6			
	GRD	103	(2)12/6			
	GRD	105	(2)12/6			
	GRD	106	(2)12/6			
	GRD	202	(2)12/6			
	GRD	204	(2)12/6			
	GRD	205	(2)12/6			
	GRD	207	(2)12/6			
	GRD	303	(2)12/6			
	GRD	306	(2)12/6			
	GRD	307	(2)12/6			
	GRD	200			GRD	
3VG0237T	GRD	014	(2)12/6			
	GRD	017	(2)12/6			
	GRD	113	(2)12/6			
	GRD	114	(2)12/6			
	GRD	115	(2)12/6			
	GRD	116	(2)12/6			
	GRD	118	(2)12/6			
	GRD	212	(2)12/6			
	GRD	213	(2)12/6			
	GRD	214	(2)12/6			
	GRD	215	(2)12/6			
	GRD	217	(2)12/6			
	GRD	218	(2)12/6			
	GRD	314	(2)12/6			
	GRD	316	(2)12/6			
	GRD	318	(2)12/6			
	GRD	319	(2)12/6		GRD	
	GRD	019				
3V058C	PWR	000	(2)14/6	203	+3	
	PWR	119	(2)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

PART OF FS 12
SYMBOL(S) 5 6

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01		B12CC

PRINTED IN U. S. A.

06/10/77

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 7

MICROSTORE
(PLANE 0,MOD 1)

```
DESIG    EQPT    CODE          ELEM     OPT
         LOC                   IDENT
-----    ----    ----          -----    ---
MP0.1    06-36   (NOTE 216)    A

-------------------- FS INFO --------------------   ---- CP INFO -----

LEAD                                                TERM.
DESIG    FUNC  TERM.  DESTINATION        NOTE       MOD      LOC
-----    ----  -----  -----------        ----       -----    ---
               312                                  PSL
MAR001A  I     208    1/3                           A0
MAR011A  I     308    1/3                           A1

MAR021A  I     111    1/3                           A2
MAR031A  I     110    1/3                           A3
MAR041A  I     309    1/3                           A4

MAR051A  I     010    1/2                           A5
MAR061A  I     011    1/2                           A6
MAR071A  I     209    1/2                           A7

MAR081A  I     012    1/2                           A8
MPS160   OT    002    4/11,9/3                      B0N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/13
MPS170   OT    302    9/3,12/1                      B1N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8

MPS180   OT    203    4/11,9/2                      B2N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/11
MPS190   OT    104    9/3,12/1                      B3N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8
MPS200   OT    005    4/10,9/3                      B4N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/13
MPS210   OT    305    9/3,12/1                      B5N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8
MPS220   OT    206    4/10,9/2                      B6N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/11
MPS230   OT    107    9/3,12/1                      B7N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8

MPS240   OT    013    4/9,9/3                       B8N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/13
MPS250   OT    313    9/3,12/1                      B9N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8
MPS260   OT    015    4/9,9/2                       B10N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
```

SYMBOL NO. 7 (CONT)

MICROSTORE
(PLANE 0,MOD 1)

```
DESIG    EQPT    CODE          ELEM     OPT
         LOC                   IDENT
-----    ----    ----          -----    ---
MP0.1    06-36   (NOTE 216)    A

-------------------- FS INFO --------------------   ---- CP INFO -----

LEAD                                                TERM.
DESIG    FUNC  TERM.  DESTINATION        NOTE       MOD      LOC
-----    ----  -----  -----------        ----       -----    ---
         I            1/5,1/11

MPS270   OT    315    9/3,12/1                      B11N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8
MPS280   OT    216    4/8,9/3                       B12N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/13
MPS290   OT    117    9/2,12/1                      B13N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/1,1/2
                      1/8

MPS300   OT    018    4/8,9/2                       B14N
                      12/1,12/3
                      12/5,12/9
                      12/11,12/13
                      12/15
         I            1/5,1/11
MPS310   OT    219    9/2,12/1                      B15N
                      12/3,12/5
                      12/9,12/11
                      12/13,12/15
         I            1/6,1/8
PL.SL00  I     112    1/2                           PSH

3T058C   GRD   0GD                       203        GRD
         GRD   2GD                       203        GRD
         GRD   200                       203        GRD

         GRD   319                       203        GRD
3VG0636B GRD   004    (2)12/7
         GRD   007    (2)12/7

         GRD   008    (2)12/7
         GRD   102    (2)12/7
         GRD   103    (2)12/7

         GRD   105    (2)12/7
         GRD   106    (2)12/7
         GRD   202    (2)12/7

         GRD   204    (2)12/7
         GRD   205    (2)12/7
         GRD   207    (2)12/7

         GRD   303    (2)12/7
         GRD   306    (2)12/7
         GRD   307    (2)12/7

         GRD   200                                  GRD
3VG0636T GRD   014    (2)12/7
         GRD   017    (2)12/7

         GRD   019    (2)12/7
         GRD   113    (2)12/7
         GRD   114    (2)12/7

         GRD   115    (2)12/7
         GRD   116    (2)12/7
         GRD   118    (2)12/7

         GRD   213    (2)12/7
         GRD   214    (2)12/7
         GRD   215    (2)12/7

         GRD   217    (2)12/7
         GRD   218    (2)12/7
         GRD   314    (2)12/7
```

SYMBOL NO. 7 (CONT)

MICROSTORE
(PLANE 0,MOD 1)

```
DESIG    EQPT    CODE          ELEM     OPT
         LOC                   IDENT
-----    ----    ----          -----    ---
MP0.1    06-36   (NOTE 216)    A

-------------------- FS INFO --------------------   ---- CP INFO -----

LEAD                                                TERM.
DESIG    FUNC  TERM.  DESTINATION        NOTE       MOD      LOC
-----    ----  -----  -----------        ----       -----    ---
3VG0636T GRD   316    (2)12/7
         GRD   318    (2)12/7
         GRD   319    (2)12/7                       GRD

         GRD   212
3V058C   PWR   000    (2)14/6            203        +3
         PWR   119    (2)14/6            203        +3

3V058F   PWR   000    14/6               203        +3
         PWR   119    14/6               203        +3
5V061A   PWR   001                       203        +5

         PWR   100                       203        +5
         PWR   101                       203        +5
         PWR   201                       203        +5

         PWR   300                       203        +5
         PWR   301                       203        +5
```

SYMBOL NO. 8

MICROSTORE
(PLANE 0,MOD 0)

```
DESIG    EQPT    CODE          ELEM     OPT
         LOC                   IDENT
-----    ----    ----          -----    ---
MP0.0    02-36   (NOTE 216)    A

-------------------- FS INFO --------------------   ---- CP INFO -----

LEAD                                                TERM.
DESIG    FUNC  TERM.  DESTINATION        NOTE       MOD      LOC
-----    ----  -----  -----------        ----       -----    ---
               312                                  PSL
MAR001A  I     208    1/3                           A0
MAR011A  I     308    1/3                           A1

MAR021A  I     111    1/3                           A2
MAR031A  I     110    1/3                           A3
MAR041A  I     309    1/3                           A4

MAR051A  I     010    1/2                           A5
MAR061A  I     011    1/2                           A6
MAR071A  I     209    1/2                           A7

MAR081A  I     012    1/2                           A8
MPS000   OT    002    4/15,9/3                      B0N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/13
MPS010   OT    302    9/2,12/2                      B1N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/6

MPS020   OT    203    4/15,9/3                      B2N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/11
MPS030   OT    104    9/2,12/2                      B3N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/8,4/1
                      4/3
MPS040   OT    005    4/14,9/3                      B4N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/13
```

SYMBOL NO. 8 (CONT)

MICROSTORE
(PLANE 0,MOD 0)

```
DESIG    EQPT    CODE          ELEM     OPT
         LOC                   IDENT
-----    ----    ----          -----    ---
MP0.0    02-36   (NOTE 216)    A

-------------------- FS INFO --------------------   ---- CP INFO -----

LEAD                                                TERM.
DESIG    FUNC  TERM.  DESTINATION        NOTE       MOD      LOC
-----    ----  -----  -----------        ----       -----    ---
MPS050   OT    305    9/2,12/2                      B5N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/2,1/3
                      1/8,4/1
                      4/3
MPS060   OT    206    4/14,9/3                      B6N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/11
MPS070   OT    107    9/3,12/2                      B7N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/1,1/3
                      1/8

MPS080   OT    013    4/13,9/3                      B8N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/13
MPS090   OT    313    9/3,12/2                      B9N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/1,1/3
                      1/8
MPS100   OT    015    4/13,9/3                      B10N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/11

MPS110   OT    315    9/3,12/2                      B11N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/1,1/3
                      1/8
MPS120   OT    216    4/12,9/3                      B12N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/13
MPS130   OT    117    9/3,12/2                      B13N
                      12/4,12/6
                      12/10,12/12
                      12/14,12/16
         I            1/1,1/3
                      1/8

MPS140   OT    018    4/12,9/2                      B14N
                      12/2,12/4
                      12/6,12/10
                      12/12,12/14
                      12/16
         I            1/5,1/11
MPS150   OT    219    9/3,12/2                      B15N
```

PART OF FS 12
SYMBOL(S) 7 8

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01	B12CD

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06/10/77

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 8 (CONT)

MICROSTORE
(PLANE 0,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP0.0	02-36	(NOTE 216)	A	

-------------------- FS INFO -------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			12/4,12/6			
			12/10,12/12			
			12/14,12/16			
	I		1/1,1/3			
			1/8			
PL.SL00	1	112	1/2		PSH	
3T058C	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0236B	GRD	004	(2)12/8			
	GRD	007	(2)12/8			
	GRD	008	(2)12/8			
	GRD	102	(2)12/8			
	GRD	103	(2)12/8			
	GRD	105	(2)12/8			
	GRD	106	(2)12/8			
	GRD	200	(2)12/8		GRD	
	GRD	202	(2)12/8			
	GRD	204	(2)12/8			
	GRD	205	(2)12/8			
	GRD	303	(2)12/8			
	GRD	306	(2)12/8			
	GRD	307	(2)12/8			
	GRD	207				
3VG0236T	GRD	014	(2)12/8			
	GRD	017	(2)12/8			
	GRD	019	(2)12/8			
	GRD	113	(2)12/8			
	GRD	114	(2)12/8			
	GRD	115	(2)12/8			
	GRD	116	(2)12/8			
	GRD	118	(2)12/8			
	GRD	212	(2)12/8			
	GRD	213	(2)12/8			
	GRD	214	(2)12/8			
	GRD	215	(2)12/8			
	GRD	217	(2)12/8			
	GRD	218	(2)12/8			
	GRD	314	(2)12/8			
	GRD	316	(2)12/8			
	GRD	318	(2)12/8			
	GRD	319			GRD	
3V058C	PWR	000	(2)14/6	203	+3	
	PWR	119	(2)14/6	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061A	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

SYMBOL NO. 9

MICROSTORE
(PLANE 7,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP7.1	06-43	(NOTE 216)	A	

-------------------- FS INFO -------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MAR0010	I	208	1/3		A0	
MAR0110	I	308	1/3		A1	
MAR0210	I	111	1/3		A2	
MAR0310	I	110	1/3		A3	
~~MAR0410~~	~~I~~	~~309~~	~~1/3~~		~~A4~~	
MAR0510	I	010	1/2		A5	
MAR0610	I	011	1/2		A6	
MAR0710	I	209	1/2		A7	
MAR0810	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL60	I	312	1/2		PSL	
PL.SL70	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0643B	GRD	007	(2)12/9			
	GRD	008	(2)12/9			
	GRD	102	(2)12/9			
	GRD	103	(2)12/9			
	GRD	105	(2)12/9			
	GRD	106	(2)12/9			
	GRD	200	(2)12/9		GRD	
	GRD	202	(2)12/9			
	GRD	204	(2)12/9			
	GRD	205	(2)12/9			
	GRD	207	(2)12/9			
	GRD	303	(2)12/9			
	GRD	306	(2)12/9			
	GRD	307	(2)12/9			
	GRD	004				
3VG0643T	GRD	014	(2)12/9			
	GRD	017	(2)12/9			
	GRD	113	(2)12/9			
	GRD	114	(2)12/9			
	GRD	115	(2)12/9			
	GRD	116	(2)12/9			
	GRD	118	(2)12/9			
	GRD	212	(2)12/9			
	GRD	213	(2)12/9			
	GRD	214	(2)12/9			
	GRD	215	(2)12/9			
	GRD	217	(2)12/9			
	GRD	218	(2)12/9			
	GRD	314	(2)12/9			

SYMBOL NO. 9 (CONT)

MICROSTORE
(PLANE 7,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP7.1	06-43	(NOTE 216)	A	

-------------------- FS INFO -------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0643T	GRD	316	(2)12/9			
	GRD	318	(2)12/9			
	GRD	319	(2)12/9		GRD	
	GRD	019				
3V054F	~~PWR~~	~~000~~	~~(2)14/3~~	~~203~~	~~+3~~	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001	14/26	203	+5	
	PWR	100	14/26	203	+5	
	PWR	101	14/26	203	+5	
	PWR	201	14/26	203	+5	
	PWR	300	14/26	203	+5	
	PWR	301	14/26	203	+5	
5V061D	PWR	001	(2)14/28	203	+5	
	PWR	100	(2)14/28	203	+5	
	PWR	101	(2)14/28	203	+5	
	PWR	201	(2)14/28	203	+5	
	PWR	300	(2)14/28	203	+5	
	PWR	301	(2)14/28	203	+5	

SYMBOL NO. 10

MICROSTORE
(PLANE 7,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP7.0	02-43	(NOTE 216)	A	

-------------------- FS INFO -------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MAR0010	1	208	1/3		A0	
MAR0110	I	308	1/3		A1	
MAR0210	I	111	1/3		A2	
MAR0310	I	110	1/3		A3	
MAR0410	I	309	1/3		A4	
MAR0510	I	010	1/2		A5	
MAR0610	I	011	1/2		A6	
MAR0710	1	209	1/2		A7	
MAR0810	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	
MPS140	OT	018	12/8		B14N	

SYMBOL NO. 10 (CONT)

MICROSTORE
(PLANE 7,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP7.0	02-43	(NOTE 216)	A	

-------------------- FS INFO -------------------- ---- CP INFO -----

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MPS150	OT	219	12/8		B15N	
PL.SL60	I	312	1/2		PSL	
PL.SL70	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0243B	GRD	004	(2)12/10			
	GRD	007	(2)12/10			
	GRD	102	(2)12/10			
	GRD	103	(2)12/10			
	GRD	105	(2)12/10			
	GRD	106	(2)12/10			
	GRD	200	(2)12/10		GRD	
	GRD	202	(2)12/10			
	GRD	204	(2)12/10			
	GRD	205	(2)12/10			
	GRD	207	(2)12/10			
	GRD	303	(2)12/10			
	GRD	306	(2)12/10			
	GRD	307	(2)12/10			
	GRD	008				
3VG0243T	GRD	014	(2)12/10			
	GRD	017	(2)12/10			
	GRD	019	(2)12/10			
	GRD	113	(2)12/10			
	GRD	114	(2)12/10			
	GRD	115	(2)12/10			
	GRD	116	(2)12/10			
	GRD	118	(2)12/10			
	GRD	212	(2)12/10			
	GRD	213	(2)12/10			
	GRD	214	(2)12/10			
	GRD	217	(2)12/10			
	GRD	218	(2)12/10			
	GRD	314	(2)12/10			
	GRD	316	(2)12/10			
	GRD	318	(2)12/10			
	GRD	319	(2)12/10		GRD	
	GRD	215				
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001	14/26	203	+5	
	PWR	100	14/26	203	+5	
	PWR	101	14/26	203	+5	
	PWR	201	14/26	203	+5	
	PWR	300	14/26	203	+5	

PART OF FS 12
SYMBOL(S) 8 9 10

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	6D

BELL LABORATORIES | SD-1C900-01 | B12CE

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06/10/77

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 10 (CONT)

MICROSTORE
(PLANE 7,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP7.0	02-43	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
5V061C	PWR	301	14/26	203	+5	
5V061D	PWR	001	(2)14/28	203	+5	
	PWR	100	(2)14/28	203	+5	
	PWR	101	(2)14/28	203	+5	
	PWR	201	(2)14/28	203	+5	
	PWR	300	(2)14/28	203	+5	
	PWR	301	(2)14/28	203	+5	

SYMBOL NO. 11

MICROSTORE
(PLANE 6,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP6.1	06-42	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		312			PSL	
MAR001D	I	208	1/3		A0	
MAR011D	I	308	1/3		A1	
MAR021D	I	111	1/3		A2	
MAR031D	I	110	1/3		A3	
MAR041D	I	309	1/3		A4	
MAR051D	I	010	1/2		A5	
MAR061D	I	011	1/2		A6	
MAR071D	I	209	1/2		A7	
MAR081D	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL60	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0642B	GRD	004	(2)12/11			
	GRD	007	(2)12/11			
	GRD	008	(2)12/11			
	GRD	102	(2)12/11			
	GRD	103	(2)12/11			

SYMBOL NO. 11 (CONT)

MICROSTORE
(PLANE 6,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP6.1	06-42	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0642B	GRD	105	(2)12/11			
	GRD	106	(2)12/11			
	GRD	200	(2)12/11		GRD	
	GRD	202	(2)12/11			
	GRD	204	(2)12/11			
	GRD	205	(2)12/11			
	GRD	207	(2)12/11			
	GRD	303	(2)12/11			
	GRD	306	(2)12/11			
	GRD	307				
3VG0642T	GRD	014	(2)12/11			
	GRD	017	(2)12/11			
	GRD	019	(2)12/11			
	GRD	113	(2)12/11			
	GRD	115	(2)12/11			
	GRD	116	(2)12/11			
	GRD	118	(2)12/11			
	GRD	212	(2)12/11			
	GRD	213	(2)12/11			
	GRD	214	(2)12/11			
	GRD	215	(2)12/11			
	GRD	217	(2)12/11			
	GRD	218	(2)12/11			
	GRD	314	(2)12/11			
	GRD	316	(2)12/11			
	GRD	318	(2)12/11			
	GRD	319	(2)12/11		GRD	
	GRD	114				
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001	14/26	203	+5	
	PWR	100	14/26	203	+5	
	PWR	101	14/26	203	+5	
	PWR	201	14/26	203	+5	
	PWR	300	14/26	203	+5	
	PWR	301	14/26	203	+5	
5V061D	PWR	001	(2)14/28	203	+5	
	PWR	100	(2)14/28	203	+5	
	PWR	101	(2)14/28	203	+5	
	PWR	201	(2)14/28	203	+5	
	PWR	300	(2)14/28	203	+5	
	PWR	301	(2)14/28	203	+5	

SYMBOL NO. 12

MICROSTORE
(PLANE 6,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP6.0	02-42	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		312			PSL	
MAR001D	I	208	1/3		A0	
MAR011D	I	308	1/3		A1	
MAR021D	I	111	1/3		A2	
MAR031D	I	110	1/3		A3	
MAR041D	I	309	1/3		A4	
MAR051D	I	010	1/2		A5	
MAR061D	I	011	1/2		A6	
MAR071D	I	209	1/2		A7	
MAR081D	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	
MPS140	OT	018	12/8		B14N	
MPS150	OT	219	12/8		B15N	
PL.SL60	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0242B	GRD	004	(2)12/12			
	GRD	007	(2)12/12			
	GRD	008	(2)12/12			
	GRD	102	(2)12/12			
	GRD	103	(2)12/12			
	GRD	105	(2)12/12			
	GRD	106	(2)12/12			
	GRD	200	(2)12/12		GRD	
	GRD	202	(2)12/12			
	GRD	204	(2)12/12			
	GRD	205	(2)12/12			
	GRD	207	(2)12/12			
	GRD	306	(2)12/12			
	GRD	307	(2)12/12			
	GRD	303				
3VG0242T	GRD	014	(2)12/12			
	GRD	017	(2)12/12			
	GRD	019	(2)12/12			
	GRD	114	(2)12/12			
	GRD	115	(2)12/12			
	GRD	116	(2)12/12			
	GRD	118	(2)12/12			
	GRD	212	(2)12/12			
	GRD	213	(2)12/12			
	GRD	214	(2)12/12			
	GRD	215	(2)12/12			
	GRD	217	(2)12/12			
	GRD	218	(2)12/12			
	GRD	314	(2)12/12			

SYMBOL NO. 12 (CONT)

MICROSTORE
(PLANE 6,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP6.0	02-42	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0242T	GRD	316	(2)12/12			
	GRD	318	(2)12/12			
	GRD	319	(2)12/12		GRD	
	GRD	113				
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001	14/26	203	+5	
	PWR	100	14/26	203	+5	
	PWR	101	14/26	203	+5	
	PWR	201	14/26	203	+5	
	PWR	300	14/26	203	+5	
	PWR	301	14/26	203	+5	
5V061D	PWR	001	(2)14/28	203	+5	
	PWR	100	(2)14/28	203	+5	
	PWR	101	(2)14/28	203	+5	
	PWR	201	(2)14/28	203	+5	
	PWR	300	(2)14/28	203	+5	
	PWR	301	(2)14/28	203	+5	

PART OF FS 12
SYMBOL(S) 10 11 12

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01		B12CF

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PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 13

MICROSTORE
(PLANE 5,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP5.1	06-41	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
MAR001C	I	208	1/3		A0	
MAR011C	I	308	1/3		A1	
MAR021C	I	111	1/3		A2	
MAR031C	I	110	1/3		A3	
MAR041C	I	309	1/3		A4	
MAR051C	I	010	1/2		A5	
MAR061C	I	011	1/2		A6	
MAR071C	I	209	1/2		A7	
MAR081C	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL40	I	312	1/2		PSL	
PL.SL50	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0641B	GRD	004	(2)12/13			
	GRD	007	(2)12/13			
	GRD	008	(2)12/13			
	GRD	102	(2)12/13			
	GRD	103	(2)12/13			
	GRD	105	(2)12/13			
	GRD	106	(2)12/13			
	GRD	200	(2)12/13		GRD	
	GRD	204	(2)12/13			
	GRD	205	(2)12/13			
	GRD	207	(2)12/13			
	GRD	303	(2)12/13			
	GRD	306	(2)12/13			
	GRD	307	(2)12/13			
	GRD	202				
3VG0641T	GRD	014	(2)12/13			
	GRD	017	(2)12/13			
	GRD	019	(2)12/13			
	GRD	113	(2)12/13			
	GRD	114	(2)12/13			
	GRD	115	(2)12/13			
	GRD	116	(2)12/13			
	GRD	118	(2)12/13			
	GRD	212	(2)12/13			
	GRD	213	(2)12/13			
	GRD	214	(2)12/13			
	GRD	215	(2)12/13			
	GRD	217	(2)12/13			
	GRD	218	(2)12/13			

SYMBOL NO. 13 (CONT)

MICROSTORE
(PLANE 5,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP5.1	06-41	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
3VG0641T	GRD	314	(2)12/13			
	GRD	316	(2)12/13			
	GRD	318	(2)12/13			
	GRD	319			GRD	
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

SYMBOL NO. 14

MICROSTORE
(PLANE 5,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP5.0	02-41	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
MAR001C	I	208	1/3		A0	
MAR011C	I	308	1/3		A1	
MAR021C	I	111	1/3		A2	
MAR031C	I	110	1/3		A3	
MAR041C	I	309	1/3		A4	
MAR051C	I	010	1/2		A5	
MAR061C	I	011	1/2		A6	
MAR071C	I	209	1/2		A7	
MAR081C	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	
MPS140	OT	018	12/8		B14N	
MPS150	OT	219	12/8		B15N	
PL.SL40	I	312	1/2		PSL	
PL.SL50	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	

SYMBOL NO. 14 (CONT)

MICROSTORE
(PLANE 5,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP5.0	02-41	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	**FUNC**	**TERM.**	**DESTINATION**	**NOTE**	**TERM. MOD**	**LOC**
3T054F	GRD	319		203	GRD	
3VG0241B	GRD	004	(2)12/14			
	GRD	007	(2)12/14			
	GRD	008	(2)12/14			
	GRD	102	(2)12/14			
	GRD	103	(2)12/14			
	GRD	105	(2)12/14			
	GRD	200	(2)12/14		GRD	
	GRD	202	(2)12/14			
	GRD	204	(2)12/14			
	GRD	205	(2)12/14			
	GRD	207	(2)12/14			
	GRD	303	(2)12/14			
	GRD	306	(2)12/14			
	GRD	307	(2)12/14			
	GRD	106				
3VG0241T	GRD	014	(2)12/14			
	GRD	017	(2)12/14			
	GRD	019	(2)12/14			
	GRD	113	(2)12/14			
	GRD	114	(2)12/14			
	GRD	115	(2)12/14			
	GRD	116	(2)12/14			
	GRD	118	(2)12/14			
	GRD	212	(2)12/14			
	GRD	213	(2)12/14			
	GRD	214	(2)12/14			
	GRD	215	(2)12/14			
	GRD	217	(2)12/14			
	GRD	218	(2)12/14			
	GRD	314	(2)12/14			
	GRD	318	(2)12/14			
	GRD	319	(2)12/14		GRD	
	GRD	316				
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

PART OF FS 12
SYMBOL(S) 13 14

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01		B12CG

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06/10/77

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

SYMBOL NO. 15

MICROSTORE
(PLANE 4,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP4.1	06-40	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		312			PSL	
MAR001C	I	208	1/3		A0	
MAR011C	I	308	1/3		A1	
MAR021C	I	111	1/3		A2	
MAR031C	I	110	1/3		A3	
MAR041C	I	309	1/3		A4	
MAR051C	I	010	1/2		A5	
MAR061C	I	011	1/2		A6	
MAR071C	I	209	1/2		A7	
MAR081C	I	012	1/2		A8	
MPS160	OT	002	12/7		B0N	
MPS170	OT	302	12/7		B1N	
MPS180	OT	203	12/7		B2N	
MPS190	OT	104	12/7		B3N	
MPS200	OT	005	12/7		B4N	
MPS210	OT	305	12/7		B5N	
MPS220	OT	206	12/7		B6N	
MPS230	OT	107	12/7		B7N	
MPS240	OT	013	12/7		B8N	
MPS250	OT	313	12/7		B9N	
MPS260	OT	015	12/7		B10N	
MPS270	OT	315	12/7		B11N	
MPS280	OT	216	12/7		B12N	
MPS290	OT	117	12/7		B13N	
MPS300	OT	018	12/7		B14N	
MPS310	OT	219	12/7		B15N	
PL.SL40	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
3VG0640B	GRD	004	(2)12/15			
	GRD	007	(2)12/15			
	GRD	008	(2)12/15			
	GRD	102	(2)12/15			
	GRD	103	(2)12/15			
	GRD	105	(2)12/15			
	GRD	106	(2)12/15			
	GRD	200	(2)12/15		GRD	
	GRD	202	(2)12/15			
	GRD	205	(2)12/15			
	GRD	207	(2)12/15			
	GRD	303	(2)12/15			
	GRD	306	(2)12/15			
	GRD	307	(2)12/15			
	GRD	204				
3VG0640T	GRD	014	(2)12/15			
	GRD	017	(2)12/15			
	GRD	019	(2)12/15			
	GRD	113	(2)12/15			
	GRD	114	(2)12/15			
	GRD	115	(2)12/15			
	GRD	116	(2)12/15			
	GRD	118	(2)12/15			
	GRD	213	(2)12/15			
	GRD	214	(2)12/15			
	GRD	215	(2)12/15			
	GRD	217	(2)12/15			
	GRD	218	(2)12/15			
	GRD	314	(2)12/15			

SYMBOL NO. 15 (CONT)

MICROSTORE
(PLANE 4,MOD 1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP4.1	06-40	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3VG0640T	GRD	316	(2)12/15			
	GRD	318	(2)12/15			
	GRD	319	(2)12/15		GRD	
	GRD	212				
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

SYMBOL NO. 16

MICROSTORE
(PLANE 4,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP4.0	02-40	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		312			PSL	
MAR001C	I	208	1/3		A0	
MAR011C	I	308	1/3		A1	
MAR021C	I	111	1/3		A2	
MAR031C	I	110	1/3		A3	
MAR041C	I	309	1/3		A4	
MAR051C	I	010	1/2		A5	
MAR061C	I	011	1/2		A6	
MAR071C	I	209	1/2		A7	
MAR081C	I	012	1/2		A8	
MPS000	OT	002	12/8		B0N	
MPS010	OT	302	12/8		B1N	
MPS020	OT	203	12/8		B2N	
MPS030	OT	104	12/8		B3N	
MPS040	OT	005	12/8		B4N	
MPS050	OT	305	12/8		B5N	
MPS060	OT	206	12/8		B6N	
MPS070	OT	107	12/8		B7N	
MPS080	OT	013	12/8		B8N	
MPS090	OT	313	12/8		B9N	
MPS100	OT	015	12/8		B10N	
MPS110	OT	315	12/8		B11N	
MPS120	OT	216	12/8		B12N	
MPS130	OT	117	12/8		B13N	
MPS140	OT	018	12/8		B14N	
MPS150	OT	219	12/8		B15N	
PL.SL40	I	112	1/2		PSH	
3T054F	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	

SYMBOL NO. 16 (CONT)

MICROSTORE
(PLANE 4,MOD 0)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
MP4.0	02-40	(NOTE 216)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T054F	GRD	319		203	GRD	
3VG0240B	GRD	007	(2)12/16			
	GRD	008	(2)12/16			
	GRD	102	(2)12/16			
	GRD	103	(2)12/16			
	GRD	105	(2)12/16			
	GRD	106	(2)12/16			
	GRD	200	(2)12/16		GRD	
	GRD	202	(2)12/16			
	GRD	204	(2)12/16			
	GRD	205	(2)12/16			
	GRD	207	(2)12/16			
	GRD	303	(2)12/16			
	GRD	306	(2)12/16			
	GRD	307	(2)12/16			
	GRD	004				
3VG0240T	GRD	017	(2)12/16			
	GRD	019	(2)12/16			
	GRD	113	(2)12/16			
	GRD	114	(2)12/16			
	GRD	115	(2)12/16			
	GRD	116	(2)12/16			
	GRD	118	(2)12/16			
	GRD	212	(2)12/16			
	GRD	213	(2)12/16			
	GRD	214	(2)12/16			
	GRD	215	(2)12/16			
	GRD	217	(2)12/16			
	GRD	218	(2)12/16			
	GRD	314	(2)12/16			
	GRD	316	(2)12/16			
	GRD	318	(2)12/16			
	GRD	319	(2)12/16		GRD	
	GRD	014				
3V054F	PWR	000	(2)14/3	203	+3	
	PWR	119	(2)14/3	203	+3	
3V058F	PWR	000	14/6	203	+3	
	PWR	119	14/6	203	+3	
5V061C	PWR	001		203	+5	
	PWR	100		203	+5	
	PWR	101		203	+5	
	PWR	201		203	+5	
	PWR	300		203	+5	
	PWR	301		203	+5	

PART OF FS 12
SYMBOL(S) 15 16

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 6D
BELL LABORATORIES	SD-1C900-01		B12CH

PRINTED IN U. S. A.

06/10/77

PART OF FS 12

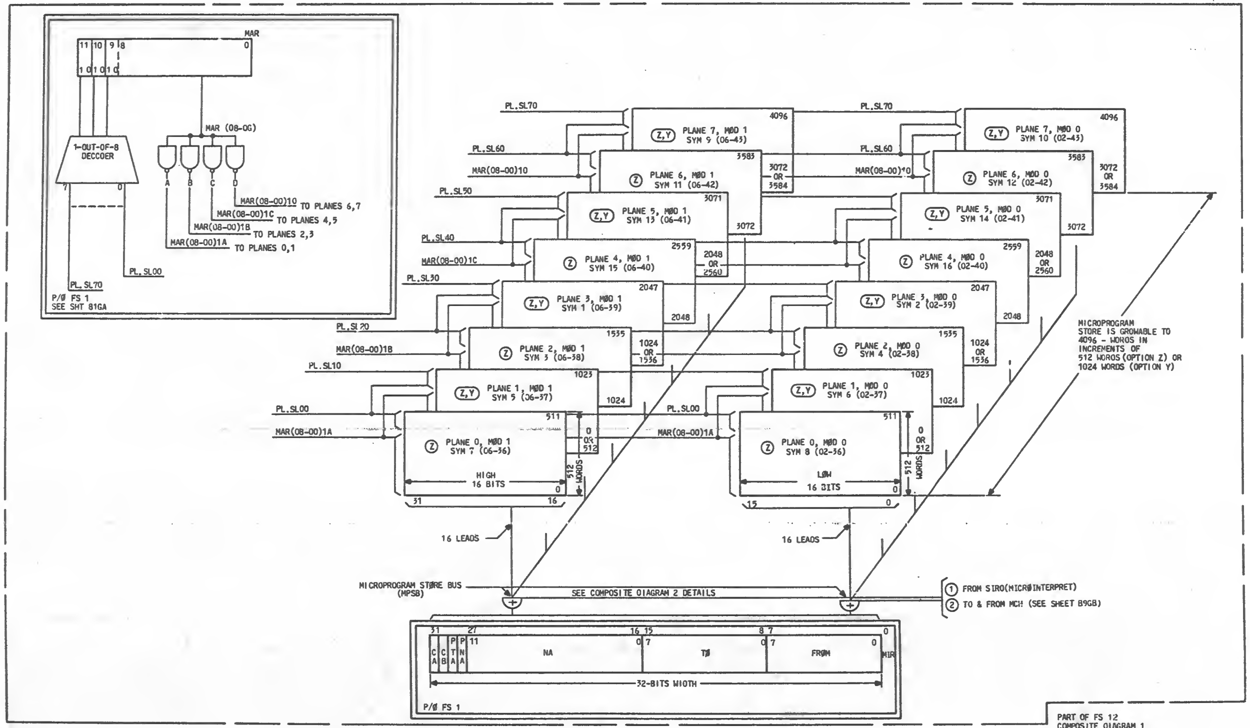
MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

COMPOSITE DIAGRAM 1

MICROPROGRAM STORE ORGANIZATION

CIRCUIT OPERATION

(SEE SHEET B12GB)



MAR
11 10 9 8
0
1 0 1 0
1-OUT-OF-8 DECODER
7
0
MAR (08-00)
A B C D
MAR(08-00)10 TO PLANES 6,7
MAR(08-00)1C TO PLANES 4,5
MAR(08-00)1B TO PLANES 2,3
MAR(08-00)1A TO PLANES 0,1
PL.SL70
PL.SL00
P/Ø FS 1 SEE SHT B1GA
PL.SL70
PL.SL60
MAR(08-00)10
PL.SL50
PL.SL40
MAR(08-00)1C
PL.SL30
PL.SL20
MAR(08-00)1B
PL.SL10
PL.SL00
MAR(08-00)1A
Z,Y PLANE 7, MØD 1 SYM 9 (06-43)
4096
Z PLANE 6, MØD 1 SYM 11 (06-42)
3583
3072 OR 3584
Z,Y PLANE 5, MØD 1 SYM 13 (06-41)
3071
3072
Z PLANE 4, MØD 1 SYM 15 (06-40)
2559
2048 OR 2560
Z,Y PLANE 3, MØD 1 SYM 1 (06-39)
2047
2048
Z PLANE 2, MØD 1 SYM 3 (06-38)
1535
1024 OR 1536
Z,Y PLANE 1, MØD 1 SYM 5 (06-37)
1023
1024
Z PLANE 0, MØD 1 SYM 7 (06-36)
511
0 OR 512
HIGH 16 BITS
512 WORDS
31 16 0
PL.SL70
PL.SL60
MAR(08-00)10
Z,Y PLANE 7, MØD 0 SYM 10 (02-43)
4096
Z PLANE 6, MØD 0 SYM 12 (02-42)
3583
3072 OR 3584
Z,Y PLANE 5, MØD 0 SYM 14 (02-41)
3071
3072
Z PLANE 4, MØD 0 SYM 16 (02-40)
2559
2048 OR 2560
Z,Y PLANE 3, MØD 0 SYM 2 (02-39)
2047
2048
Z PLANE 2, MØD 0 SYM 4 (02-38)
1535
1024 OR 1536
Z,Y PLANE 1, MØD 0 SYM 6 (02-37)
1023
1024
PL.SL00
MAR(08-00)1A
Z PLANE 0, MØD 0 SYM 8 (02-36)
511
0 OR 512
LØW 16 BITS
512 WORDS
15 0
MICROPROGRAM STORE IS GROWABLE TO 4096 - WORDS IN INCREMENTS OF 512 WORDS (OPTION Z) OR 1024 WORDS (OPTION Y)
16 LEADS
16 LEADS
MICROPROGRAM STØRE BUS (MPSB)
SEE COMPOSITE DIAGRAM 2 DETAILS
① FROM SIRO(MICRØINTERPRET)
② TO & FROM MCH (SEE SHEET B9GB)
31 27 16 15 8 7 0
C A
C B
P T A
P N A
11 0 7 0 7 0
NA
TØ
FRØM
MIR
32-BITS WIDTH
P/Ø FS 1

PART OF FS 12
COMPOSITE DIAGRAM 1

3A CENTRAL CONTROL	DWG SIZE	ISSUE
	6S	6D
BELL LABORATORIES — SD-1C900-01		B12GA

E-7025 (12-73)

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PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

CIRCUIT OPERATION

THE MICROPROGRAM STORE CONTAINS THE BASIC CONTROL AND SEQUENCING INFORMATION FOR THE 3A CC. IT CONTAINS THE CONTROL AND SEQUENCING INFORMATION FOR THE FOLLOWING FUNCTIONS:

(1) THE INSTRUCTION SET FOR THE LANGUAGE OR LANGUAGES TO BE USED FOR THE 3A CC.

(2) THE INITIALIZATION SEQUENCES TO BE INVOKED IN THE EVENT AN ERROR OCCURS OR A RESTART IS REQUIRED.

(3) THE INTERRUPT SEQUENCING CONTROL THAT PROVIDES THE INTERPRETATION OF WHAT INTERRUPT HAS OCCURRED AND WHAT FUNCTION IS TO TAKE PLACE.

(4) THE CONTROL NECESSARY TO PERFORM THE 3A CC CONTROL PANEL FUNCTIONS.

(5) IN SOME APPLICATIONS THE MICROPROGRAM CONTROL CONTAINS SPECIAL CONTROL FUNCTIONS THAT ARE ROUTINELY AND FREQUENTLY EXECUTED AND THEREFORE ARE MICROCODED. THE EMULATION OF THE NO. 2 ESS WIRED LOGIC I/Ø UNIT IS AN EXAMPLE OF THIS.

THE MICROPROGRAM STORE CONSISTS OF A MAXIMUM OF 4K (K=1024) 32-BIT WIDTH WORDS THAT ARE READ-ONLY. THAT IS, THE CONTENTS OF THE MICROPROGRAM STORE ARE NOT ALTERABLE WHEN IN THE 3A CC. THE MEMORY IS GROWABLE IN 512(Z) OR 1024(Y) BY 32-WORD BLOCKS. THE 512- OR 1024-WORD BLOCK CONSISTS OF TWO CIRCUIT PACKS WITH ONE PACK CONTAINING THE LOW 16 BITS AND THE OTHER CONTAINING THE HIGH 16 BITS OF EACH WORD. EACH BLOCK IS SELECTED BY ONE(Z) OR TWO(Y) PLANE SELECT LEADS. THE PLANE SELECT LEAD IS DECODED FROM THE HIGH THREE BITS OF THE MAR REGISTER. THE LOW NINE BITS OF THE MAR REGISTER, BITS 0-8, ARE OUTPUTTED DIRECTLY TO THE MICROPROGRAM STORE AND THEY ARE DECODED WITHIN THE MICROPROGRAM STORE CIRCUIT PACKS, AS INDICATED IN COMPOSITE DIAGRAM 1. WHEN A WORD IS ACCESSED FROM THE MICROPROGRAM STORE, IT IS "OR"ED ONTO A COMMON OUTPUT BUS CALLED THE MICROPROGRAM STORE BUS (MPSB) DESIGNATED BY THE NETNAMES MPS(31-00)0. THE OUTPUT OF THE MPSB IS MAPPED INTO THE MIR REGISTER. THE MAPPING OF THE MICROPROGRAM STORE OUTPUT IS SHOWN IN COMPOSITE DIAGRAM 2. NOTE THAT THE MIR REGISTER IS 32 BITS IN WIDTH, WITH THE FROM FIELD CONTAINED IN BITS 0-7, THE TO FIELD IN BITS 8-15, THE NEXT ADDRESS FIELD, IN BITS 8-27, AND THE TWO PARITY BITS PNA AND PTA AND THE TWO CONTROL BITS CB AND CA IN THE UPPER FOUR BITS, RESPECTIVELY. THE MAPPING OF THE 32-BIT OUTPUT OF THE MICROPROGRAM STORE, 0-31, IS NOT DIRECT INTO BITS 0-31 OF THE MIR. THE MAPPING OF THE BITS IS SCRAMBLED IN ORDER TO MAXIMIZE THE FAULT DETECTION CAPABILITY OF THE VARIOUS CODING TECHNIQUES USED IN THE TO, FROM, AND NEXT ADDRESS FIELDS IMPLEMENTED IN THE MICROPROGRAM STORE. THE FROM FIELD, IN FACT, IS CONTAINED IN EVERY FOURTH BIT POSITION OF THE MICROPROGRAM STORE OUTPUT. THE TO FIELD IS ALSO IN EVERY FOURTH BIT POSITION OF THE MICROPROGRAM STORE OUTPUT . WITH EACH OCCURRENCE OF ITS OUTPUT BEING 2 BIT POSITIONS AWAY FROM THE CORRESPONDING BIT POSITION OF THE FROM FIELD. THEN INTERLEAVED BETWEEN EACH ADJACENT POSITION OF THE TO- AND FROM-FIELD BIT POSITION IS THE NEXT ADDRESS FIELD, TOGETHER WITH THE TWO PARITY BITS AND THE TWO CONTROL BITS. THE TO AND FROM FIELDS ARE ENCODED WITH 4-OUT-OF-8 CODES AND 4-OUT-OF-8 CODES WILL DETECT ALL MULTIPLE UNIDIRECTIONAL ERRORS. THE NEXT ADDRESS FIELD USES ONLY A PARITY CHECK CODE WHICH WILL DETECT ONLY SINGLE-BIT ERRORS AND SOME MULTIPLE ERRORS. THEREFORE, IF A MULTIPLE ERROR OCCURS AND IT AFFECTS TWO BITS IN THE PARITY CHECK FIELD, BECAUSE OF THE INTERLEAVING. IT WILL TEND TO AFFECT EITHER A TO FIELD OR FROM FIELD. IN THIS WAY AN ERROR THAT MIGHT OTHERWISE BE UNDETECTED BY THE PARITY CHECK ON THE NEXT ADDRESS FIELD WILL BE DETECTED BY THE MORE POWERFULL 4-OUT-OF-8 CODE ON THE TO AND FROM FIELDS.

THE CORRESPONDING BIT POSITIONS OF EACH OF THE PLANES OF THE MICROPROGRAM STORE (PLANES 0-7) ARE COLLECTOR-TIED TOGETHER AT THE COMMON POINT. THIS COMMON POINT IS THE MPSB. IN ADDITION TO THE MICROPROGRAM STORE OUTPUT. TWO OTHER OUTPUTS ARE "OR"ED ONTO THE MPSB. THE FIRST IS THE OUTPUT OF SIRO WHICH "OR"S ONTO THE 16 MICROPROGRAM STORE OUTPUTS THAT INPUT INTO THE LOW 16 BITS OF THE MIR (i.e. THE TO AND FROM FIELDS). THIS GATING PATH ALLOWS MICROINSTRUCTIONS STORED IN THE MAIN STORE TO BE EXECUTED BY THE MICROCONTROL WITH VERY LITTLE ADDITIONAL CIRCUITRY. THAT IS, WHEN A CONTROL CONSTANT IS PLACED ON THE MPSB FROM SIRO, THE NORMAL CLOCKING INTO THE MIR AND SUBSEQUENT DECODING OF THE TO- AND FROM-FIELD DECODERS TAKES PLACE AS IF THE CONTROL CONSTANT HAD ORIGINATED FROM THE MICROSTORE ITSELF. SEE SHEET B1GH FOR ADDITIONAL DETAILS OF THIS

CIRCUIT OPERATION (CONT)

OPERATION WHICH IS REFERRED TO A MICROINTERPRET. THE SECOND SOURCE THAT OUTPUTS INTO THE MPSB IS THE MAINTENANCE CHANNEL (MCH). IN ADDITION TO OR'ING ONTO THE LOW 16 BITS OF THE INPUTS TO THE MIR, IT ALSO OR'S ONTO THE HIGH 16 BITS. THEREFORE, IN ADDITION TO BEING ABLE TO PERFORM MICROINSTRUCTIONS THAT ORIGINATE FROM THE MCH AND HENCE THE OTHER 3A CC, THE ABILTY IS PROVIDED FOR THE MCH TO LOAD ADDRESS INFORMATION INTO THE MIR. THIS PROVIDES THE ABILITY TO LOAD AN ARBITRARY ADDRESS INTO THE MAR. THIS CAPABILITY TOGETHER WITH THE FACT THAT THE MCH CAN READ THE CONTENTS OF THE MPSB ALLOWS THE MCH TO READ ALL LOCATIONS OF THE MICROPROGRAM STORE AND HENCE CHECK ITS VALIDITY.. THE MPSB FANOUT, IN ADDITION TO THE MIR AND THE MCH, TO THE " FAST MISCELLANEOUS DECODER" (SEE SHEET B1GK). NOTE ALSO THAT SOME BITS OF THE MIR ARE DUPLICATED FOR TIMING PURPOSES (CA AND CB BITS, SEE SHEET B1GB, B1GF AND B4GK) AND HENCE MPSB HAS ADDITIONAL FANOUT FOR THESE FUNCTIONS.

COMPOSITE DIAGRAM 2

MAPPING OF MICROSTORE OUTPUT TO MIR FUNCTION

TABLE OF MICROPROGRAM STORE
OUTPUT TRANSLATION
TO MIR FUNCTION

NETNAME	MICROPROGRAM STORE OUTPUT (PIN NO)		MIR FUNCTION	MIR BIT POSITION
MPS000	002	LEVEL 02 MICROSTORE CIRCUIT PACKS	FROM 0	00
MPS010	302		PTA	29
MPS020	203		TO 0	08
MPS030	104		CB	30
MPS040	005		FROM 1	01
MPS050	305		CA	31
MPS060	206		TO 1	09
MPS070	107		NA00	16
MPS080	013		FROM 2	02
MPS090	313		NA01	17
MPS100	015		TO 2	10
MPS110	315		NA02	18
MPS120	216		FROM 3	03
MPS130	117		NA03	19
MPS140	018		TO 3	11
MPS150	219		NA04	20
MPS160	002	LEVEL 06 MICROSTORE CIRCUIT PACKS	FROM 4	04
MPS170	302		NA05	21
MPS180	203		TO 4	12
MPS190	104		NA06	22
MPS200	005		FROM 5	05
MPS210	305		NA07	23
MPS220	206		TO 5	13
MPS230	107		NA08	24
MPS240	013		FROM 6	06
MPS250	313		NA09	25
MPS260	015		TO 6	14
MPS270	315		NA10	26
MPS280	216		FROM 7	07
MPS290	117		NA11	27
MPS300	018		TO 7	15
MPS310	219		PNA	28

PART OF FS 12
COMPOSITE DIAGRAM 2

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 6D
BELL LABORATORIES	SD-1C900-01	B12GB

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PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

Ⓩ COMPOSITE DIAGRAM 3

FUNCTION DIAGRAM OF A MICROPROGRAM
STORE PLANE WITH 512 WORDS
(SEE NOTE 2)

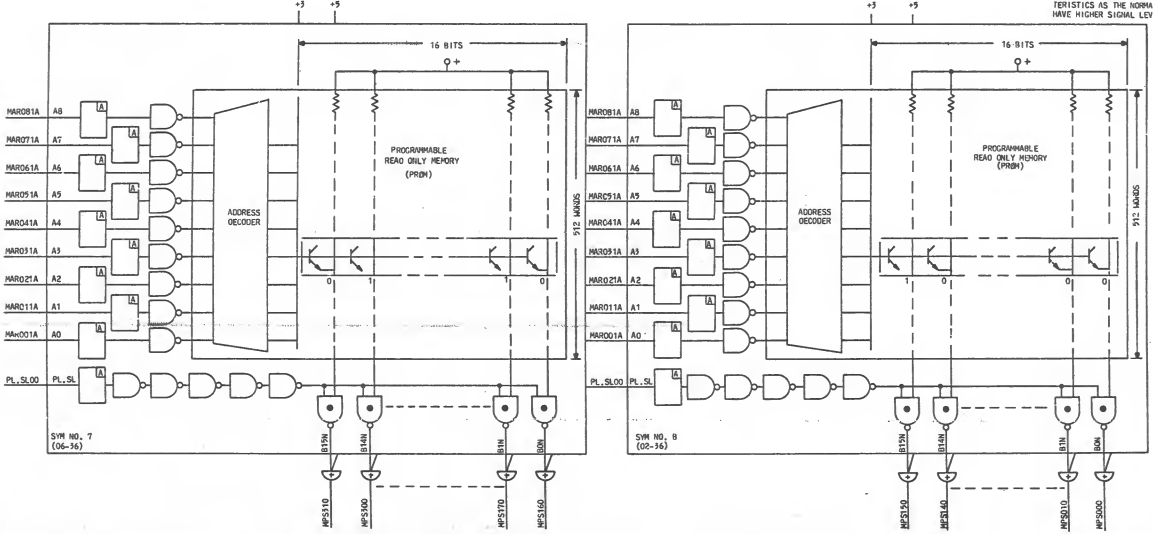
CIRCUIT OPERATION

COMPOSITE DIAGRAM 3 SHOWS THE BASIC LOGIC OPERATION OF THE MICROPROGRAM STORE PACKS THEMSELVES. THEY CONSIST OF A PROGRAMMABLE READ ONLY ARRAY COMPOSED OF FUSES IN THE EMITTER LEG OF A TRANSISTOR. THEY ARE EITHER OPENED OR SHORTED DEPENDING UPON WHETHER 1 OR 0 IS STORED IN THAT BIT POSITION. THE ADDRESS SELECTION OF A GIVEN READ ONLY MEMORY WORD IS PERFORMED BY DECODING BITS 0-8 OF THE MAR REGISTER WITHIN THE MICROPROGRAM STORE PACK. THIS WILL SELECT 1 OF 512 WORDS WITHIN A MICROPROGRAM STORE PACK. A PLANE SELECT LEAD IS THEN USED TO ENABLE THE OUTPUT OF THE TWO PACKS, ONE FOR BITS 0-15 AND THE OTHER FOR BITS 16-31. THE PLANE SELECT LEAD IS GENERATED BY DECODING BITS 9-11 OF THE MAR WITHIN THE MICROCONTROL AND SENDING A 1-OUT-OF-8 PLANE SELECT SIGNAL TO THE MICROPROGRAM STORE PACKS.

NOTE THAT ALL OF THE GATES WITHIN THE MICROPROGRAM STORE PACKS ARE 5-VOLT T^2L GATES WITH THE SAME BASIC CHARACTERISTICS AS THE NORMAL 3-VOLT 1A GATE. HOWEVER THEY HAVE HIGHER SIGNAL LEVEL THRESHOLDS AND THEREFORE AN

CIRCUIT OPERATION (CONT)

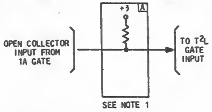
INTERFACE CIRCUIT IS REQUIRED WHEN GOING FROM THE 1A GATE TO THE T^2L GATE. THE LOGIC LEVELS FOR THE 1A GATE VARY FROM ABOUT 100 TO 250 MILLIVOLTS FOR A ZERO LEVEL TO 1 TO 1.2 VOLTS FOR A ONE LEVEL. THIS COMPARES WITH 400 TO 800 MILLIVOLTS FOR A ZERO LEVEL AND 2.5 TO 4.0 VOLTS FOR A ONE LEVEL T^2L GATE. THE ONLY TIMING REQUIREMENT ON THE MICROPROGRAM STORE IS THAT THE DATA BE STABLE AT ITS OUTPUT IN APPROXIMATELY 65ns AFTER THE ADDRESS LEADS HAVE BECOME STABLE AT ITS INPUT. ALSO, THE MICROPROGRAM STORE CANNOT CHANGE STATE WITHIN 25ns FOLLOWING THE CHANGE OF STATE OF THE ADDRESS LEADS AT ITS INPUT. FOR ADDITIONAL TIMING INFORMATION ON THE MICROPROGRAM STORE AND THE ASSOCIATED MICROCONTROL, SEE FS 1.



NOTES:

1. THIS BOX REPRESENTS A SPECIAL INTERFACE BETWEEN THE 1A LOGIC USED IN THE 3A CC AND T^2L LOGIC USED ON THE MICROSTORE PACKS.

2. FOR A DETAILED DESCRIPTION OF A MICROPROGRAM STORE PLANE SEE SD-4C005-01.



PART OF FS 12
COMPOSITE DIAGRAM 3

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 6D
BELL LABORATORIES	SD-1C900-01	B12GC

PART OF FS 12

MICROPROGRAM STORE
(4096 X 32-BIT WORDS)

Ⓨ COMPOSITE DIAGRAM 4

FUNCTION DIAGRAM OF A MICROPROGRAM
STORE PLANE WITH 1024 WORDS
(SEE NOTE 1)

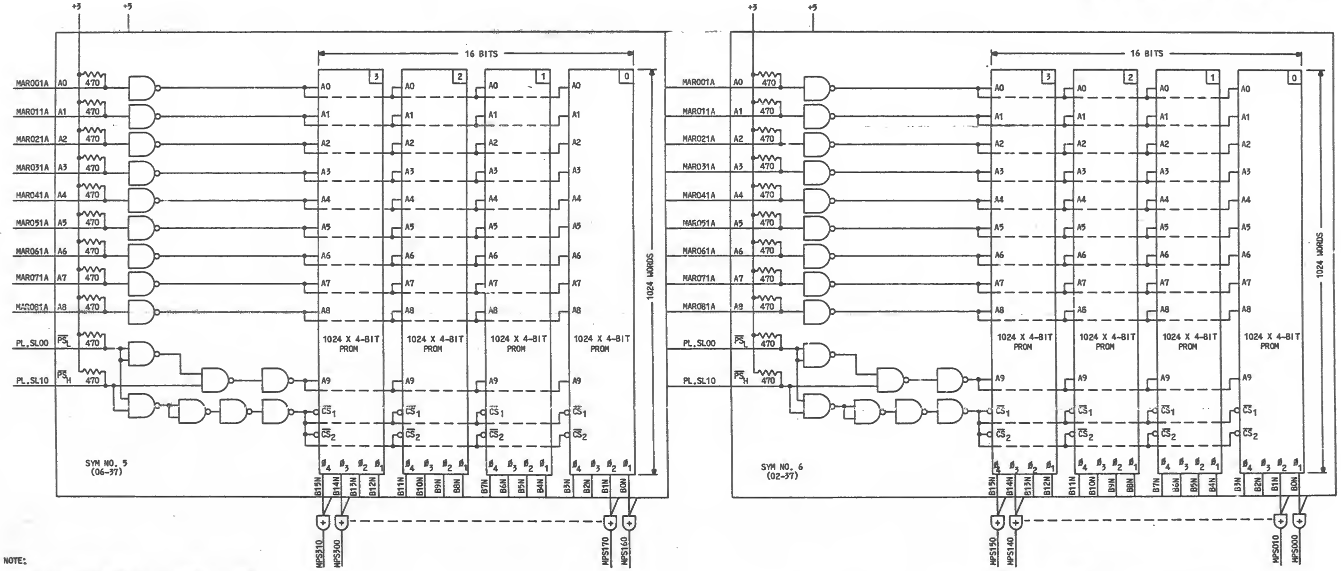
CIRCUIT OPERATION

COMPOSITE DIAGRAM 4 SHOWS THE BASIC LOGIC OPERATION OF THE MICROPROGRAM STORE PACKS THEMSELVES. THEY CONSIST OF A PROGRAMMABLE READ ONLY ARRAY COMPOSED OF FUSES IN THE EMITTER LEG OF A TRANSISTOR. THEY ARE EITHER OPENED OR SHORTED DEPENDING UPON WHETHER 1 OR 0 IS STORED IN THAT BIT POSITION. THE ADDRESS SELECTION OF A GIVEN READ ONLY MEMORY WORD IS PERFORMED BY DECODING BITS 0-8 OF THE MAR REGISTER WITHIN THE MICROPROGRAM STORE PACK. THIS WILL SELECT 1 OF 1024 WORDS WITHIN A MICROPROGRAM STORE PACK. TWO PLANE SELECT LEADS ARE THEN USED TO ENABLE THE OUTPUT OF THE TWO PACKS, ONE FOR BITS 0-15 AND THE OTHER FOR BITS 16-31. THE PLANE SELECT LEADS ARE GENERATED BY DECODING BITS 9-11 OF THE MAR WITHIN THE MICROCONTROL AND SENDING A 2-OUT-OF-8 PLANE SELECT SIGNAL TO THE MICROPROGRAM STORE PACKS.

NOTE THAT ALL OF THE GATES WITHIN THE MICROPROGRAM STORE PACKS ARE 5-VOLT T²L GATES WITH THE SAME BASIC CHARACTERISTICS AS THE NORMAL 3-VOLT 1A GATE. HOWEVER THEY HAVE HIGHER SIGNAL LEVEL THRSHOLDS AND THEREFORE AN

CIRCUIT OPERATION (CONT)

INTERFACE CIRCUIT IS REQUIRED WHEN GOING FROM THE 1A GATE TO THE T²L GATE. THE LOGIC LEVELS FOR THE 1A GATE VARY FROM ABOUT 100 TO 250 MILLIVOLTS FOR A ZERO LEVEL TO 1 TO 1.2 VOLTS FOR A ONE LEVEL. THIS COMPARES WITH 400 TO 800 MILLIVOLTS FOR A ZERO LEVEL AND 2.5 TO 5.0 VOLTS FOR A ONE LEVEL T²L GATE. THE ONLY TIMING REQUIREMENT ON THE MICROPROGRAM STORE IS THAT THE DATA BE STABLE AT ITS OUTPUT IN APPROXIMATELY 65ns AFTER THE ADDRESS LEADS HAVE BECOME STABLE AT ITS INPUT. ALSO, THE MICROPROGRAM STORE CANNOT CHANGE STATE WITHIN 25ns FOLLOWING THE CHANGE OF STATE OF THE ADDRESS LEADS AT ITS INPUT. FOR ADDITIONAL TIMING INFORMATION ON THE MICROPROGRAM STORE AND THE ASSOCIATED MICROCONTROL, SEE FS 1.



NOTE:

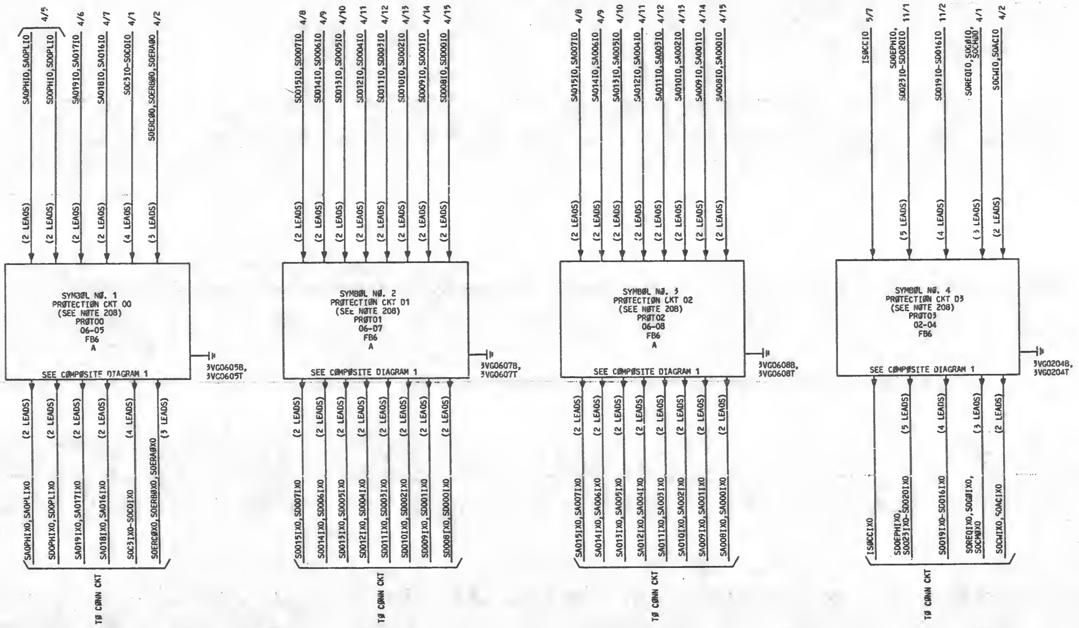
1. FOR A DETAILED DESCRIPTION OF A MICROPROGRAM STORE PLANE SEE SD-4C005-02.

PART OF FS 12
COMPOSITE DIAGRAM 4

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 6D
BELL LABORATORIES	SD-1C900-01	B12GD

PART OF FS 13

PRØTECTIØN CIRCUIT
INTERCØNNECTIØN AND FLØW DIAGRAM



PART ØF FS 13
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

B13AA

PART OF FS 13

PROTECTION CIRCUIT

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
ISOCCIXO	INTERRUPT SET FROM OTHER CENTRAL CONTROL (UNFUSED)
ISDCCIO	INTERRUPT SET FROM OTHER CENTRAL CONTROL (FUSED) (SETS BIT 7 OF THE IS)
SAOPHIXO	MY MAIN STORE ADDRESS BUS INPUT PARITY HIGH (UNFUSED)
SAOPHIO	MY MAIN STORE ADDRESS BUS INPUT PARITY HIGH (FUSED)
SAOPLIXO	MY MAIN STORE ADDRESS BUS INPUT PARITY LOW (UNFUSED)
SAOPLIO	MY MAIN STORE ADDRESS BUS INPUT PARITY LOW (FUSED)
SA000IXO-SA019IXO	MY MAIN STORE ADDRESS BUS INPUTS BITS 0-19 (UNFUSED)
SA000IO-SA019IO	MY MAIN STORE ADDRESS BUS INPUTS BITS 0-19 (FUSED)
SDOEPHIO	MY MAIN STORE DATA BUS, EXTENDED PARITY HIGH INPUT
SDOEPHXO	MY MAIN STORE DATA BUS EXTENDED PARITY HIGH (UNFUSED)
SDOPHIXO	MY MAIN STORE DATA BUS PARITY HIGH INPUT (UNFUSED)
SOOPHIO	MY MAIN STORE DATA BUS PARITY HIGH INPUT (FUSED)
SDOPLIXO	MY MAIN STORE DATA BUS PARITY LOW INPUT (UNFUSED)
SDOPLIO	MY MAIN STORE DATA BUS PARITY LOW INPUT (FUSED)
SD000IXO-SD015IXO	MY MAIN STORE DATA BUS INPUT LEADS 0-15 (UNFUSED)
SD000IO-SD015IO	MY MAIN STORE DATA BUS INPUT LEADS 0-15 (FUSED)
SD016IXO-SD023IXO	MY MAIN STORE DATA BUS INPUT LEADS 16-23 (UNFUSED)
SD016IO-SD023IO	MY MAIN STORE DATA BUS INPUT LEADS 16-23 (FUSED)
SOACIXO	MY MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL INPUT (UNFUSED)
SOACIO	MY MAIN STORE BUS AUTOMATIC ERROR CORRECTION SIGNAL INPUT (FUSED)
SOCMOXO	MY MAIN STORE BUS STORE COMPLETE SIGNAL OUTPUT (UNFUSED)
SOCMOO	MY MAIN STORE BUS STORE COMPLETE SIGNAL OUTPUT (FUSED)
SOCWIXO	MY MAIN STORE BUS COMPLEMENT WRITE SIGNAL INPUT (UNFUSED)
SOCWIO	MY MAIN STORE BUS COMPLEMENT WRITE SIGNAL INPUT (FUSED)
SOC0IXO-SOC3IXO	MY MAIN STORE BUS CONTROL LEAD INPUTS (UNFUSED)
SOC0IO-SOC3IO	MY MAIN STORE BUS CONTROL LEAD INPUTS (FUSED)
SOERAOXO	MY MAIN STORE BUS ERROR SIGNAL OUTPUT (UNFUSED)
SOERAOO	MY MAIN STORE ERROR SIGNAL A OUTPUT (FUSED)
SOERBOXO	MY MAIN STORE BUS ERROR SIGNAL B OUTPUT (UNFUSED)

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
SOERBDO	MY MAIN STORE BUS ERROR SIGNAL B OUTPUT (FUSED)
SOERCOXO	MY MAIN STORE BUS ERROR SIGNAL C OUTPUT (UNFUSED)
SOERCDO	MY MAIN STORE BUS ERROR SIGNAL C OUTPUT (FUSED)
SOGOIXO	MY MAIN STORE BUS STORE GO SIGNAL INPUT (UNFUSED)
SOGDIO	MY MAIN STORE BUS STORE GO SIGNAL INPUT (FUSED)
SOREOIXO	MY MAIN STORE BUS STORE REQUEST SIGNAL INPUT (UNFUSED)
SOREDIO	MY MAIN STORE BUS STORE REQUEST SIGNAL INPUT (FUSED)

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

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02/21/77

PART OF FS 13

PROTECTION CIRCUIT

SYMBOL NO. 1

PROTECTION CKT 00
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT00	06-05	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		015			PC120	
		215			CCI120	
SA0PHIX0	0	204	TO CONN CKT		CCI030	
SA0PHI0	I	004	4/5		PC030	
SA0PLIX0	0	203	TO CONN CKT		CCI020	
SA0PLI0	I	003	4/5		PC020	
SA016IX0	0	205	TO CONN CKT		CCI040	
SA016I0	I	005	4/7		PC040	
SA017IX0	0	207	TO CONN CKT		CCI060	
SA017I0	I	007	4/6		PC060	
SA018IX0	0	206	TO CONN CKT		CCI050	
SA018I0	I	006	4/7		PC050	
SA019IX0	0	208	TO CONN CKT		CCI070	
SA019I0	I	008	4/6		PC070	
SD0PHIX0	0	202	TO CONN CKT		CCI010	
SD0PHI0	I	002	4/5		PC010	
SD0PLIX0	0	201	TO CONN CKT		CCI000	
SD0PLI0	I	001	4/5		PC000	
SDC0IX0	0	211	TO CONN CKT		CCI080	
SDC0I0	I	011	4/1		PC080	
SDC1IX0	0	212	TO CONN CKT		CCI090	
SDC1I0	I	012	4/1		PC090	
SDC2IX0	0	213	TO CONN CKT		CCI100	
SDC2I0	I	013	4/1		PC100	
SDC3IX0	0	214	TO CONN CKT		CCI110	
SDC3I0	I	014	4/1		PC110	
SDERA0X0	0	216	TO CONN CKT		CCI130	
SDERA00	I	016	4/2		PC130	
SDERB0X0	0	218	TO CONN CKT		CCI150	
SDERB00	I	018	4/2		PC150	
SDERC0X0	0	217	TO CONN CKT		CCI140	
SDERC00	I	017	4/2		PC140	
3T0588	GRD	0GD		203	GRD	
	GRD	100		203		
	GRD	101		203		
	GRD	102		203		
	GRD	103		203		
	GRD	104		203		
	GRD	105		203		
	GRD	106		203		
	GRD	107		203		
	GRD	108		203		
	GRD	109		203		
	GRD	110		203		
	GRD	111		203		
	GRD	112		203		
	GRD	113		203		
	GRD	114		203		
	GRD	115		203		
	GRD	116		203		
	GRD	117		203		
	GRD	118		203		
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	301		203		
	GRD	302		203		
	GRD	303		203		
	GRD	304		203		
	GRD	305		203		
	GRD	306		203		

SYMBOL NO. 1 (CONT)

PROTECTION CKT 00
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT00	06-05	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T0588	GRD	307		203		
	GRD	308		203		
	GRD	309		203		
	GRD	310		203		
	GRD	311		203		
	GRD	312		203		
	GRD	313		203		
	GRD	314		203		
	GRD	315		203		
	GRD	316		203		
	GRD	317		203		
	GRD	318		203		
	GRD	319		203	GRD	
3VG0605B	GRD	009			GRD	
	GRD	200			GRD	
	GRD	209			GRD	
3VG0605T	GRD	010			GRD	
	GRD	210			GRD	
	GRD	219			GRD	
	GRD	319			GRD	
3V0588	PWR	000		203	+3	
	PWR	019		203	+3	

SYMBOL NO. 2

PROTECTION CKT 01
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT01	06-07	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SD000IX0	0	201	TO CONN CKT		CCI000	
SD000I0	I	001	4/15		PC000	
SD001IX0	0	203	TO CONN CKT		CCI020	
SD001I0	I	003	4/14		PC020	
SD002IX0	0	205	TO CONN CKT		CCI040	
SD002I0	I	005	4/13		PC040	
SD003IX0	0	207	TO CONN CKT		CCI060	
SD003I0	I	007	4/12		PC060	
SD004IX0	0	211	TO CONN CKT		CCI080	
SD004I0	I	011	4/11		PC080	
SD005IX0	0	213	TO CONN CKT		CCI100	
SD005I0	I	013	4/10		PC100	
SD006IX0	0	215	TO CONN CKT		CCI120	
SD006I0	I	015	4/9		PC120	
SD007IX0	0	217	TO CONN CKT		CCI140	
SD007I0	I	017	4/8		PC140	
SD008IX0	0	202	TO CONN CKT		CCI010	
SD008I0	I	002	4/15		PC010	
SD009IX0	0	204	TO CONN CKT		CCI030	
SD009I0	I	004	4/14		PC030	
SD010IX0	0	206	TO CONN CKT		CCI050	

SYMBOL NO. 2 (CONT)

PROTECTION CKT 01
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT01	06-07	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SD010I0	I	006	4/13		PC050	
SD011IX0	0	208	TO CONN CKT		CCI070	
SD011I0	I	008	4/12		PC070	
SD012IX0	0	212	TO CONN CKT		CCI090	
SD012I0	I	012	4/11		PC090	
SD013IX0	0	214	TO CONN CKT		CCI110	
SD013I0	I	014	4/10		PC110	
SD014IX0	0	216	TO CONN CKT		CCI130	
SD014I0	I	016	4/9		PC130	
SD015IX0	0	218	TO CONN CKT		CCI150	
SD015I0	I	018	4/8		PC150	
3T0588	GRD	0GD		203	GRD	
	GRD	100		203		
	GRD	101		203		
	GRD	102		203		
	GRD	103		203		
	GRD	104		203		
	GRD	105		203		
	GRD	106		203		
	GRD	107		203		
	GRD	108		203		
	GRD	109		203		
	GRD	110		203		
	GRD	111		203		
	GRD	112		203		
	GRD	113		203		
	GRD	114		203		
	GRD	115		203		
	GRD	116		203		
	GRD	117		203		
	GRD	118		203		
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	301		203		
	GRD	302		203		
	GRD	303		203		
	GRD	304		203		
	GRD	305		203		
	GRD	306		203		
	GRD	307		203		
	GRD	308		203		
	GRD	309		203		
	GRD	310		203		
	GRD	311		203		
	GRD	312		203		
	GRD	313		203		
	GRD	314		203		
	GRD	315		203		
	GRD	316		203		
	GRD	317		203		
	GRD	318		203		
	GRD	319		203	GRD	
3VG0607B	GRD	009			GRD	
	GRD	200			GRD	
	GRD	209			GRD	
3VG0607T	GRD	010			GRD	
	GRD	210			GRD	
	GRD	219			GRD	
	GRD	319			GRD	
3V0588	PWR	000		203	+3	

SYMBOL NO. 2 (CONT)

PROTECTION CKT 01
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT01	06-07	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V0588	PWR	019		203	+3	

PART OF FS 13
SYMBOL(S) 1 2

3A CENTRAL CONTROL
DWG SIZE C2
ISSUE 7D
BELL LABORATORIES
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PART OF FS 13

PROTECTION CIRCUIT

SYMBOL NO. 3

PROTECTION CKT 02
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT02	06-08	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SA000IX0	0	201	TO CONN CKT		CC1000	
SA000I0	I	001	4/15		PC000	
SA001IX0	0	203	TO CONN CKT		CC1020	
SA001I0	I	003	4/14		PC020	
SA002IX0	0	205	TO CONN CKT		CC1040	
SA002I0	I	005	4/13		PC040	
SA003IX0	0	207	TO CONN CKT		CC1060	
SA003I0	I	007	4/12		PC060	
SA004IX0	0	211	TO CONN CKT		CC1080	
SA004I0	I	011	4/11		PC080	
SA005IX0	0	213	TO CONN CKT		CC1100	
SA005I0	I	013	4/10		PC100	
SA006IX0	0	215	TO CONN CKT		CC1120	
SA006I0	I	015	4/9		PC120	
SA007IX0	0	217	TO CONN CKT		CC1140	
SA007I0	I	017	4/8		PC140	
SA008IX0	0	202	TO CONN CKT		CC1010	
SA008I0	I	002	4/15		PC010	
SA009IX0	0	204	TO CONN CKT		CC1030	
SA009I0	I	004	4/14		PC030	
SA010IX0	0	206	TO CONN CKT		CC1050	
SA010I0	I	006	4/13		PC050	
SA011IX0	0	208	TO CONN CKT		CC1070	
SA011I0	I	008	4/12		PC070	
SA012IX0	0	212	TO CONN CKT		CC1090	
SA012I0	I	012	4/11		PC090	
SA013IX0	0	214	TO CONN CKT		CC1110	
SA013I0	I	014	4/10		PC110	
SA014IX0	0	216	TO CONN CKT		CC1130	
SA014I0	I	016	4/9		PC130	
SA015IX0	0	218	TO CONN CKT		CC1150	
SA015I0	I	018	4/8		PC150	
3T058B	GRD	0GD		203	GRD	
	GRD	100		203		
	GRD	101		203		
	GRD	102		203		
	GRD	103		203		
	GRD	104		203		
	GRD	105		203		
	GRD	106		203		
	GRD	107		203		
	GRD	108		203		
	GRD	109		203		
	GRD	110		203		
	GRD	111		203		
	GRD	112		203		
	GRD	113		203		
	GRD	114		203		
	GRD	115		203		
	GRD	116		203		
	GRD	117		203		
	GRD	118		203		
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	301		203		
	GRD	302		203		
	GRD	303		203		
	GRD	304		203		
	GRD	305		203		
	GRD	306		203		

SYMBOL NO. 3 (CONT)

PROTECTION CKT 02
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT02	06-08	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058B	GRD	307		203		
	GRD	308		203		
	GRD	309		203		
	GRD	310		203		
	GRD	311		203		
	GRD	312		203		
	GRD	313		203		
	GRD	314		203		
	GRD	315		203		
	GRD	316		203		
	GRD	317		203		
	GRD	318		203		
	GRD	319		203	GRD	
3VG0608B	GRD	009			GRD	
	GRD	200			GRD	
	GRD	209			GRD	
3VG0608T	GRD	010			GRD	
	GRD	210			GRD	
	GRD	219			GRD	
	GRD	319			GRD	
3V058B	PWR	000		203	+3	
	PWR	019		203	+3	

SYMBOL NO. 4

PROTECTION CKT 03
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT03	02-04	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		005			PC040	
		205			CC1040	
ISOCCIX0	0	202	TO CONN CKT		CC1010	
ISOCCI0	I	002	5/7		PC010	
SD0EPHI0	I	008	11/1		PC070	
SD0EPHX0	0	208	TO CONN CKT		CC1070	
SD016IX0	0	211	TO CONN CKT		CC1080	
SD016I0	I	011	11/2		PC080	
SD017IX0	0	212	TO CONN CKT		CC1090	
SD017I0	I	012	11/2		PC090	
SD018IX0	0	213	TO CONN CKT		CC1100	
SD018I0	I	013	11/2		PC100	
SD019IX0	0	214	TO CONN CKT		CC1110	
SD019I0	I	014	11/2		PC110	
SD020IX0	0	215	TO CONN CKT		CC1120	
SD020I0	I	015	11/1		PC120	
SD021IX0	0	216	TO CONN CKT		CC1130	
SD021I0	I	016	11/1		PC130	
SD022IX0	0	217	TO CONN CKT		CC1140	
SD022I0	I	017	11/1		PC140	
SD023IX0	0	218	TO CONN CKT		CC1150	

SYMBOL NO. 4 (CONT)

PROTECTION CKT 03
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT03	02-04	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SD023I0	I	018	11/1		PC150	
SOACIX0	0	206	TO CONN CKT		CC1050	
SOACI0	I	006	4/2		PC050	
SOCMOX0	0	203	TO CONN CKT		CC1020	
SOCMO0	I	003	4/1		PC020	
SOCHIX0	0	204	TO CONN CKT		CC1030	
SOCHI0	I	004	4/2		PC030	
SOGDIX0	0	201	TO CONN CKT		CC1000	
SOGOI0	I	001	4/1		PC000	
SOREOIX0	0	207	TO CONN CKT		CC1060	
SOREDI0	I	007	4/1		PC060	
3T054A	GRD	0GD		203	GRD	
	GRD	100		203		
	GRD	101		203		
	GRD	102		203		
	GRD	103		203		
	GRD	104		203		
	GRD	105		203		
	GRD	106		203		
	GRD	107		203		
	GRD	108		203		
	GRD	109		203		
	GRD	110		203		
	GRD	111		203		
	GRD	112		203		
	GRD	113		203		
	GRD	114		203		
	GRD	115		203		
	GRD	116		203		
	GRD	117		203		
	GRD	118		203		
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	301		203		
	GRD	302		203		
	GRD	303		203		
	GRD	304		203		
	GRD	305		203		
	GRD	306		203		
	GRD	307		203		
	GRD	308		203		
	GRD	309		203		
	GRD	310		203		
	GRD	311		203		
	GRD	312		203		
	GRD	313		203		
	GRD	314		203		
	GRD	315		203		
	GRD	316		203		
	GRD	317		203		
	GRD	318		203		
	GRD	319		203	GRD	
3VG0204B	GRD	009			GRD	
	GRD	200			GRD	
	GRD	209			GRD	
3VG0204T	GRD	010			GRD	
	GRD	210			GRD	
	GRD	219			GRD	
	GRD	319			GRD	
3V054A	PWR	000	(X)14/1	203	+3	

SYMBOL NO. 4 (CONT)

PROTECTION CKT 03
(SEE NOTE 208)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PROT03	02-04	FB6	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V054A	PWR	019	(X)14/1	203	+3	
3V054B	PWR	000	14/1		+3	
	PWR	019	14/1		+3	

PART OF FS 13
SYMBOL(S) 3 4

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B13CB

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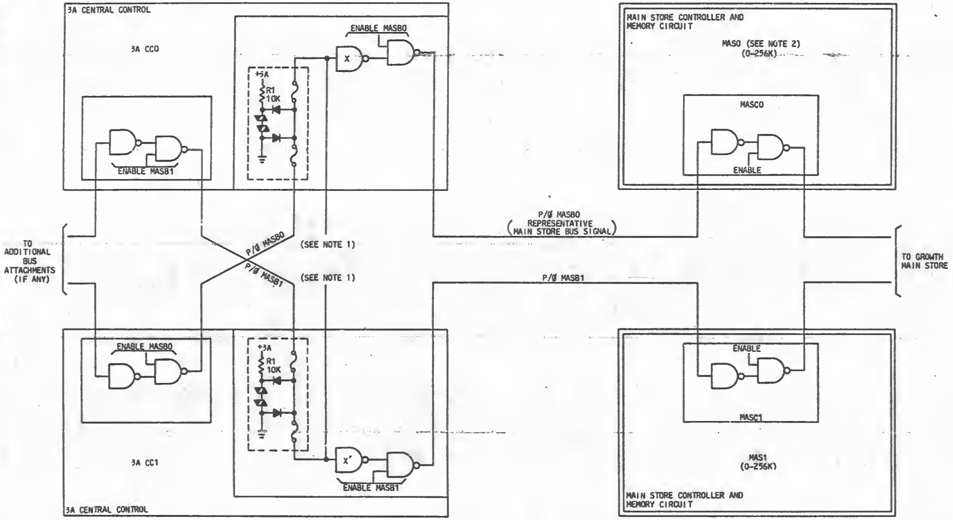
12/01/77

PART OF FS 13

PROTECTION CIRCUIT

COMPOSITE DIAGRAM 1

MAIN STORE BUS - INTERPROCESSOR CONNECTION SHOWING PLACEMENT OF PROTECTION CIRCUIT



NOTES:

1. IF ADDITIONAL BUS ATTACHMENTS ARE USED THE PROTECTION CIRCUIT CAN BE BY-PASSED VIA THIS INPUT (SEE CAD 1, ELEMENT C). IT IS ASSUMED THAT THE ADDED BUS ATTACHMENT WILL PROVIDE THE PROTECTION CIRCUIT.
2. K=1024

CIRCUIT OPERATION

A FUSE PROTECTION CIRCUIT IS USED FOR ALL LEADS CONNECTING BETWEEN A DUPLEX PAIR OF 3A CC'S. THIS PROTECTION CIRCUIT PROVIDES FAULT ISOLATION FOR CATASTROPHIC TYPE FAULTS, i.e., A FOREIGN POTENTIAL THAT MIGHT OTHERWISE BRING DOWN A DUPLEX SYSTEM. SINCE, WITH ONLY ONE EXCEPTION, ALL OF THE LEADS THAT INTERCONNECT THE TWO 3A CC'S (THE DUPLEX SYSTEM) ARE MAIN STORE BUS (MASB) SIGNALS, THE FUSE PROTECTION CIRCUIT IS SHOWN IN ITS RELATIONSHIP TO THE MASB IN COMPOSITE DIAGRAM 1. NOTE THAT THERE ARE SOME OTHER LEADS INTERCONNECTING THE TWO 3A CC'S, FOR EXAMPLE I/O SUBCHANNELS, BUT THESE SIGNALS USE TRANSFORMERS AND THEREFORE HAVE THE FAULT PROTECTION BUILT INTO THE TRANSFORMER ISOLATION. THE ONE OTHER LEAD THAT CONNECTS THE TWO 3A CC'S IS AN INTERRUPT LEAD THAT GOES FROM ONE 3A CC TO ANOTHER. BECAUSE THIS LEAD IS TRANSMITTED BY THE SAME RIBBON CABLES AS THE STORE BUS LEADS, IT CAN BE ASSUMED TO OPERATE THE SAME, RELATIVE TO THE FUSE PROTECTION CIRCUIT, AS DO THE MASB SIGNALS. AS SHOWN IN COMPOSITE DIAGRAM 1, THE MASB SIGNALS ARE FUSED AT THEIR INPUT TO THE 3A CC WHICH THEY ENTER. THIS REQUIREMENT IS NECESSARY BECAUSE IF A FOREIGN POTENTIAL WAS ACCIDENTLY APPLIED TO CC1, FOR EXAMPLE, AND THE FUSE PROTECTION WAS CONTAINED IN THE OUTPUT OF THE MASB SIGNALS IN CC1, IT MIGHT BE POSSIBLE FOR THE POTENTIAL TO BE PLACED ON THE SIDE OF THE FUSE CLOSEST TO THE CCO AND HENCE DEFEAT ITS PURPOSE. THUS, WITH THE PROTECTION CIRCUIT PLACED IN THE POSITION SHOWN IN COMPOSITE DIAGRAM 1, IT IS NOT POSSIBLE FOR A FOREIGN POTENTIAL TO BE PLACED ANYWHERE ON CC1 WITHOUT IT GOING THROUGH THE INPUT FUSE ON CCO. THE FUSE PROTECTION CIRCUIT IS CONTAINED ON A CIRCUIT PACK FB6 AND FOR THE DETAILS OF ITS OPERATION, SEE CPS DESCRIPTION. THE BASIC OPERATION OF THE PROTECTION CIRCUIT PROVIDES BOTH OVERVOLTAGE AND OVER-CURRENT PROTECTION. IF THE FUSE IS BLOWN, THE FB6 PACK ON WHICH IT IS LOCATED MUST BE REPLACED. NOTE ALSO THAT IN SOME APPLICATIONS, ADDITIONAL BUS ATTACHMENTS MAY BE ADDED TO THE MAIN STORE BUS. IN THOSE CASES, IT MAY BE DESIRABLE TO HAVE THE FUSE PROTECTION IN THE NEW BUS ATTACHMENT UNIT INSTEAD OF IN THE 3A CC'S. FOR THAT PURPOSE THE FB6 PACKS ARE PROVIDED ON AN OPTIONAL BASIS, AND IF THEY ARE NOT USED, THE CONNECTORS INPUTTING ON THE MASB SIGNALS INPUTS TO A 3A CC MUST BE MOVED SO AS TO DIRECTLY CONNECT INTO THE INPUT OF GATE X AS SHOWN IN COMPOSITE DIAGRAM 1. (SEE CAD 1, ELEMENT C FOR EXACT INFORMATION.)

PART OF FS 13
COMPOSITE DIAGRAM 1

ISSUE 5A

3A CENTRAL CONTROL

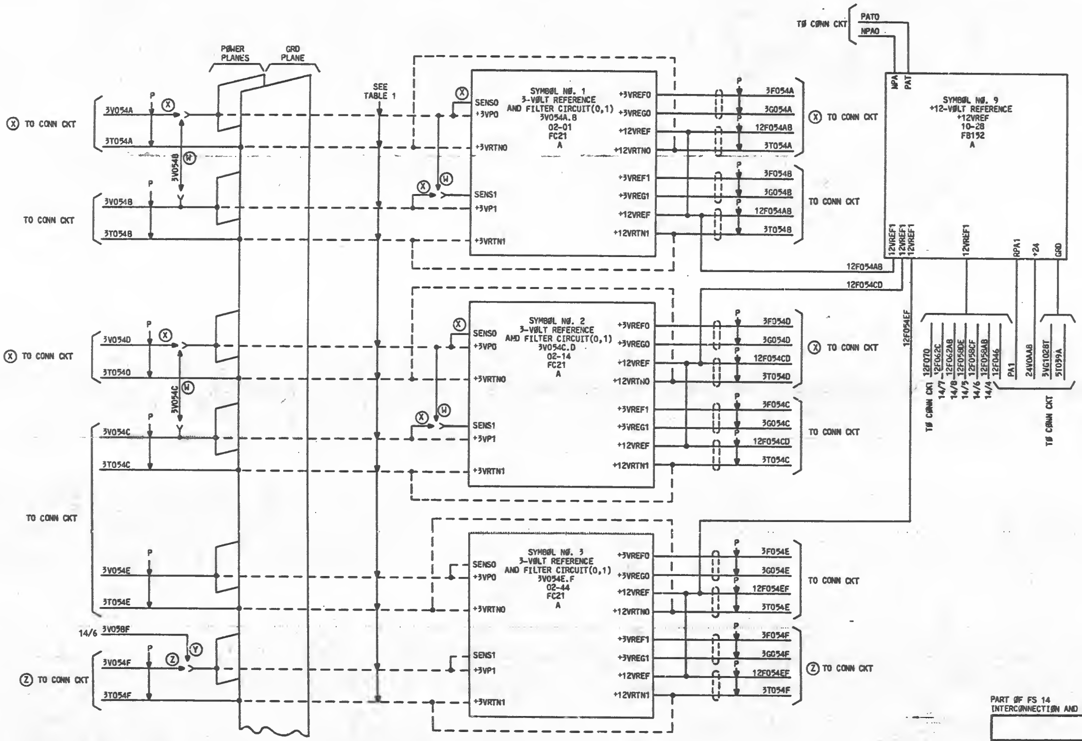
SD-1C900-01-B13GA

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF FS 14

POWER
INTERCONNECTION AND FLOW DIAGRAM

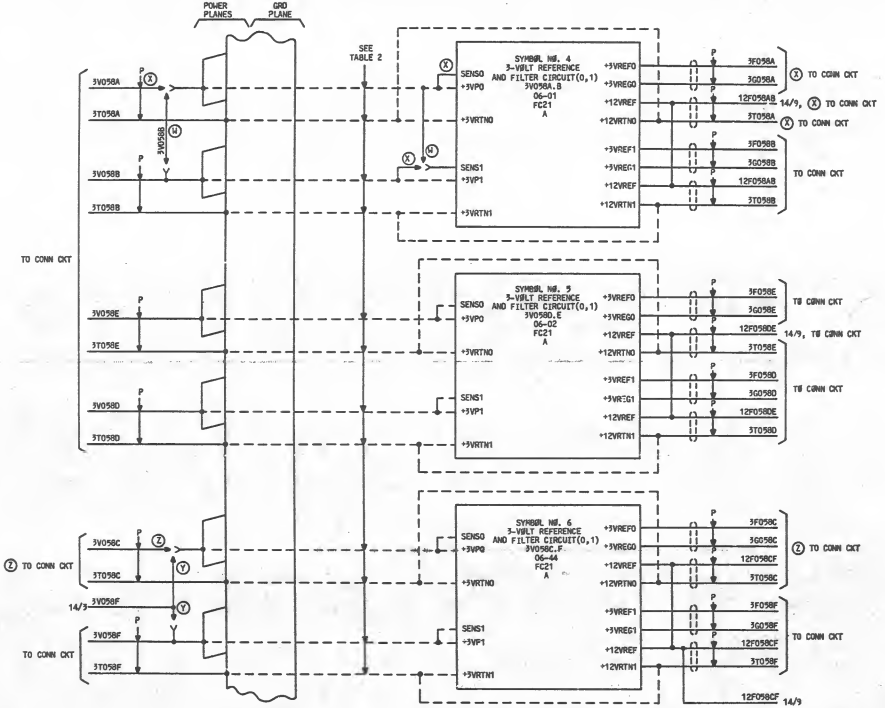


PART OF FS 14
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	814AA

PART OF FS 14

PØWER
INTERCØNNECTIØN AND FLØW DIAGRAM



PART ØF FS 14
INTERCØNNECTIØN AND FLØW DIAGRAM

3A CENTRAL CØNTRØL ②

DWG SIZE	ISSUE
6S	7D

BELL LABORATORIES

SD-1C900-01

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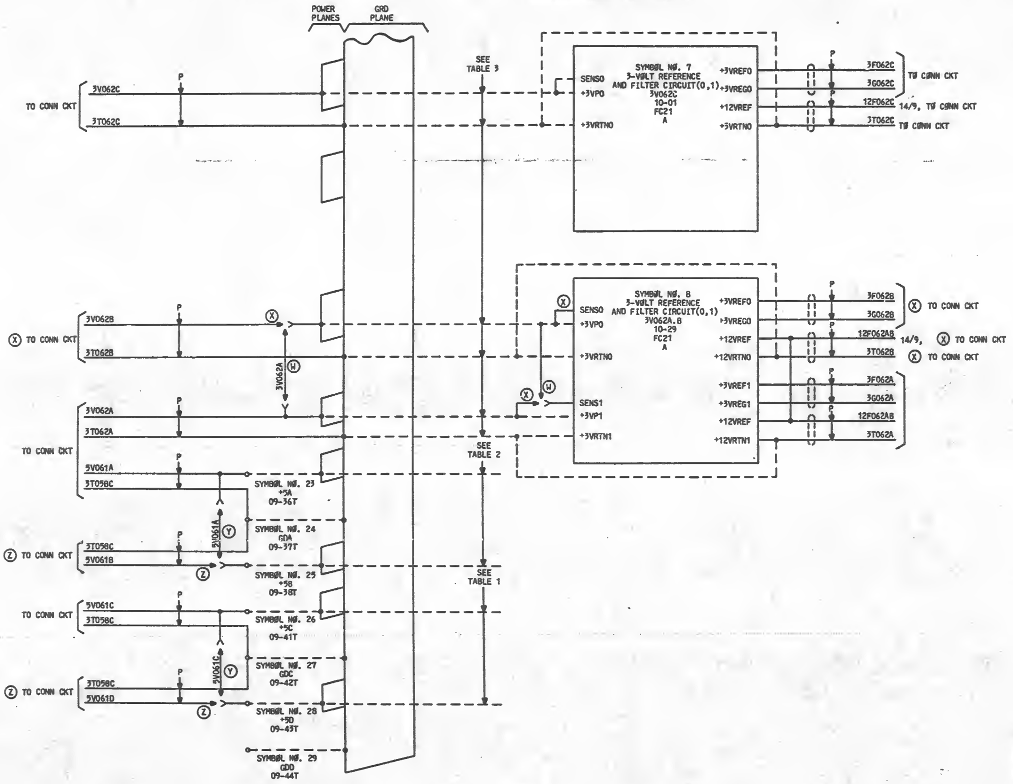
PART OF FS 14

POWER
INTERCONNECTION AND FLOW DIAGRAM



SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
NPAO	THE COMPLEMENT OF THE POWER ALARM SIGNAL OF THE 3 VOLT POWER SYSTEM
PATO	POWER ALARM TEST LEAD FOR 3 VOLT CONVERTERS
PA1	POWER ALARM INDICATOR ON 3 VOLT POWER SUPPLY

PART OF FS 14
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CONTROL ②		DWG SIZE 6S	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B14AC

E-7431 (12-73)

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PART OF FS 14

POWER
INTERCONNECTION AND FLOW DIAGRAM

POWER DISTRIBUTION TABLE 1

CIRCUIT PACK	EQPT LOC	GRD PLANE	Ⓦ 3V054B Ⓧ 3V054A	3V054B	3V054C	Ⓦ 3V054C Ⓧ 3V054D	3V054E	Ⓨ 3V058F Ⓩ 3V054F	5V061C	Ⓨ 5V061C Ⓩ 5V061D
		TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM
FC21	02-01	100-108, 300-307, 200,211, 112-118, 312-319, 0G0,2G0	000-007, 201-207	012-019, 212-219, 119						
FA1031	02-02	200,319, 0G0,2G0		000,119						
SPARE (NOTE 210)	02-03	200,319, 0G0,2G0	000,019							
F86	02-04	100-118, 301-319, 200, 0G0,2G0	000,019							
FA1024	02-08	200,319, 0G0,2G0		000,119						
↓	02-09	↓		↓						
↓	02-10	↓		↓						
↓	02-11	↓		000,119						
↓	02-12	↓	000,119							
FA1024	02-13	200,319, 0G0,2G0	000,119							
FC21	02-14	100-108, 300-307, 200,211, 112-118, 312-319, 0G0,2G0			012-019, 212-219, 119	000-007, 201-207				
FA1024	02-16	200,319, 0G0,2G0	000,119							
FA1024	02-17	↓	000,119							
FA1024	02-18	↓	000,119							
FA1030	02-19	↓				000,119				
FA1030	02-20	↓				↓				
FA1029	02-21	↓				↓				
FA1029	02-22	↓				↓				
FA1046	02-23	↓				000,119				
FA1033	02-24	↓			000,119					
FA1032	02-25	↓			↓					
FC202	02-26	↓			↓					
FA1037	02-27	↓			↓					
FA1036	02-28	↓			000,119					
FA1035	02-29	↓					000,119			
FA1023	02-31	↓					↓			
FA1022	02-32	↓					↓			
FA1018	02-33	↓					↓			
FA1017	02-34	↓					↓			
FA1016	02-35	↓					000,119			
(NOTE 216)	02-40	↓						000,119	001,100, 101,201, 300,301	
(NOTE 216)	02-41	↓						↓	001,100, 101,201, 300,301	
(NOTE 216)	02-42	↓						↓		001,100, 101,201, 300,301
(NOTE 216)	02-43	200,319, 0G0,2G0						000,119		001,100, 101,201, 300,301
FC21	02-44	100-108, 300-307, 200,211, 112-118, 312-319, 0G0,2G0					000-007, 201-207	012-019, 212-219, 119		

(CONT)

POWER DISTRIBUTION TABLE 1

CIRCUIT PACK	EQPT LOC	GRD PLANE	Ⓦ 3V054B Ⓧ 3V054A	3V054B	3V054C	Ⓦ 3V054C Ⓧ 3V054D	3V054E	Ⓨ 3V058F Ⓩ 3V054F	5V061C	Ⓨ 5V061C Ⓩ 5V061D
		TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM
(NOTE 216)	06-40	200,319, 0GD,2G0						000,119	001,100, 101,201, 300,301	
(NOTE 216)	06-41	↓						↓	001,100, 101,201, 300,301	
(NOTE 216)	06-42	↓						↓		001,100, 101,201, 300,301
(NOTE 216)	06-43	200,319, 0GD,2G0						000,119		001,100, 101,201, 300,301

PART OF FS 14
INTERCONNECTION AND FLOW DIAGRAM

ISSUE 7D

3A CENTRAL CONTROL ②

SD-1C900-01-B14AD

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF FS 14

PØWER
INTERCONNECTION AND FLOW DIAGRAM

POWER DISTRIBUTION TABLE 2

CIRCUIT PACK	EQPT LOC	GRD PLANE	Ⓦ3V058B Ⓧ3V058A	3V058B	Ⓨ3V058F Ⓩ3V058C	3V058D	3V058E	3V058F	5V061A	Ⓨ5V061C Ⓩ5V061D
		TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM
FA1040	02-05	200,319, 0GD,2GD					000,119			
FA1040	02-06	↓					000,119			
FA1040	02-07	↓					000,119			
(NOTE 216)	02-36	↓			000,119				001,100, 101,201, 300,301	
(NOTE 216)	02-37	↓			↓				001,100, 101,201, 300,301	
(NOTE 216)	02-38	↓			↓					001,100, 101,201, 300,301
(NOTE 216)	02-39	200,319, 0GD,2GD			000,119					001,100, 101,201, 300,301
FC21	06-01	100-108, 300-307, 200,211, 112-118, 312-319, 0GD,2GD	000-007, 201-207	012-019, 212-219, 119						
FC21	06-02	100-108, 300-307, 200,211, 112-118, 312-319, 0GD,2GD				012-019, 200-219, 119	000-007, 201-207			
SPARE (NOTE209)	06-03	200,319, 0GD,2GD								
FA1031	06-04	200,319, 0GD,2GD		000,119						
FB6	06-05	100-118, 301-319, 200, 0GD,2GD		000,019						
FA1034	06-06	200,319, 0GD,2GD		000,119						
FB6	06-07	100-118, 301-319, 200, 0GD,2GD		000,019						
FB6	06-08	100-118, 301-319, 200, 0GD,2GD		000,019						
FA1010	06-09	200,319, 0GD,2GD		000,119						
↓	06-10	↓		000,119						
↓	06-11	↓		000,119						
↓	06-12	↓	000,119							
↓	06-13	↓	↓							
↓	06-14	↓	↓							
↓	06-16	↓	↓							
FA1010	06-17	↓	000,119							
FA1014	06-28	↓						000,119		
FB486	06-29	↓						000,019	010,210	
FA1025	06-31	↓						000,119		
FA1019	06-32	↓						↓		
FA1011	06-33	↓						↓		
FA1045	06-34	↓						↓		
FA1021	06-35	200,319, 0GD,2GD						000,119		

(CONT)

POWER DISTRIBUTION TABLE 2

CIRCUIT PACK	EQPT LOC	GRD PLANE	Ⓗ3V058B Ⓧ3V058A	3V058B	Ⓨ3V058F Ⓩ3V058C	3V058D	3V058E	3V058F	5V061A	Ⓨ5V061C Ⓩ5V061D
		TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM
(NOTE 216)	06-36	200,319, 0GD,2GD			000,119				001,100, 101,201, 300,301	
(NOTE 216)	06-37	↓			↓				001,100, 101,201, 300,301	
(NOTE 216)	06-38	↓			↓					001,100, 101,201, 300,301
(NOTE 216)	~~06-39~~	200,319, 0GD,2GD			000,119					001,100, 101,201, 300,301
FC21	06-44	100-108, 300-307, 200,211, 112-118, 312-319, 0GD,2GD			000-007, 201-207			012-019, 212-219, 119		
FA1038	10-07	200 319, 0GD,2GD				~~000,119~~				
FA1039	10-08	↓				↓				
FC201	10-09	↓				↓				
FC201	10-10	↓				↓				
FA1038	10-11	↓				000,119				
FA1039	10-12	↓					000,119			
FC201	10-13	↓					000,119			
FC201	10-14	200,319, 0GD,2GD					000,119			

PART OF FS 14
INTERCONNECTION AND FLOW DIAGRAM

ISSUE
7D

3A CENTRAL CØNTRØL ②

SD-1C900-01-B14AE

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF FS 14

PØWER
INTERCONNECTION AND FLOW DIAGRAM

PØWER DISTRIBUTIØN TABLE 3

CIRCUIT PACK	EQPT LØC	GRD PLANE	3V062A	Ⓦ3V062A Ⓧ3V062B	3V062C
		TERM	TERM	TERM	TERM
FA1010	06-18	200,319, 0G0,2G0		000,119	
FA1020	06-19	↓		↓	
FA1026	06-20	↓		↓	
FA1013	06-21	↓		↓	
FA1012	06-22	↓		000,119	
FA1015	06-23	↓	000,119		
FA1012	06-24	↓	↓		
FA1012	06-25	↓	↓		
FA1015	06-26	↓	↓		
FA1012	06-27	200,319, 0G0,2G0	000,119		
FC21	10-01	100-108, 300-307, 200,211, 112-118, 312-319, 0G0,2G0			000-007, 201-207
TS1 (NØTE 213)	10-02	000-019, 200-219, 0G0,2G0			
FA1038	10-03	200,319, 0G0,2G0			000,119
FA1039	10-04	↓			↓
FC201	10-05	↓			↓
FC201	10-06	200.319, 0G0,2G0			000,119
TS2 (NØTE 213)	10-16	000-019, 200-219, 0G0,2G0			
TS3 (NØTE 214)	10-17	000-010, 012-019, 200-219, 0G0,2G0			
TS4 (NØTE 215)	10-18	200,319, 0G0,2G0			
TS5 (NØTE 215)	10-19	↓			
TS6 (NØTE 211)	10-20	↓			
TS7 (NØTE 211)	10-21	↓			
FA1028	10-22	↓			000,119
FA1027	10-23	↓			000,119
SPARE (NØTE 209)	10-24	↓	000,119		
SPARE (NØTE 209)	10-25	↓	↓		
TS8 (NØTE 212)	10-26	↓	↓		
TS9 (NØTE 212)	10-27	200,319, 0G0,2G0	000,119		
F8152	10-28	200,319, 219, 0G0,2G0			
FC21	10-29	100-108, 300-307, 200,211, 112-118, 312-319, 0G0,2G0	012-019, 212-219, 119	000-007, 201-207	

PART OF FS 14
INTERCONNECTION AND FLOW DIAGRAM

3A CENTRAL CØNTRØL

②

ISSUE
7D

SD-1C900-01-B14AF

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF FS 14

POWER

SYMBOL NO. 1

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V054A.B	02-01	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F054AB	OI	109	14/9 (X)TO CONN CKT	202	+12VREF	
	OI	210	14/1 TO CONN CKT	202	+12VREF	
3F054A	O	009	(X)TO CONN CKT		+3VREF0	
3F054B	O	310	TO CONN CKT		+3VREF1	
3G054A	O	008	(X)TO CONN CKT		+3VREG0	
3G054B	O	311	TO CONN CKT		+3VREG1	
3T054A	O	108		203	+12VRTN0	
	GRD	100		203	+3VRTN0	
	GRD	101		203	+3VRTN0	
	GRD	102		203	+3VRTN0	
	GRD	103		203	+3VRTN0	
	GRD	104		203	+3VRTN0	
	GRD	105		203	+3VRTN0	
	GRD	106		203	+3VRTN0	
	GRD	107		203	+3VRTN0	
	GRD	200	(X)TO CONN CKT	203	+3VRTN0	
	GRD	300		203	+3VRTN0	
	GRD	301		203	+3VRTN0	
	GRD	302		203	+3VRTN0	
	GRD	303		203	+3VRTN0	
	GRD	304		203	+3VRTN0	
	GRD	305		203	+3VRTN0	
	GRD	306		203	+3VRTN0	
	GRD	307		203	+3VRTN0	
3T054B	O	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	TO CONN CKT	203	+3VRTN1	
3V054A	PWR	000	(X)4/5,(X)4/8 (X)4/9,(X)4/10 (X)4/11,(X)13/4 (X)14/10 (X)TO CONN CKT	203	+3VP0	
	PWR	001	(X)14/1	203	+3VP0	
	PWR	002	(X)14/1	203	+3VP0	
	PWR	003	(X)14/1	203	+3VP0	
	PWR	004	(X)14/1	203	+3VP0	
	PWR	005	(X)14/1	203	+3VP0	
	PWR	006	(X)14/1	203	+3VP0	
	PWR	007	(X)14/1	203	+3VP0	
	PWR	201	(X)14/1	203	+3VP0	
	PWR	202	(X)14/1	203	+3VP0	
	PWR	203	(X)14/1	203	+3VP0	
	PWR	204	(X)14/1	203	+3VP0	

SYMBOL NO. 1 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V054A.B	02-01	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V054A	PWR	205	(X)14/1	203	+3VP0	
	PWR	206	(X)14/1	203	+3VP0	
	PWR	207	(X)14/1	203	+3VP0	
	I	309	(X)14/1	203	SENS0	
3V054B	PWR	119	(W)4/5,(W)4/8 (W)4/9,(W)4/10 (W)4/11,(W)13/4 (W)14/1,(W)14/10 TO CONN CKT	203	+3VP1	
	PWR	000	14/1	203	+3VP0	
	PWR	001	14/1	203	+3VP0	
	PWR	002	14/1	203	+3VF0	
	PWR	003	14/1	203	+3VP0	
	PWR	004	14/1	203	+3VP0	
	PWR	005	14/1	203	+3VP0	
	PWR	006	14/1	203	+3VP0	
	PWR	007	14/1	203	+3VP0	
	PWR	012	14/1	203	+3VP1	
	PWR	013	14/1	203	+3VP1	
	PWR	014	14/1	203	+3VP1	
	PWR	0'5	14/1	203	+3VP1	
	PWR	016	14/1	203	+3VP1	
	PWR	017	14/1	203	+3VP1	
	PWR	018	14/1	203	+3VP1	
	PWR	019	14/1	203	+3VP1	
	PWR	201	14/1	203	+3VP0	
	PWR	202	14/1	203	+3VP0	
	PWR	203	14/1	203	+3VP0	
	PWR	204	14/1	203	+3VP0	
	PWR	205	14/1	203	+3VP0	
	PWR	206	14/1	203	+3VP0	
	PWR	207	14/1	203	+3VP0	
	PWR	212	14/1	203	+3VP1	
	PWR	213	14/1	203	+3VP1	
	PWR	214	14/1	203	+3VP1	
	PWR	215	14/1	203	+3VP1	
	PWR	216	14/1	203	+3VP1	
	PWR	217	14/1	203	+3VP1	
	PWR	218	14/1	203	+3VP1	
	PWR	219	14/1	203	+3VP1	
	I	010	14/1	203	SENS1	

SYMBOL NO. 2

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V054C.D	02-14	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F054CD	OI	109	14/9 (X)TO CONN CKT	202	+12VREF	
	OI	210	14/2 TO CONN CKT	202	+12VREF	
3FC54C	O	310	TO CONN CKT		+3VREF1	
3F054D	O	009	(X)TO CONN CKT		+3VREF0	
3G054C	O	311	TO CONN CKT		+3VREG1	
3G054D	O	008	(X)TO CONN CKT		+3VREG0	
3T054C	O	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	TO CONN CKT	203	+3VRTN1	
3T054D	O	108		203	+12VRTN0	
	GRD	100		203	+3VRTN0	
	GRD	101		203	+3VRTN0	
	GRD	102		203	+3VRTN0	
	GRD	103		203	+3VRTN0	
	GRD	104		203	+3VRTN0	
	GRD	105		203	+3VRTN0	
	GRD	106		203	+3VRTN0	
	GRD	107		203	+3VRTN0	
	GRD	200	(X)TO CONN CKT	203	+3VRTN0	
	GRD	300		203	+3VRTN0	
	GRD	301		203	+3VRTN0	
	GRD	302		203	+3VRTN0	
	GRD	303		203	+3VRTN0	
	GRD	304		203	+3VRTN0	
	GRD	305		203	+3VRTN0	
	GRD	306		203	+3VRTN0	
	GRD	307		203	+3VRTN0	
3V054C	PWR	119	(W)4/1,(W)4/2 (W)4/3,(W)4/6 (W)4/7,(W)14/2 TO CONN CKT	203	+3VP1	
	PWR	000	14/2	203	+3VP0	
	PWR	001	14/2	203	+3VP0	
	PWR	002	14/2	203	+3VP0	
	PWR	003	14/2	203	+3VP0	
	PWR	004	14/2	203	+3VP0	
	PWR	005	14/2	203	+3VP0	
	PWR	006	14/2	203	+3VP0	
	PWR	007	14/2	203	+3VP0	
	PWR	012	14/2	203	+3VP1	
	PWR	013	14/2	203	+3VP1	
	PWR	014	14/2	203	+3VP1	

SYMBOL NO. 2 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V054C.D	02-14	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V054C	PWR	015	14/2	203	+3VP1	
	PWR	016	14/2	203	+3VP1	
	PWR	017	14/2	203	+3VP1	
	PWR	018	14/2	203	+3VP1	
	PWR	019	14/2	203	+3VP1	
	PWR	201	14/2	203	+3VP0	
	PWR	202	14/2	203	+3VP0	
	PWR	203	14/2	203	+3VP0	
	PWR	204	14/2	203	+3VP0	
	PWR	205	14/2	203	+3VP0	
	PWR	206	14/2	203	+3VP0	
	PWR	207	14/2	203	+3VP0	
	PWR	212	14/2	203	+3VP1	
	PWR	213	14/2	203	+3VP1	
	PWR	214	14/2	203	+3VP1	
	PWR	215	14/2	203	+3VP1	
	PWR	216	14/2	203	+3VP1	
	PWR	217	14/2	203	+3VP1	
	PWR	218	14/2	203	+3VP1	
	PWR	219	14/2	203	+3VP1	
	I	010	14/2	203	SENS1	
3V054D	PWR	000	(X)4/1,(X)4/2 (X)4/3,(X)4/6 (X)4/7 (X)TO CONN CKT	203	+3VP0	
	PWR	001	(X)14/2	203	+3VP0	
	PWR	002	(X)14/2	203	+3VP0	
	PWR	003	(X)14/2	203	+3VP0	
	PWR	004	(X)14/2	203	+3VP0	
	PWR	005	(X)14/2	203	+3VP0	
	PWR	006	(X)14/2	203	+3VP0	
	PWR	007	(X)14/2	203	+3VP0	
	PWR	201	(X)14/2	203	+3VP0	
	PWR	202	(X)14/2	203	+3VP0	
	PWR	203	(X)14/2	203	+3VP0	
	PWR	204	(X)14/2	203	+3VP0	
	PWR	205	(X)14/2	203	+3VP0	
	PWR	206	(X)14/2	203	+3VP0	
	PWR	207	(X)14/2	203	+3VP0	
	I	309	(X)14/2	203	SENS0	

PART OF FS 14
SYMBOL(S) 1 2

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B14CA

PRINTED IN U. S. A.

12/01/77

PART OF FS 14

POWER

SYMBOL NO. 3

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V054E.F	02-44	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F054EF	OI	109	14/9 TO CONN CKT	202	+12VREF	
	OI	210	14/3 (2)TO CONN CKT	202	+12VREF	
3F054E	O	009	TO CONN CKT		+3VREFO	
3F054F	O	310	(2)TO CONN CKT		+3VREF1	
3G054E	O	008	TO CONN CKT		+3VREGO	
3G054F	O	311	(2)TO CONN CKT		+3VREG1	
3T054E	O	108		203	+12VRTNO	
	GRD	100		203	+3VRTNO	
	GRD	101		203	+3VRTNO	
	GRD	102		203	+3VRTNO	
	GRD	103		203	+3VRTNO	
	GRD	104		203	+3VRTNO	
	GRD	105		203	+3VRTNO	
	GRD	106		203	+3VRTNO	
	GRD	107		203	+3VRTNO	
	GRD	200	TO CONN CKT	203	+3VRTNO	
	GRD	300		203	+3VRTNO	
	GRD	301		203	+3VRTNO	
	GRD	302		203	+3VRTNO	
	GRD	303		203	+3VRTNO	
	GRD	304		203	+3VRTNO	
	GRD	305		203	+3VRTNO	
	GRD	306		203	+3VRTNO	
	GRD	307		203	+3VRTNO	
3T054F	O	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	(2)TO CONN CKT	203	+3VRTN1	
3V054E	PWR	000	TO CONN CKT	203	+3VPO	
	PWR	001		203	+3VPO	
	PWR	002		203	+3VPO	
	PWR	003		203	+3VPO	
	PWR	004		203	+3VPO	
	PWR	005		203	+3VPO	
	PWR	006		203	+3VPO	
	PWR	007		203	+3VPO	
	PWR	201		203	+3VPO	
	PWR	202		203	+3VPO	
	PWR	203		203	+3VPO	
	PWR	204		203	+3VPO	
	PWR	205		203	+3VPO	
	PWR	206		203	+3VPO	
	PWR	207		203	+3VPO	

SYMBOL NO. 3 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V054E.F	02-44	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V054E	I	309		203	SENSO	
3V054F	PWR	119	(2)12/9,(2)12/10 (2)12/11,(2)12/12 (2)12/13,(2)12/14 (2)12/15,(2)12/16 (2)TO CONN CKT	203	+3VP1	
	PWR	012	(2)14/3	203	+3VP1	
	PWR	013	(2)14/3	203	+3VP1	
	PWR	014	(2)14/3	203	+3VP1	
	PWR	015	(2)14/3	203	+3VP1	
	PWR	016	(2)14/3	203	+3VP1	
	PWR	017	(2)14/3	203	+3VP1	
	PWR	018	(2)14/3	203	+3VP1	
	PWR	019	(2)14/3	203	+3VP1	
	PWR	212	(2)14/3	203	+3VP1	
	PWR	213	(2)14/3	203	+3VP1	
	PWR	214	(2)14/3	203	+3VP1	
	PWR	215	(2)14/3	203	+3VP1	
	PWR	216	(2)14/3	203	+3VP1	
	PWR	217	(2)14/3	203	+3VP1	
	PWR	218	(2)14/3	203	+3VP1	
	PWR	219	(2)14/3	203	+3VP1	
	I	010	(2)14/3	203	SENS1	
3V058F	PWR	012	14/6	203	+3VP1	
	PWR	013	14/6	203	+3VP1	
	PWR	014	14/6	203	+3VP1	
	PWR	015	14/6	203	+3VP1	
	PWR	016	14/6	203	+3VP1	
	PWR	017	14/6	203	+3VP1	
	PWR	018	14/6	203	+3VP1	
	PWR	019	14/6	203	+3VP1	
	PWR	119	14/6	203	+3VP1	
	PWR	212	14/6	203	+3VP1	
	PWR	213	14/6	203	+3VP1	
	PWR	214	14/6	203	+3VP1	
	PWR	215	14/6	203	+3VP1	
	PWR	216	14/6	203	+3VP1	
	PWR	217	14/6	203	+3VP1	
	PWR	218	14/6	203	+3VP1	
	PWR	219	14/6	203	+3VP1	
	I	010	14/6	203	SENS1	

SYMBOL NO. 4

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058A.B	06-01	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F058AB	OI	109	14/9 (X)TO CONN CKT	202	+12VREF	
	OI	210	14/4 TO CONN CKT	202	+12VREF	
3F058A	O	009	(X)TO CONN CKT		+3VREFO	
3F058B	O	310	TO CONN CKT		+3VREF1	
3G058A	O	008	(X)TO CONN CKT		+3VREGO	
3G058B	O	311	TO CONN CKT		+3VREG1	
3T058A	O	108		203	+12VRTNO	
	GRD	100		203	+3VRTNO	
	GRD	101		203	+3VRTNO	
	GRD	102		203	+3VRTNO	
	GRD	103		203	+3VRTNO	
	GRD	104		203	+3VRTNO	
	GRD	105		203	+3VRTNO	
	GRD	106		203	+3VRTNO	
	GRD	107		203	+3VRTNO	
	GRD	200	(X)TO CONN CKT	203	+3VRTNO	
	GRD	300		203	+3VRTNO	
	GRD	301		203	+3VRTNO	
	GRD	302		203	+3VRTNO	
	GRD	303		203	+3VRTNO	
	GRD	304		203	+3VRTNO	
	GRD	305		203	+3VRTNO	
	GRD	306		203	+3VRTNO	
	GRD	307		203	+3VRTNO	
3T058B	O	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	TO CONN CKT	203	+3VRTN1	
3V058A	PWR	000	(X)3/2,(X)3/3 (X)3/4,(X)3/5 (X)3/6 (X)TO CONN CKT	203	+3VPO	
	PWR	001	(X)14/4	203	+3VPO	
	PWR	002	(X)14/4	203	+3VPO	
	PWR	003	(X)14/4	203	+3VPO	
	PWR	004	(X)14/4	203	+3VPO	
	PWR	005	(X)14/4	203	+3VPO	
	PWR	006	(X)14/4	203	+3VPO	
	PWR	007	(X)14/4	203	+3VPO	
	PWR	201	(X)14/4	203	+3VPO	
	PWR	202	(X)14/4	203	+3VPO	
	PWR	203	(X)14/4	203	+3VPO	
	PWR	204	(X)14/4	203	+3VPO	

SYMBOL NO. 4 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058A.B	06-01	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V058A	PWR	205	(X)14/4	203	+3VPO	
	PWR	206	(X)14/4	203	+3VPO	
	PWR	207	(X)14/4	203	+3VPO	
	I	309	(X)14/4	203	SENSO	
3V058B	PWR	119	(W)3/2,(W)3/3 (W)3/4,(W)3/5 (W)3/6,(W)14/4 TO CONN CKT	203	+3VP1	
	PWR	000	14/4	203	+3VPO	
	PWR	001	14/4	203	+3VPO	
	PWR	002	14/4	203	+3VPO	
	PWR	003	14/4	203	+3VPO	
	PWR	004	14/4	203	+3VPO	
	PWR	005	14/4	203	+3VPO	
	PWR	006	14/4	203	+3VPO	
	PWR	007	14/4	203	+3VPO	
	PWR	012	14/4	203	+3VP1	
	PWR	013	14/4	203	+3VP1	
	PWR	014	14/4	203	+3VP1	
	PWR	015	14/4	203	+3VP1	
	PWR	016	14/4	203	+3VP1	
	PWR	017	14/4	203	+3VP1	
	PWR	018	14/4	203	+3VP1	
	PWR	019	14/4	203	+3VP1	
	PWR	201	14/4	203	+3VPO	
	PWR	202	14/4	203	+3VPO	
	PWR	203	14/4	203	+3VPO	
	PWR	204	14/4	203	+3VPO	
	PWR	205	14/4	203	+3VPO	
	PWR	206	14/4	203	+3VPO	
	PWR	207	14/4	203	+3VPO	
	PWR	212	14/4	203	+3VP1	
	PWR	213	14/4	203	+3VP1	
	PWR	214	14/4	203	+3VP1	
	PWR	215	14/4	203	+3VP1	
	PWR	216	14/4	203	+3VP1	
	PWR	217	14/4	203	+3VP1	
	PWR	218	14/4	203	+3VP1	
	PWR	219	14/4	203	+3VP1	
	1	010	14/4	203	SENS1	

PART OF FS 14
SYMBOL(S) 3 4

3A CENTRAL CONTROL	DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01	B14CB

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12/01/77

PART OF FS 14

POWER

SYMBOL NO. 5

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058D.E	06-02	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F058DE	DI	109	14/9 TO CONN CKT	202	+12VREF	
	DI	210	14/5	202	+12VREF	
3F058D	O	310	TO CONN CKT		+3VREF1	
3F058E	O	009	TO CONN CKT		+3VREF0	
3G058D	O	311	TO CONN CKT		+3VREG1	
3G058E	O	008	TO CONN CKT		+3VREG0	
3T058D	O	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	TO CONN CKT	203	+3VRTN1	
3T058E	O	108		203	+12VRTN0	
	GRD	100		203	+3VRTN0	
	GRD	101		203	+3VRTN0	
	GRD	102		203	+3VRTN0	
	GRD	103		203	+3VRTN0	
	GRD	104		203	+3VRTN0	
	GRD	105		203	+3VRTN0	
	GRD	106		203	+3VRTN0	
	GRD	107		203	+3VRTN0	
	GRD	200	TO CONN CKT	203	+3VRTN0	
	GRD	300		203	+3VRTN0	
	GRD	301		203	+3VRTN0	
	GRD	302		203	+3VRTN0	
	GRD	303		203	+3VRTN0	
	GRD	304		203	+3VRTN0	
	GRD	305		203	+3VRTN0	
	GRD	306		203	+3VRTN0	
	GRD	307		203	+3VRTN0	
3V058D	PWR	012		203	+3VP1	
	PWR	013		203	+3VP1	
	PWR	014		203	+3VP1	
	PWR	015		203	+3VP1	
	PWR	016		203	+3VP1	
	PWR	017		203	+3VP1	
	PWR	018		203	+3VP1	
	PWR	019		203	+3VP1	
	PWR	119	TO CONN CKT	203	+3VP1	
	PWR	212		203	+3VP1	
	PWR	213		203	+3VP1	
	PWR	214		203	+3VP1	
	PWR	215		203	+3VP1	
	PWR	216		203	+3VP1	
	PWR	217		203	+3VP1	

SYMBOL NO. 5 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058D.E	06-02	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V058D	PWR	218		203	+3VP1	
	PWR	219		203	+3VP1	
	I	010		203	SENS1	
3V058E	PWR	000	TO CONN CKT	203	+3VP0	
	PWR	001		203	+3VP0	
	PWR	002		203	+3VP0	
	PWR	003		203	+3VP0	
	PWR	004		203	+3VP0	
	PWR	005		203	+3VP0	
	PWR	006		203	+3VP0	
	PWR	007		203	+3VP0	
	PWR	201		203	+3VP0	
	PWR	202		203	+3VP0	
	PWR	203		203	+3VP0	
	PWR	204		203	+3VP0	
	PWR	205		203	+3VP0	
	PWR	206		203	+3VP0	
	PWR	207		203	+3VP0	
	I	309		203	SENS0	

SYMBOL NO. 6

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058C.F	06-44	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F058CF	DI	109	14/9 (2)TO CONN CKT	202	+12VREF	
	DI	210	14/6 TO CONN CKT	202	+12VREF	
3F058C	O	009	(2)TO CONN CKT		+3VREF0	
3F058F	O	310	TO CONN CKT		+3VREF1	
3G058C	O	008	(2)TO CONN CKT		+3VREG0	
3G058F	O	311	TO CONN CKT		+3VREG1	
3T058C	O	108		203	+12VRTN0	
	GRD	100		203	+3VRTN0	
	GRD	101		203	+3VRTN0	
	GRD	102		203	+3VRTN0	
	GRD	103		203	+3VRTN0	
	GRD	104		203	+3VRTN0	
	GRD	105		203	+3VRTN0	
	GRD	106		203	+3VRTN0	
	GRD	107		203	+3VRTN0	
	GRD	200	(2)TO CONN CKT	203	+3VRTN0	
	GRD	300		203	+3VRTN0	
	GRD	301		203	+3VRTN0	
	GRD	302		203	+3VRTN0	
	GRD	303		203	+3VRTN0	
	GRD	304		203	+3VRTN0	
	GRD	305		203	+3VRTN0	
	GRD	306		203	+3VRTN0	
	GRD	307		203	+3VRTN0	

SYMBOL NO. 6 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058C.F	06-44	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058F	O	211		203	+12VRTN1	
3T058F	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	TO CONN CKT	203	+3VRTN1	
3V058C	PWR	000	(2)12/1,(2)12/2 (2)12/3,(2)12/4 (2)12/5,(2)12/6 (2)12/7,(2)12/8 (2)TO CONN CKT	203	+3VP0	
	PWR	001	(2)14/6	203	+3VP0	
	PWR	002	(2)14/6	203	+3VP0	
	PWR	003	(2)14/6	203	+3VP0	
	PWR	004	(2)14/6	203	+3VP0	
	PWR	005	(2)14/6	203	+3VP0	
	PWR	006	(2)14/6	203	+3VP0	
	PWR	007	(2)14/6	203	+3VP0	
	PWR	201	(2)14/6	203	+3VP0	
	PWR	202	(2)14/6	203	+3VP0	
	PWR	203	(2)14/6	203	+3VP0	
	PWR	204	(2)14/6	203	+3VP0	
	PWR	205	(2)14/6	203	+3VP0	
	PWR	206	(2)14/6	203	+3VP0	
	PWR	207	(2)14/6	203	+3VP0	
	I	309	(2)14/6	203	SENS0	
3V058F	PWR	119	(Y)12/1,(Y)12/2 (Y)12/3,(Y)12/4 (Y)12/5,(Y)12/6 (Y)12/7,(Y)12/8 (Y)12/9,(Y)12/10 (Y)12/11,(Y)12/12 (Y)12/13,(Y)12/14 (Y)12/15,(Y)12/16 (Y)14/3,(Y)14/6 (Y)14/3,(Y)16/6 TO CONN CKT	203	+3VP1	
	PWR	000	14/6	203	+3VP0	
	PWR	001	14/6	203	+3VP0	
	PWR	002	14/6	203	+3VP0	
	PWR	003	14/6	203	+3VP0	
	PWR	004	14/6	203	+3VP0	
	PWR	005	14/6	203	+3VP0	
	PWR	006	14/6	203	+3VP0	
	PWR	007	14/6	203	+3VP0	
	PWR	012	14/6	203	+3VP1	
	PWR	013	14/6	203	+3VP1	
	PWR	014	14/6	203	+3VP1	
	PWR	015	14/6	203	+3VP1	
	PWR	016	14/6	203	+3VP1	

SYMBOL NO. 6 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V058C.F	06-44	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V058F	PWR	017	14/6	203	+3VP1	
	PWR	018	14/6	203	+3VP1	
	PWR	019	14/6	203	+3VP1	
	PWR	201	14/6	203	+3VP0	
	PWR	202	14/6	203	+3VP0	
	PWR	203	14/6	203	+3VP0	
	PWR	204	14/6	203	+3VP0	
	PWR	205	14/6	203	+3VP0	
	PWR	206	14/6	203	+3VP0	
	PWR	207	14/6	203	+3VP0	
	PWR	212	14/6	203	+3VP1	
	PWR	213	14/6	203	+3VP1	
	PWR	214	14/6	203	+3VP1	
	PWR	215	14/6	203	+3VP1	
	PWR	216	14/6	203	+3VP1	
	PWR	217	14/6	203	+3VP1	
	PWR	218	14/6	203	+3VP1	
	PWR	219	14/6	203	+3VP1	
	I	010	14/6	203	SENS1	
	I	309	14/6	203	SENS0	

PART OF FS 14
SYMBOL(S) 5 6

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

BELL LABORATORIES
SD-1C900-01
B14CC

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12/01/77

PART OF FS 14

POWER

SYMBOL NO. 7

3-VOLT REFERENCE AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V062C	10-01	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		010			SENS1	
		012			+3VP1	
		013			+3VP1	
		014			+3VP1	
		015			+3VP1	
		016			+3VP1	
		017			+3VP1	
		018			+3VP1	
		019			+3VP1	
		119			+3VP1	
		210			+12VREF	
		212			+3VP1	
		213			+3VP1	
		214			+3VP1	
		215			+3VP1	
		216			+3VP1	
		217			+3VP1	
		218			+3VP1	
		219			+3VP1	
		310			+3VREF1	
		311			+3VREG1	
12F062C	OI	109	14/9 TO CONN CKT	202	+12VREF	
3F062C	O	009	TO CONN CKT		+3VREF0	
3G062C	O	008	TO CONN CKT		+3VREG0	
3T062C	OT	108		203	+12VRTN0	
	OT	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	100		203	+3VRTN0	
	GRD	101		203	+3VRTN0	
	GRD	102		203	+3VRTN0	
	GRD	103		203	+3VRTN0	
	GRD	104		203	+3VRTN0	
	GRD	105		203	+3VRTN0	
	GRD	106		203	+3VRTN0	
	GRD	107		203	+3VRTN0	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	200	TO CONN CKT	203	+3VRTN0	
	GRD	300		203	+3VRTN0	
	GRD	301		203	+3VRTN0	
	GRD	302		203	+3VRTN0	
	GRD	303		203	+3VRTN0	
	GRD	304		203	+3VRTN0	
	GRD	305		203	+3VRTN0	
	GRD	306		203	+3VRTN0	
	GRD	307		203	+3VRTN0	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	

SYMBOL NO. 7 (CONT)

3-VOLT REFERENCE AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V062C	10-01	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062C	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319		203	+3VRTN1	
3V062C	PWR	000	TO CONN CKT	203	+3VP0	
	PWR	001		203	+3VP0	
	PWR	002		203	+3VP0	
	PWR	003		203	+3VP0	
	PWR	004		203	+3VP0	
	PWR	005		203	+3VP0	
	PWR	006		203	+3VP0	
	PWR	007		203	+3VP0	
	PWR	201		203	+3VP0	
	PWR	202		203	+3VP0	
	PWR	203		203	+3VP0	
	PWR	204		203	+3VP0	
	PWR	205		203	+3VP0	
	PWR	206		203	+3VP0	
	PWR	207		203	+3VP0	
	I	309		203	SENS0	

SYMBOL NO. 8

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V062A.B	10-29	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
12F062AB	OI	109	14/9 TO CONN CKT	202	+12VREF	
	OI	210	14/8 (X)TO CONN CKT	202	+12VREF	
3F062A	O	310	TO CONN CKT		+3VREF1	
3F062B	O	009	(X)TO CONN CKT		+3VREF0	
3G062A	O	311	TO CONN CKT		+3VREG1	
3G062B	O	008	(X)TO CONN CKT		+3VREG0	
3T062A	O	211		203	+12VRTN1	
	GRD	0GD		203	GRD	
	GRD	112		203	+3VRTN1	
	GRD	113		203	+3VRTN1	
	GRD	114		203	+3VRTN1	
	GRD	115		203	+3VRTN1	
	GRD	116		203	+3VRTN1	
	GRD	117		203	+3VRTN1	
	GRD	118		203	+3VRTN1	
	GRD	2GD		203	GRD	
	GRD	312		203	+3VRTN1	
	GRD	313		203	+3VRTN1	
	GRD	314		203	+3VRTN1	
	GRD	315		203	+3VRTN1	
	GRD	316		203	+3VRTN1	
	GRD	317		203	+3VRTN1	
	GRD	318		203	+3VRTN1	
	GRD	319	TO CONN CKT	203	+3VRTN1	

SYMBOL NO. 8 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V062A.B	10-29	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062B	O	108		203	+12VRTN0	
3T062B	GRD	100		203	+3VRTN0	
	GRD	101		203	+3VRTN0	
	GRD	102		203	+3VRTN0	
	GRD	103		203	+3VRTN0	
	GRD	104		203	+3VRTN0	
	GRD	105		203	+3VRTN0	
	GRD	106		203	+3VRTN0	
	GRD	107		203	+3VRTN0	
	GRD	200	(X)TO CONN CKT	203	+3VRTN0	
	GRD	300		203	+3VRTN0	
	GRD	301		203	+3VRTN0	
	GRD	302		203	+3VRTN0	
	GRD	303		203	+3VRTN0	
	GRD	304		203	+3VRTN0	
	GRD	305		203	+3VRTN0	
	GRD	306		203	+3VRTN0	
	GRD	307		203	+3VRTN0	
3V062A	PWR	119	(W)1/7,(W)2/6 (W)2/7,(W)2/9 (W)3/1,(W)14/8 TO CONN CKT	203	+3VP1	
	PWR	000	14/8	203	+3VP0	
	PWR	001	14/8	203	+3VP0	
	PWR	002	14/8	203	+3VP0	
	PWR	003	14/8	203	+3VP0	
	PWR	004	14/8	203	+3VP0	
	PWR	005	14/8	203	+3VP0	
	PWR	006	14/8	203	+3VP0	
	PWR	007	14/8	203	+3VP0	
	PWR	012	14/8	203	+3VP1	
	PWR	013	14/8	203	+3VP1	
	PWR	014	14/8	203	+3VP1	
	PWR	015	14/8	203	+3VP1	
	PWR	016	14/8	203	+3VP1	
	PWR	017	14/8	203	+3VP1	
	PWR	018	14/8	203	+3VP1	
	PWR	019	14/8	203	+3VP1	
	PWR	201	14/8	203	+3VP0	
	PWR	202	14/8	203	+3VP0	
	PWR	203	14/8	203	+3VP0	
	PWR	204	14/8	203	+3VP0	
	PWR	205	14/8	203	+3VP0	
	PWR	206	14/8	203	+3VP0	
	PWR	207	14/8	203	+3VP0	
	PWR	212	14/8	203	+3VP1	
	PWR	213	14/8	203	+3VP1	
	PWR	214	14/8	203	+3VP1	
	PWR	215	14/8	203	+3VP1	
	PWR	216	14/8	203	+3VP1	
	PWR	217	14/8	203	+3VP1	
	PWR	218	14/8	203	+3VP1	
	PWR	219	14/8	203	+3VP1	
	I	010	14/8	203	SENS1	
3V062B	PWR	000	(X)1/7,(X)2/6 (X)2/7,(X)2/9 (X)3/1 (X)TO CONN CKT	203	+3VP0	
	PWR	001	(X)14/8	203	+3VP0	
	PWR	002	(X)14/8	203	+3VP0	

SYMBOL NO. 8 (CONT)

3-VOLT REFERENCE
AND FILTER CIRCUIT (0,1)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
3V062A.B	10-29	FC21	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V062B	PWR	003	(X)14/8	203	+3VP0	
	PWR	004	(X)14/8	203	+3VP0	
	PWR	005	(X)14/8	203	+3VP0	
	PWR	006	(X)14/8	203	+3VP0	
	PWR	007	(X)14/8	203	+3VP0	
	PWR	201	(X)14/8	203	+3VP0	
	PWR	202	(X)14/8	203	+3VP0	
	PWR	203	(X)14/8	203	+3VP0	
	PWR	204	(X)14/8	203	+3VP0	
	PWR	205	(X)14/8	203	+3VP0	
	PWR	206	(X)14/8	203	+3VP0	
	PWR	207	(X)14/8	203	+3VP0	
	I	309	(X)14/8	203	SENS0	

PART OF FS 14
SYMBOL(S) 7 8

3A CENTRAL CONTROL

BELL LABORATORIES	SD-1C900-01	B14CD
DWG SIZE C2	ISSUE 7D	

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PART OF FS 14

POWER

SYMBOL NO. 9

+12 VOLT REFERENCE

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
+12VREF	10-28	FB152	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		002			+24A0	
		004			1RPA1	
		008			12VREF1	
		009			12VREF1	
		010			12VREF1	
		011			12VREF1	
		012			12VREF1	
		013			12VREF1	
		014			12VREF1	
		017			12VREF3	
		210			12VREF1	
		211			12VREF1	
		212			12VREF1	
		217			12VREF2	
NPA0	I	201	TO CONN CKT		NPA	
PAT0	I	215	TO CONN CKT		PAT	
PA1	0	203	TO CONN CKT		RPA1	
12F046	0	214	TO CONN CKT		12VREF1	
12F054AB	0	206	14/1	202	12VREF1	
12F054CD	0	205	14/2	202	12VREF1	
12F054EF	0	005	14/3	202	12VREF1	
12F058AB	0	208	14/4	202	12VREF1	
12F058CF	0	006	14/6	202	12VREF1	
12F058DE	0	207	14/5	202	12VREF1	
12F062AB	0	007	14/8	202	12VREF1	
12F062C	0	209	14/7	202	12VREF1	
12F070	0	213	TO CONN CKT		12VREF1	
24V0AA8	PWR	018			+24	
	PWR	218	TO CONN CKT		+24	
3T062B	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	219		203	GRD	
	GRD	319		203	GRD	
3VG1028T	GRD	219	TO CONN CKT		GRD	
5T039A	GRD	200	TO CONN CKT		GRD	

SYMBOL NO. 10

(SEE NOTE 210)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPARE	02-03	(NOTE 210)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T054A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		
3VG0203T	GRD	219				
	GRD	319				
3V054A	PWR	000	(X)14/1	203		
	PWR	019	(X)14/1	203		
3V054B	PWR	000	14/1			

SYMBOL NO. 10 (CONT)

(SEE NOTE 210)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPARE	02-03	(NOTE 210)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3V054B	PWR	019	14/1			

SYMBOL NO. 11

(SEE NOTE 209)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPARE	06-03	(NOTE 209)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		

SYMBOL NO. 12

(SEE NOTE 213)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS1	10-02	(NOTE 213)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	000		203		
	GRD	001		203		
	GRD	002		203		
	GRD	003		203		
	GRD	004		203		
	GRD	005		203		
	GRD	006		203		
	GRD	007		203		
	GRD	008		203		
	GRD	009		203		
	GRD	010		203		
	GRD	011		203		
	GRD	012		203		
	GRD	013		203		
	GRD	014		203		
	GRD	015		203		
	GRD	016		203		
	GRD	017		203		
	GRD	018		203		
	GRD	019		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	201		203		

SYMBOL NO. 12 (CONT)

(SEE NOTE 213)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS1	10-02	(NOTE 213)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	202		203		
	GRD	203		203		
	GRD	204		203		
	GRD	205		203		
	GRD	206		203		
	GRD	207		203		
	GRD	208		203		
	GRD	209		203		
	GRD	210		203		
	GRD	211		203		
	GRD	212		203		
	GRD	213		203		
	GRD	214		203		
	GRD	215		203		
	GRD	216		203		
	GRD	217		203		
	GRD	218		203		
	GRD	219		203		

SYMBOL NO. 13

(SEE NOTE 213)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS2	10-16	(NOTE 213)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062B	GRD	0GD		203		
	GRD	000		203		
	GRD	001		203		
	GRD	002		203		
	GRD	003		203		
	GRD	004		203		
	GRD	005		203		
	GRD	006		203		
	GRD	007		203		
	GRD	008		203		
	GRD	009		203		
	GRD	010		203		
	GRD	011		203		
	GRD	012		203		
	GRD	013		203		
	GRD	014		203		
	GRD	015		203		
	GRD	016		203		
	GRD	017		203		
	GRD	018		203		
	GRD	019		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	201		203		
	GRD	202		203		
	GRD	203		203		
	GRD	204		203		

SYMBOL NO. 13 (CONT)

(SEE NOTE 213)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS2	10-16	(NOTE 213)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062B	GRD	205		203		
	GRD	206		203		
	GRD	207		203		
	GRD	208		203		
	GRD	209		203		
	GRD	210		203		
	GRD	211		203		
	GRD	212		203		
	GRD	213		203		
	GRD	214		203		
	GRD	215		203		
	GRD	216		203		
	GRD	217		203		
	GRD	218		203		
	GRD	219		203		

PART OF FS 14
SYMBOL(S) 9 10 11 12 13

3A CENTRAL CONTROL

DWG SIZE C2
ISSUE 7D

BELL LABORATORIES
SD-1C900-01
814CE

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PART OF FS 14

POWER

SYMBOL NO. 14

(SEE NOTE 214)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS3	10-17	(NOTE 214)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062C	GRD	0GD		203		
	GRD	000		203		
	GRD	001		203		
	GRD	002		203		
	GRD	003		203		
	GRD	004		203		
	GRD	005		203		
	GRD	006		203		
	GRD	007		203		
	GRD	008		203		
	GRD	009		203		
	GRD	010		203		
	GRD	012		203		
	GRD	013		203		
	GRD	014		203		
	GRD	015		203		
	GRD	016		203		
	GRD	017		203		
	GRD	018		203		
	GRD	019		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	201		203		
	GRD	202		203		
	GRD	203		203		
	GRD	204		203		
	GRD	205		203		
	GRD	206		203		
	GRD	207		203		
	GRD	208		203		
	GRD	209		203		
	GRD	210		203		
	GRD	211		203		
	GRD	212		203		
	GRD	213		203		
	GRD	214		203		
	GRD	215		203		
	GRD	216		203		
	GRD	217		203		
	GRD	218		203		
	GRD	219		203		
3VG1017T	GRD	011				
	GRD	012				

SYMBOL NO. 15

(SEE NOTE 215)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS4	10-18	(NOTE 215)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		

SYMBOL NO. 16

(SEE NOTE 215)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS5	10-19	(NOTE 215)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		

SYMBOL NO. 17

(SEE NOTE 211)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS6	10-20	(NOTE 211)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062B	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		

SYMBOL NO. 18

(SEE NOTE 211)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS7	10-21	(NOTE 211)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062B	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		

SYMBOL NO. 19

(SEE NOTE 209)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPARE	10-24	(NOTE 209)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		
3V062A	PWR	000		203		
	PWR	119		203		

SYMBOL NO. 20

(SEE NOTE 209)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPARE	10-25	(NOTE 209)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		
3V062A	PWR	000		203		
	PWR	119		203		

SYMBOL NO. 21

(SEE NOTE 212)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS8	10-26	(NOTE 212)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		
3V062A	PWR	000		203		
	PWR	119		203		

SYMBOL NO. 22

(SEE NOTE 212)

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS9	10-27	(NOTE 212)	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T062A	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203		
	GRD	319		203		
3V062A	PWR	000		203		
	PWR	119		203		

PART OF FS 14
SYMBOL(S) 14 15 16 17 18 19 20 21 22

3A CENTRAL CONTROL

		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B14CF

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PART OF FS 14

POWER

SYMBOL NO. 23

+5A LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
+5A	09-36T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
5V061A	PWR	+5A	(Y)12/1,(Y)12/2 (Y)12/3,(Y)12/4 (Y)14/25 TO CONN CKT	203		

SYMBOL NO. 24

GDA LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GDA	09-37T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058C	GRD	GDA		203		

SYMBOL NO. 25

+5B LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
+5B	09-38T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
5V061A	PWR	+5B	14/23	203		
5V061B	PWR	+5B	(2)12/1,(2)12/2 (2)12/3,(2)12/4 (2)TO CONN CKT	203		

SYMBOL NO. 26

+5C LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
+5C	09-41T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
5V061C	PWR	+5C	(Y)12/9,(Y)12/10 (Y)12/11,(Y)12/12 (Y)14/28 TO CONN CKT	203		

SYMBOL NO. 27

GDC LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GDC	09-42T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058C	GRD	GDC		203		

SYMBOL NO. 28

+5D LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
+5D	09-43T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
5V061C	PWR	+5D	14/26	203		
5V061D	PWR	+5D	(2)12/9,(2)12/10 (2)12/11,(2)12/12 (2)TO CONN CKT	203		

SYMBOL NO. 29

GDD LUG

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
GDD	09-44T	840851778		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
3T058C	GRD	GDD		203		

PART OF FS 14
SYMBOL(S) 23 24 25 26 27 28 29

3A CENTRAL CONTROL

3A CENTRAL CONTROL		DWG SIZE C2	ISSUE 7D
BELL LABORATORIES	SD-1C900-01		B14CG

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12/01/77

PART OF APP FIG. 1

CIRCUIT PACK

EQPT LOC	02-01		02-02		02-03		02-08		02-09		02-10		02-11		02-12		02-13		02-14		02-16		02-17		02-18		EQPT LOC
DESIG	3V054A.B		TCHECKER		SPARE														3V054C.D								DESIG
CODE	FC21		FA1031		(NOTE 210)		FA1024		FA1024		FA1024		FA1024		FA1024		FA1024		FC21		FA1024		FA1024		FA1024		CODE
OPTION																											OPTION
ELEM IDENT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		14/1		6/1		14/10	STBT0800	4/15	STBT0901	4/14	STBT1002	4/13	STBT1103	4/12	STBT1204	4/11	STBT1305	4/10		14/2	STBT1406	4/9	STBT1507	4/8	STBTPHPL	4/5	A
B							MTBT0800	7/18	MTBT0901	7/17	MTBT1002	7/16	MTBT1103	7/15	MTBT1204	7/14	MTBT1305	7/13			MTBT1406	7/12	MTBT1507	7/11	MTBTPHPL	7/8	B
C																											C
D																											D
E																											E
F																											F

CIRCUIT PACK

EQPT LOC	02-19		02-20		02-21		02-22		02-23		02-24		02-25		02-26		02-27		02-28		02-29		02-31		02-32		EQPT LOC
DESIG					PBC0		PBC1										MCHCNTRL		MCH21-11		MCH10-00				MC B7		DESIG
CODE	FA1030		FA1030		FA1029		FA1029		FA1046		FA1033		FA1032		FC202		FA1037		FA1036		FA1035		FA1023		FA1022		CODE
OPTION																											OPTION
ELEM IDENT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A	STBT1816	4/7	STBT1917	4/6		4/1		4/3	DSR	4/2	PT.TC	8/4	MRFLOGIC	7/19	TRNSFINT	9/1		9/4		9/2		9/3	MC B8	1/6		1/3	A
B	MTBT1816	7/10	MTBT1917	7/9					MISCDECE	1/10	C.TA.LOG	7/3	BACK.MSB	6/4	SSPTRNSF	7/21							ID CHCHK	6/5			B
C	MISCDECC	1/12	MISCDECD	1/14									ADRPTPRD	4/4									REG.SEL	7/2			C
D	SPR18.16	5/6	SPR19 17	5/5									INTRPLOG	5/3													D
E																											E
F																											F

CIRCUIT PACK

EQPT LOC	02-33		02-34		02-35		02-36		02-37		02-38		02-39		02-40		02-41		02-42		02-43		02-44		06-01		EQPT LOC
DESIG	MC B3		MC B2		MC B1		MP0.0		MP1.0		MP2.0		MP3.0		MP4.0		MP5.0		MP6.0		MP7.0		3V054E.F		3V058A.B		DESIG
CODE	FA1018		FA1017		FA1016		(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)		FC21		FC21		CODE
OPTION																											OPTION
ELEM IDENT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		1/1		1/2		1/3		12/8		12/6		12/4		12/2		12/16		12/14		12/12		12/10		14/3		14/4	A
B																											B
C																											C
D																											D
E																											E
F																											F

CIRCUIT PACK

EQPT LOC	06-02		06-03		06-04		06-06		06-09		06-10		06-11		06-12		06-13		06-14		06-16		06-17		06-18		EQPT LOC
DESIG	3V0580.E		SPARE		FCHECKER																						DESIG
CODE	FC21		(NOTE 209)		FA1031		FA1034		FA1010		FA1010		FA1010		FA1010		FA1010		FA1010		FA1010		FA1010		FA1010		CODE
OPTION																											OPTION
ELEM IDENT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		14/5		14/11		6/2	CPANITRF	7/1	GRBT0800	3/9	GRBT0901	3/8	GRBT1002	3/7	GRBT1103	3/6	GRBT1204	3/5	GRBT1305	3/4	GRBT1406	3/3	GRBT1507	3/2	GRBTPHPL	3/1	A
B							MTHENLGC	7/7	SPR08.00	5/14	SPR09.01	5/13	SPR10.02	5/12	SPR11.03	5/11	SPR12.04	5/10	SPR13.05	5/9	SPR14.06	5/8	SPR15.07	5/7	SPRPH.PL	5/4	B
C							SSPINTRF	7/22																			C
D							MISCDECB	1/9																			D
E							MISCKT	7/6																			E
F							DISENBPO	7/20																			F

ISSUE
6D

3A CENTRAL CONTROL

BELL TELEPHONE LABORATORIES
INCORPORATED

DWG SIZE
C2

SD-1C900-01-C1

PART OF APP FIG. 1

CIRCUIT PACK

EQPT LOC	06-19		06-20		06-21		06-22		06-23		06-24		06-25	
DESIG	MC B5				DML11916		DML11508		DML1RPHG		DML10700		DML01508	
CODE	FA1020		FA1026		FA1013		FA1012		FA1015		FA1012		FA1012	
OPTION														
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		CKT	
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM
A		1/7	DMLMATCH	2/9		2/6		2/7		2/5		2/8		2/3
B			GBPCHECK	6/3										
C														
D														
E														
F														

EQPT LOC	06-26		06-27		06-28		06-29		06-31		06-32		EQPT LOC
DESIG	DMLORPLG		DML00700		DML01916				CLOCK		MC B4		DESIG
CODE	FA1015		FA1012		FA1014		FB486		FA1025		FA1019		CODE
OPTION													OPTION
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		2/1		2/4		2/2	CRYS OSC	8/1		8/3		1/4	A
B							TTMO	8/2					B
C							IOTIM	8/5					C
D													D
E													E
F													F

CIRCUIT PACK

EQPT LOC	06-33		06-34		06-35		06-36		06-37		06-38		06-39	
DESIG	FDECODER		TDECODER		MC B6		MP0.1		MP1.1		MP2.1		MP3.1	
CODE	FA1011		FA1045		FA1021		(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)	
OPTION														
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		CKT	
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM
A		1/13		1/11		1/5		12/7		12/5		12/3		12/1
B														
C														
D														
E														
F														

EQPT LOC	06-40		06-41		06-42		06-43		06-44		10-01		EQPT LOC
DESIG	MP4.1		MP5.1		MP6.1		MP7.1		3V058C.F		3V062C		DESIG
CODE	(NOTE 216)		(NOTE 216)		(NOTE 216)		(NOTE 216)		FC21		FC21		CODE
OPTION													OPTION
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		12/15		12/13		12/11		12/9		14/6		14/7	A
B													B
C													C
D													D
E													E
F													F

CIRCUIT PACK

EQPT LOC	10-02		10-03		10-04		10-05		10-06		10-16		10-17	
DESIG	TS1		IOS00		IOD00		IO00SCA		IO00SCB		TS2		TS3	
CODE	(NOTE 213)		FA1038		FA1039		FC201		FC201		(NOTE 213)		(NOTE 214)	
OPTION														
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		CKT	
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM
A		14/12		10/1		10/2		10/3		10/4		14/13		14/14
B														
C														
D														
E														
F														

EQPT LOC	10-18		10-19		10-20		10-21		10-22		10-23		EQPT LOC
DESIG	TS4		TS5		TS6		TS7						DESIG
CODE	(NOTE 215)		(NOTE 215)		(NOTE 211)		(NOTE 211)		FA1028		FA1027		CODE
OPTION													OPTION
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		14/15		14/16		14/17		14/18	DBHL1910	7/4	D309-00	7/5	A
B									ERHL1910	5/1	E309-00	5/2	B
C													C
D													D
E													E
F													F

CIRCUIT PACK

EQPT LOC	10-24		10-25		10-26		10-27		10-28		10-29		EQPT LOC
DESIG	SPARE		SPARE		TS8		TS9		+12VREF		3V062A.B		DESIG
CODE	(NOTE 209)		(NOTE 209)		(NOTE 212)		(NOTE 212)		FB152		FC21		CODE
OPTION													OPTION
ELEM IDENT	CKT		CKT		CKT		CKT		CKT		CKT		ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		14/19		14/20		14/21		14/22		14/9		14/8	A
B													B
C													C
D													D
E													E
F													F

ISSUE
6D

3A CENTRAL CONTROL

BELL TELEPHONE LABORATORIES
INCORPORATED

DWG SIZE
C2

SD-1C900-01-C2

SD-1C900-01-C2

APP FIG. 2

CIRCUIT PACK

EQPT LOC	02-05		02-06		02-07		EQPT LOC
DESIG	STBT2116		STBT2722		STBTPH28		DESIG
CODE	FA1040		FA1040		FA1040		CODE
OPTION							OPTION
ELEM IDENT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		11/3		11/2		11/1	A
B							B
C							C
D							D
E							E
F							F

APP FIG. 3

CIRCUIT PACK

EQPT LOC	10-07		10-08		10-09		10-10		EQPT LOC
DESIG	IOS01		IOD01		IO01SCA		IO01SCB		DESIG
CODE	FA1038		FA1039		FC201		FC201		CODE
OPTION									OPTION
ELEM IDENT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		10/5		10/6		10/7		10/8	A
B									B
C									C
D									D
E									E
F									F

APP FIG. 4

CIRCUIT PACK

EQPT LOC	10-11		10-12		10-13		10-14		EQPT LOC
DESIG	IOS02		IOD02		IO02SCA		IO02SCB		DESIG
CODE	FA1038		FA1039		FC201		FC201		CODE
OPTION									OPTION
ELEM IDENT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		10/9		10/10		10/11		10/12	A
B									B
C									C
D									D
E									E
F									F

APP FIG. 5

CIRCUIT PACK

EQPT LOC	02-04		06-05		06-07		06-08		EQPT LOC
DESIG	PROT03		PROT00		PROT01		PROT02		DESIG
CODE	FB6		FB6		FB6		FB6		CODE
OPTION									OPTION
ELEM IDENT		CKT		CKT		CKT		CKT	ELEM IDENT
CKT	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	DESIG	FS/SYM	CKT
A		13/4		13/1		13/2		13/3	A
B									B
C									C
D									D
E									E
F									F

ISSUE
6D

3A CENTRAL CONTROL

BELL TELEPHONE LABORATORIES
INCORPORATED

DWG SIZE
C2

SD-1C900-01-C3

CIRCUIT NØTES:

101.

DESIG	FUSE AMP	PØTENTIAL	ØNE PER
+24V0AA8	1-1/3	+24	APP FIG. 1
+24V0AA9	1-1/3	+24	APP FIG. 1

BATTERY SYMBØL	VØLTAGE RANGE
+24	20.75-26.25

102.

FEATURE ØR ØPTIØN		PRØVIDE		
		APP FIG	APP ØR WRG	QUANTITY
3A CENTRAL CONTROL CKT		1		1 PER CKT
EXPANDED MAIN MEMORY INTERFACE, EXPANDS 18 BIT STORE DATA BUS TO 26 DATA BITS		2		
GROWTH I/O MAIN CHANNEL	CHANNEL 01	3		
	CHANNEL 02	4		
PROTECTION CKT FOR DUPLEX OPERATION		5		
POWER WIRING FOR MICROPROGRAM STORE CIRCUIT PACKS	512 WORDS PER BOARD		Z	
	1024 WORDS PER BOARD		Y	
POWER WIRING FOR 4 TO 8 AMP POWER CONVERTER CHANGE	4 AMP CONVERTER J87389F (A8)		X	
	8 AMP CONVERTER J87389P (A19)		W	

103.

RECØRD ØF FIGURES, WIRING AND APPARATUS CHANGES

CHANGED ØN ISSUE	IF JØB RECORDS DØ NØT SPECIFY	THIS ØPTIØN WAS FURN	SEE NØTE	USE IN CIRCUIT		
				STD	A&M	MD
6D	Z OR Y	Z		Y	Z	
7D	X OR W	X		W		X

3A CENTRAL CØNTRØL

DWG SIZE	ISSUE
6S	7D

BELL LABORATORIES | SD-1C900-01 | D1

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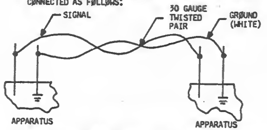
EQUIPMENT NOTES:

201. UNLESS OTHERWISE SPECIFIED, IF A NET HAS A TOTAL NET WIRING DISTANCE GREATER THAN 7.0 INCHES, NET SEGMENTS WITH A WIRING DISTANCE GREATER THAN 6.0 INCHES SHALL REQUIRE 30 GAUGE SEMIAUTOMATICALLY INSTALLED TWISTED PAIR, D2 OR D4-TYPE WIRING WHICH TERMINATES ON COAXIAL TERMINATING FIELD TERMINALS OR DIRECTLY ON THE APPARATUS. ALL OTHER NET SEGMENTS SHALL BE 30 GAUGE AUTOMATICALLY INSTALLED D4-TYPE WIRING. (SEE NOTES 204, 205, 206, 207).

202. ALL CONNECTIONS BETWEEN TERMINALS IN THIS NET SHALL BE 30 GAUGE AUTOMATICALLY INSTALLED D4-TYPE WIRING.

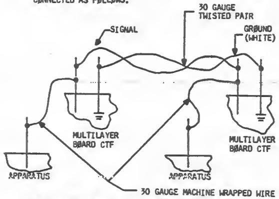
203. WIRING SHALL BE PRINTED WIRING PLANES LOCATED IN MULTILAYER PRINTED WIRING BOARD, ED-4C018-01. PRINTED WIRING NETS 3T054A AND 3T0588 SHALL CONTAIN A 30 GAUGE, AUTOMATICALLY INSTALLED WIRE TO TERMINAL 219 OF EACH FB6 CIRCUIT PACK. ALL 3V POWER NETS SHALL CONTAIN A 30 GAUGE, AUTOMATICALLY INSTALLED WIRE TO IT'S RESPECTIVE SENSE TERMINAL (309 OR 010) OF EACH FC21 CIRCUIT PACK.

204. THE TWO TERMINALS TO BE CONNECTED ARE SUCH THAT BOTH TERMINALS HAVE ADJACENT GROUND TERMINALS. THE RESULTING SIGNAL-GROUND TWISTED PAIR (TG) IS TO BE CONNECTED AS FOLLOWS:



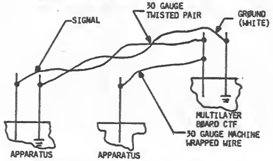
THE ADJACENT GROUND TERMINALS ARE CONNECTED TO GROUND VIA THE CIRCUIT PACK OR A 30 GAUGE MACHINE WRAPPED WIRE FROM CIRCUIT PACK GROUND ON THE CORRESPONDING CIRCUIT PACK HALF.

205. THE TWO TERMINALS TO BE CONNECTED ARE SUCH THAT NEITHER TERMINAL HAS AN ADJACENT GROUND. THE RESULTING SIGNAL-GROUND TWISTED PAIR (TG) IS TO BE CONNECTED AS FOLLOWS:



THE ADJACENT COAXIAL TERMINATION FIELD GROUND TERMINALS ARE CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD.

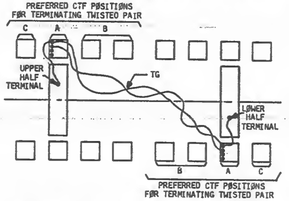
206. THE TWO TERMINALS TO BE CONNECTED ARE SUCH THAT ONE HAS AN ADJACENT GROUND AND THE SECOND DOES NOT. THE RESULTING SIGNAL-GROUND TWISTED PAIR (TG) IS TO BE CONNECTED AS FOLLOWS:



THE ADJACENT CTF GROUND TERMINAL IS CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD. THE ADJACENT APPARATUS GROUND TERMINAL IS CONNECTED TO GROUND VIA THE CIRCUIT PACK OR A 30 GAUGE MACHINE WRAPPED WIRE FROM CIRCUIT PACK GROUND ON THE CORRESPONDING CIRCUIT PACK HALF.

207. WHEREVER POSSIBLE APPARATUS TERMINALS (SIGNAL) LOCATED IN THE UPPER HALF OF THE CIRCUIT PACK CONNECTOR SHALL UTILIZE THE UPPER COAXIAL TERMINATION FIELDS AND APPARATUS TERMINALS (SIGNAL) LOCATED IN THE LOWER HALF OF THE CIRCUIT CONNECTOR SHALL UTILIZE THE LOWER COAXIAL TERMINATION FIELDS. PREFERRED COAXIAL TERMINATION FIELD POSITIONS (TO PICK UP ADJACENT GROUNDS) ARE IN ORDER OF PREFERENCE:

A) DIRECTLY ABOVE OR BELOW THE CONNECTOR POSITION.
B) TWO POSITIONS IN THE DIRECTION OF THE SECOND TERMINAL.
C) ONE POSITION IN THE OPPOSITE DIRECTION FROM THE SECOND TERMINAL.


PREFERRED CTF POSITIONS FOR TERMINATING TWISTED PAIR
C
A
B
UPPER HALF TERMINAL
TG
LOWER HALF TERMINAL
B
A
C
PREFERRED CTF POSITIONS FOR TERMINATING TWISTED PAIR

208. TERMINALS 100-118 AND 301-319 ARE GROUNDED VIA THE MULTILAYER PRINTER WIRING BOARD GROUND PLANES AND ARE PART OF AN 82-PIN (947C) CONNECTOR WHICH ARE NOT USED BY THE 42-PIN (9468) CONNECTOR WHICH MATES WITH IT. THESE TERMINALS ARE USED FOR TWISTED PAIR GROUND TERMINATIONS WHERE REQUIRED. SEE POWER DISTRIBUTION TABLES.

209. CIRCUIT PACK CAN BE MOUNTED IN THIS POSITION. TERMINALS 200, 319, OGD AND 2GD ARE CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD. TERMINALS 000 AND 119 ARE CONNECTED TO POWER (+3) VIA THE MULTILAYER PRINTED WIRING BOARD FOR POSITIONS 02-23, 10-24, AND 10-25 ONLY. SEE POWER DISTRIBUTION TABLES.

210. CIRCUIT PACK POSITION 02-03 SHALL BE RESERVED FOR AN FB6 CIRCUIT PACK. TERMINALS 200, 319, OGD AND 2GD ARE GROUNDED VIA THE MULTILAYER PRINTED WIRING BOARD. TERMINALS 000 AND 019 ARE CONNECTED TO POWER (+3) VIA MULTILAYER PRINTED WIRING BOARD. SEE POWER DISTRIBUTION TABLE.

211. CIRCUIT PACK POSITIONS 10-20 AND 10-21 SHALL BE USED AS TERMINAL STRIPS FOR CABLING TO THE 3A CC CONTROL PANEL. NO CIRCUIT PACK SHALL BE MOUNTED IN EITHER OF THESE POSITIONS. TERMINALS 200, 319, OGD AND 2GD ARE CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD. SEE POWER DISTRIBUTION TABLES.

212. CIRCUIT PACK POSITIONS 10-26 AND 10-27 SHALL BE USED AS TERMINAL STRIPS FOR 3A CC TEST SET. NO CIRCUIT PACK SHALL BE MOUNTED IN EITHER OF THESE POSITIONS. TERMINALS 200, 319, OGD AND 2GD ARE CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD. TERMINALS 000 AND 119 ARE CONNECTED TO POWER (+3) VIA THE MULTILAYER PRINTED WIRING BOARD. SEE POWER DISTRIBUTION TABLES AND NOTE 315.

213. CIRCUIT PACK POSITIONS 10-02 AND 10-16 SHALL BE USED AS TERMINAL STRIPS FOR I/O MAIN CHANNELS 0 AND 2 RESPECTIVELY. NO CIRCUIT PACK SHALL BE MOUNTED IN EITHER OF THESE POSITIONS. TERMINALS 000-119, 200-219 OGD AND 2GD ARE CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD. SEE POWER DISTRIBUTION TABLES.

214. CIRCUIT PACK POSITION 10-17 SHALL BE USED AS A TERMINAL STRIP FOR CABLING TO THE SYSTEMS STATUS, TTYC, TDC AND I/O CIRCUITS. NO CIRCUIT PACK SHALL BE MOUNTED IN THIS POSITION. TERMINALS 000-010, 012-019, 200-219, OGD AND 2GD ARE CONNECTED TO GROUND VIA THE MULTILAYER PRINTED WIRING BOARD (MLPWB). SEE POWER DISTRIBUTION TABLES.

215. CIRCUIT PACK POSITIONS 10-18 AND 10-19 ARE USED AS TERMINAL STRIPS FOR CABLING TO THE FIELD DIAGNOSTIC TEST SET. NO CIRCUIT PACK SHALL BE MOUNTED IN EITHER OF THESE POSITIONS. TERMINALS 200,319,OGD AND 2GD ARE CONNECTED TO GROUND VIA THE MLPWB. SEE POWER DISTRIBUTION TABLES.

216. THESE POSITIONS ARE RESERVED FOR MICROSTORE CIRCUIT PACKS WHICH MAY BE EQUIPPED AT THE FRAME LEVEL.

POSITION	512 WORD CP	1024 WORD CP
	PROVIDES WORDS	
02-36,06-36	0-511	-
02-37,06-37	512-1023	0-1023
02-38,06-38	1024-1535	-
02-39,06-39	1536-2047	1024-2047
02-40,06-40	2048-2559	-
02-41,06-41	2560-3071	2048-3071
02-42,06-42	3072-3583	-
02-43,06-43	3584-4095	3072-4095

3A CENTRAL CONTROL ②

DWG SIZE 6S

ISSUE 7D

BELL LABORATORIES

SD-1C900-01

D2

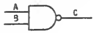
INFORMATION NOTES:

301. UNLESS ØTHERWISE SPECIFIED:
VALUES PRECEDED BY THE SYMBØL +(PLUS) ØR-(MINUS) ARE IN VOLTS.

302. THE FOLLOWING SYMBOLS ARE USED WITHIN THE COMPOSITE DIAGRAMS TO ABBREVIATE THE DESCRIPTION OF THE LOGIC FUNCTIONS DESCRIBED.

SYMBOL — FUNCTION

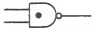
(A)



NAND GATE

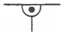
TRUTH TABLE	
A,B	C
00	1
01	1
10	1
11	0

(B)



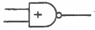
"AND" FUNCTION WITH RESULT COMPLEMENTED (A ONE IS HIGH SIGNAL LEVEL ON GATE INPUT)

(C)



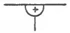
COLLECTOR TIE POINT (A ONE IS HIGH SIGNAL LEVEL AT COLLECTOR TIE)

(D)



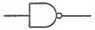
"OR" FUNCTION WITH RESULT COMPLEMENTED (A ONE IS LOW SIGNAL LEVEL AT GATE INPUT)

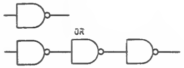
(E)



"OR" FUNCTION AT A COLLECTOR TIE POINT (A ONE IS LOW SIGNAL LEVEL AT COLLECTOR TIE)

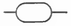
(F)



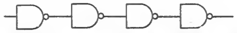


(G)

4 GATES DELAYS



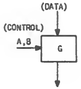
(SEE NOTE 1)

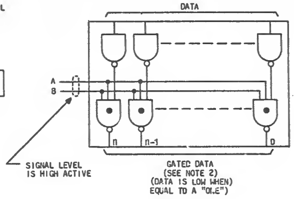


(UNLESS EXPLICITLY STATED ONLY LOGIC POLARITIES ARE PRESERVED AND THEIR GATE DELAYS ARE NOT SHOWN)

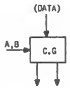
SYMBOL — FUNCTION

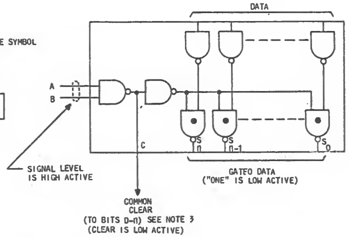
(H) GATING SYMBOL



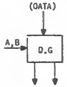

DATA
A
B
SIGNAL LEVEL IS HIGH ACTIVE
n
n-1
0
GATED DATA (SEE NOTE 2) (DATA IS LOW WHEN EQUAL TO A "ONE")

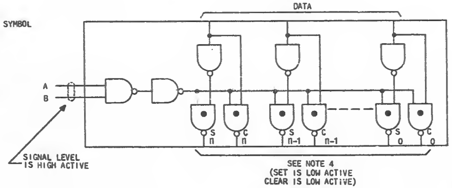
(J) CLEAR AND GATE SYMBOL




DATA
A
B
C
S n
S n-1
S 0
SIGNAL LEVEL IS HIGH ACTIVE
GATED DATA ("ONE" IS LOW ACTIVE)
COMMON CLEAR (TO BITS 0-n) SEE NOTE 3 (CLEAR IS LOW ACTIVE)

(K) DUAL RAIL GATE SYMBOL




DATA
A
B
S n
C n
S n-1
C n-1
S 0
C 0
SIGNAL LEVEL IS HIGH ACTIVE
SEE NOTE 4 (SET IS LOW ACTIVE CLEAR IS LOW ACTIVE)

NOTES:

1. THIS DELAY ELEMENT SYMBOL IS USED ONLY IN FS 4 WHERE EXPLICIT DELAYS ARE REQUIRED FOR MAIN STORE BUS TIMING.

2. THE GATING SYMBOL IS USED TO INDICATE A PARALLEL GATING PATH ENABLE FUNCTION. IT IS TYPICALLY USED TO GATE FROM A SOURCE REGISTER TO THE GB WITH THE FROM-FIELD DECODER PROVIDING THE CONTROL SIGNAL (SEE SHEET B3GB FOR A DETAIL DESCRIPTION).

3. THE CLEAR AND GATE SYMBOL IS USED TO INDICATE A SIMULTANEOUSLY CLEAR AND GATE TO A REGISTER ON A PARALLEL INPUT BASIS. IT IS TYPICALLY USED TO GATE THE GB TO A DESTINATION REGISTER WITH THE TØ-FIELD DECODER PROVIDING THE CONTROL SIGNAL (SEE SHEET B3GB FOR A DETAIL DESCRIPTION).

4. THE DUAL RAIL GATE SYMBOL IS USED TO INDICATE A DUAL RAIL GATING OPERATION INTO A REGISTER ON A PARALLEL BASIS. IN DUAL RAIL GATING THE INDIVIDUAL BITS OF A REGISTER (I.e. BITS 0-n GET INDIVIDUAL SET AND CLEAR INPUT SIGNALS. NOTE THAT FOR THE CLEAR AND GATE OPERATION ALL BITS OF THE REGISTER (I.e. BITS 0-n) ARE FIRST CLEARED BEFORE THEY ARE GATED INTO. THEREFORE THE DUAL RAIL GATING OPERATION IS TYPICALLY USED FOR THOSE REGISTERS THAT CANNOT HAVE THEIR CONTENTS PASSED THROUGH A TRANSIENT STATE IN THE PROCESS OF GATING TO THEM. THE MMS REGISTER DESCRIBED ON SHEET B4GB IS SUCH A REGISTER. THE SS AND THE IS REGISTERS ALSO CANNOT PASS THROUGH A TRANSIENT STATE WHEN GATING TO THEM. FOR THESE TWO REGISTERS AN ALTERNATE TECHNIQUE TO DUAL RAIL GATING IS USED (SEE SHEET B5GE FOR DETAILS).

3A CENTRAL CONTROL (2)

DWG SIZE 6S

ISSUE 4A

BELL LABORATORIES

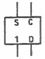
SD-1C900-01

D3

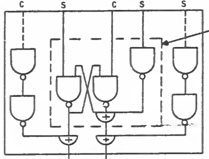
INFORMATION NOTES: (CONT)

302. (CONT)

(L)



A LOW LEVEL SIGNAL WILL SET OR CLEAR R-S FLIP-FLOP RESPECTIVELY

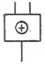


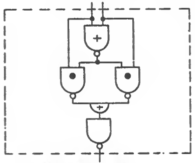
THIS LOGIC IS TYPICAL CONTAINED WITH A TWO BIT REGISTER DEVICE (SEE SHT.B3GB)

"1" "0"

R-S FLIP-FLOP

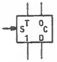
(R)

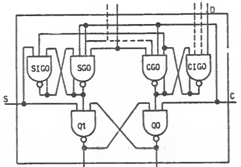




EXCLUSIVE "OR" FUNCTION

(M)

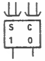




"1" "0"

GATED DELAY FLIP-FLOP

(S)



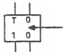
SAME AS SYMBOL (L) EXCEPT WITH MULTIPLE INPUTS TO THE SET AND CLEAR INPUTS. AN "OR" FUNCTION IS PERFORMED ON THE MULTIPLE INPUTS TO THE SET AND CLEAR INPUTS RESPECTIVELY.

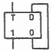
THAT IS, ANY ONE OF THE INPUTS LOW ACTIVE TO THE SET SIDE WILL SET THE FLIP-FLOP. SIMILARLY FOR THE CLEAR INPUT.

(T)

SAME AS SYMBOL (M) EXCEPT WITH MULTIPLE INPUTS TO THE T AND D INPUTS. AN "AND" FUNCTION IS PERFORMED ON THE MULTIPLE INPUTS TO THE T AND D INPUTS RESPECTIVELY. THAT IS, ALL INPUTS TO THE T INPUT MUST BE HIGH ACTIVE BEFORE THE DATA ON THE D INPUT WILL BE STROBED ON THE FLIP-FLOP. SIMILARLY ALL D INPUTS MUST BE HIGH ACTIVE BEFORE A ONE IS STROBED INTO THE FLIP-FLOP.

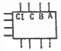
(N)



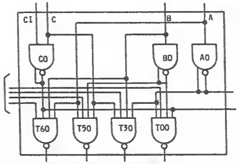


GATED DELAY FLIP-FLOP AS A BINARY CELL

(P)



THESE INPUTS DEFINE FUNCTION TO BE PERFORMED



GENERAL PURPOSE TRANSLATOR

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

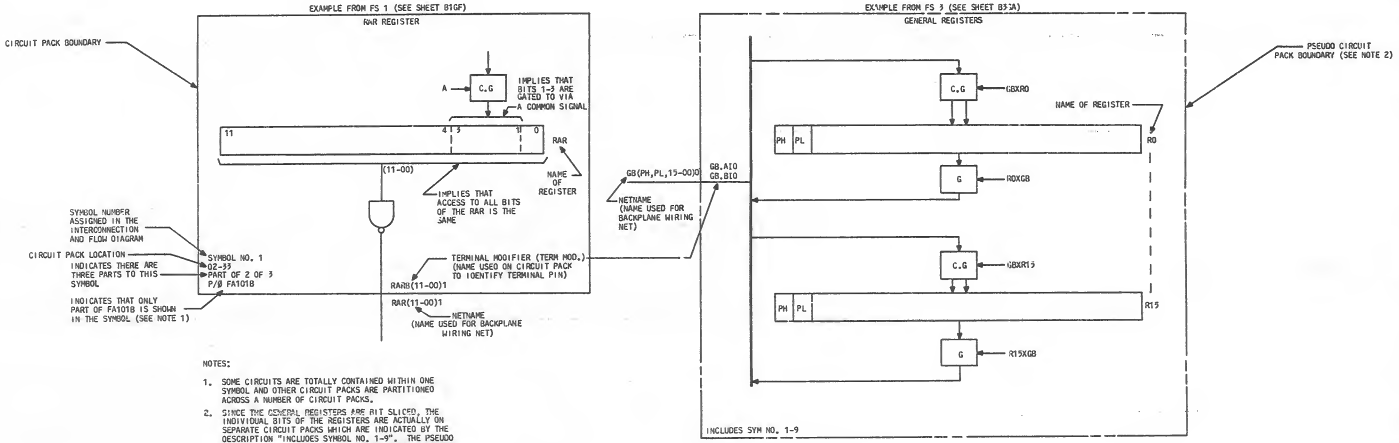
BELL LABORATORIES

SD-1C900-01

D4

INFORMATION NOTES: (CONT)

303. COMPOSITE DIAGRAM DRAWING CONVENTIONS


EXAMPLE FROM FS 1 (SEE SHEET B1GF)
RAR REGISTER
CIRCUIT PACK BOUNDARY
A
C.G
IMPLIES THAT BITS 1-3 ARE GATED TO VIA A COMMON SIGNAL
11
4
3
1
0
RAR
(11-00)
IMPLIES THAT ACCESS TO ALL BITS OF THE RAR IS THE SAME
NAME OF REGISTER
SYMBOL NUMBER ASSIGNED IN THE INTERCONNECTION AND FLOW DIAGRAM
CIRCUIT PACK LOCATION
INDICATES THERE ARE THREE PARTS TO THIS SYMBOL
INDICATES THAT ONLY PART OF FA101B IS SHOWN IN THE SYMBOL (SEE NOTE 1)
SYMBOL NO. 1
02-33
PART OF 2 OF 3
P/0 FA101B
TERMINAL MODIFIER (TERM MOD.) (NAME USED ON CIRCUIT PACK TO IDENTIFY TERMINAL PIN)
RARB(11-00)1
RAR(11-00)1
NETNAME (NAME USED FOR BACKPLANE WIRING NET)
GB(PH,PL,15-00)0
GB.AIO
GB.BIO
NETNAME (NAME USED FOR BACKPLANE WIRING NET)
EXAMPLE FROM FS 3 (SEE SHEET B33A)
GENERAL REGISTERS
C.G
GBXR0
NAME OF REGISTER
PH
PL
R0
G
R0XGB
C.G
GBXR15
PH
PL
R15
G
R15XGB
INCLUDES SYM NO. 1-9
PSEUDO CIRCUIT PACK BOUNDARY (SEE NOTE 2)

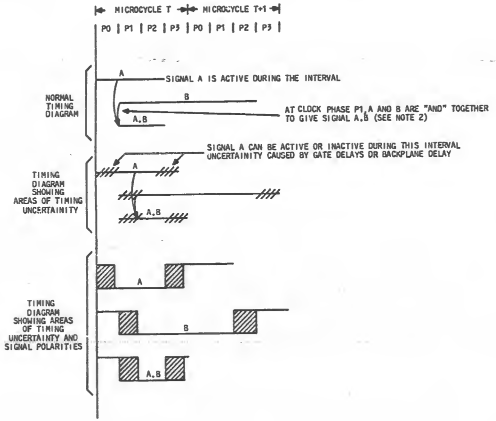
NOTES:

1. SOME CIRCUITS ARE TOTALLY CONTAINED WITHIN ONE SYMBOL AND OTHER CIRCUIT PACKS ARE PARTITIONED ACROSS A NUMBER OF CIRCUIT PACKS.
2. SINCE THE GENERAL REGISTERS ARE BIT SLICED, THE INDIVIDUAL BITS OF THE REGISTERS ARE ACTUALLY ON SEPARATE CIRCUIT PACKS WHICH ARE INDICATED BY THE DESCRIPTION "INCLUDES SYMBOL NO. 1-9". THE PSEUDO CIRCUIT BOUNDARY THEREFORE REPRESENTS THE BOUNDARY BETWEEN THE CIRCUIT PACKS AND THE BACKPLANE ON A FUNCTIONAL BASIS INSTEAD OF AN INDIVIDUAL CIRCUIT PACK BASIS.

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	D5

INFORMATION NOTES: (CONT)

304. COMPOSITE DIAGRAM TIMING CONVENTIONS


MICROCYCLE T
MICROCYCLE T+1
P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3
NORMAL TIMING DIAGRAM
A
SIGNAL A IS ACTIVE DURING THE INTERVAL
B
AT CLOCK PHASE P1, A AND B ARE "AND" TOGETHER TO GIVE SIGNAL A.B (SEE NOTE 2)
A.B
TIMING DIAGRAM SHOWING AREAS OF TIMING UNCERTAINITY
SIGNAL A CAN BE ACTIVE OR INACTIVE DURING THIS INTERVAL UNCERTAINITY CAUSED BY GATE DELAYS OR BACKPLANE DELAY
A
A.B
TIMING DIAGRAM SHOWING AREAS OF TIMING UNCERTAINTY AND SIGNAL POLARITIES
A
B
A.B

NOTES:

1. NO ATTEMPT HAS BEEN MADE IN THE DIAGRAMS TO SHOW EXACT TIME RELATIONSHIP BECAUSE THE GATE DELAYS USED IN THE LOGIC FUNCTIONS AS WELL AS THE INTRINSIC DELAY OF THE BACKPLANE VARY CONSIDERABLY AND REPRESENT A SIGNIFICANT FACTOR IN THE CONTROL SIGNAL SET UP TIME. IF THIS INFORMATION IS REQUIRED REFER TO CIRCUIT PACK DRAWINGS TO OBTAIN THE NUMBER OF GATES IN LOGIC CHAIN. ALSO GATE DELAY SPECIFICATIONS AND BACKPLANE WIRING MUST BE TAKEN INTO ACCOUNT.
2. IN MOST CASES THE ACTIVATION OF CONTROL SIGNALS OR A CHANGE OF STATE OF A FLIP FLOP IS INITIATED BY A CLOCK PHASE. WHEN A CHANGE OF STATE STARTS AT THE BEGINNING OF A CLOCK PHASE IT CAN BE ASSUMED THAT THE CLOCK INITIATES THE FUNCTION.

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 3A
BELL LABORATORIES	SD-1C900-01	D6

INFORMATION NOTES: (CONT)

305. LOGIC SIGNAL LEVELS

NOTE (1) THE SIGNAL LEVELS ON MOST BACKPLANE NETS IN THE 3ACC ARE:

(1) A HIGH LEVEL SIGNAL ≈ 900-1500 m VOLTS
(2) A LOW LEVEL SIGNAL ≈ 100-200 m VOLTS

THERE ARE ONLY THREE EXCEPTIONS TO THE PRECEDING:

(1) THE OUTPUT OF THE CLOCK PHASES (P01, P11, P21, P31, IO.P01, IO.P11, IO.P21, AND IO.P31) DRIVEN BY A 1A HIGH POWERED GATE (SEE SHEET B8GB)
(2) THE OUTPUT OF THE I/O SERIAL CHANNEL THAT IS DRIVEN BY A 1A HIGH POWERED GATE
(3) THE OUTPUT OF THE MAR REGISTER SIGNALS (MAR (00-08)1-FANOUT PHASES A,B,C AND D) THAT FANOUT TO THE MICROSTORE. THE MICROSTORE PROVIDES A PULL UP RESISTOR TO 3V SO THAT THE 1A LOGIC FROM THE MAR CAN INTERFACE TO THE T²L LOGIC USED IN THE MICROSTORE INTERFACE LOGIC (SEE SHEET B12GB).

306. GENERAL COMMENTS ON MNEMONIC DEFINITIONS

THE MNEMONIC DEFINITIONS THAT ARE OF MAJOR CONCERN FROM THE STANDPOINT OF THE SD ARE THE TERMINAL MODIFIERS AND THE NET NAMES. THE TERMINAL MODIFIERS REFER TO THE NAME ASSIGNED TO A TERMINAL PIN ON A CIRCUIT PACK. TERMINAL PINS ON INDIVIDUAL CIRCUIT PACKS ARE INTERCONNECTED ON A BACKPLANE BY ONE OR MORE WIRE SEGMENTS IN A CONTINUOUS SEQUENCE. THIS SEQUENCE OF WIRES IS REFERRED TO AS A "NET". THE CONVENTION FOR NET NAMES AND TERMINAL MODIFIERS IN THIS SD IS THE SAME.

THE MNEMONICS ARE COMPOSED OF 8 OR LESS ALPHA-NUMERIC CHARACTERS, THE LAST CHARACTER IS TYPICALLY AN 0 OR 1. THE 0 OR 1 REPRESENTS THE POLARITY OF THE SIGNAL WHEN ACTIVE. FOR CONTROL SIGNALS THE MEANING IS OBVIOUS; FOR DATA LEADS, IT REPRESENTS THE STATE OF THE DATA BIT FROM WHICH THE SIGNAL ORIGINATED. IF THE LAST CHARACTER IS ALPHABETIC (ONLY A,B,C OR D IS USED) THEN THE SECOND LAST CHARACTER (0 OR 1) REPRESENTS THE POLARITY OF THE SIGNAL WHEN ACTIVE. THE ALPHABETIC CHARACTER REPRESENTS THE FANOUT PHASE OF THE LOGIC SIGNAL. THAT IS, IF THE LAST CHARACTER IS ALPHABETIC THEN THERE IS MORE THAN ONE SIGNAL WITH THE SAME LOGICAL SIGNAL.

SOME ADDITIONAL COMMENTS OF THE NET NAME MNEMONICS:

MOST OF THE BACKPLANE NETS IN THE 3A CC HAVE A "LOW ACTIVE" POLARITY. THERE ARE TWO REASONS FOR THIS.

(1) SINCE MOST NETS IN THE BACKPLANE DRIVE BUFFER INVERTERS (TYPE OF 1A GATE), IN GENERAL MORE NOISE MARGIN IS PROVIDED FOR THE CONTROL SIGNALS WHOSE INACTIVE STATE IS HIGH.

(2) THE ABILITY TO COLLECTOR-TIE CONTROL OR DATA LEADS IS PROVIDED BY THE LOW ACTIVE CONVENTION IN THE BACKPLANE. THIS IS USED EXTENSIVELY FOR NETS SUCH AS THE GATING BUS (GB000-GB190).

MOST OF THE CONTROL AND DATA SIGNALS ASSOCIATED WITH THE MAINTENANCE CHANNEL ARE PREFIXED BY MC.

MOST CONTROL LEADS OTHER THAN THE ONES ALREADY DEFINED ARE PREFIXED WITH E OR EN TO INDICATE THAT THEY ARE ENABLE LEADS.

ALL DIRECT SETS TO THE ERROR REGISTER AND, HENCE, OUTPUTS OF CHECK CIRCUITS ARE PREFIXED WITH ER. FOR EXAMPLE, ER.GBPTO IS THE OUTPUT OF THE GATING BUS PARITY CHECKER AND WHEN THIS LEAD IS LOW, THE CORRESPONDING BIT IN THE ER (BIT 3) GETS SET.

ALL DIRECT SETS TO THE INTERRUPT SET REGISTER ARE PREFIXED WITH IS. FOR EXAMPLE, ISPANLO IS THE INPUT TO THE INTERRUPT BIT IN THE IS (BIT 13) THAT INDICATES A CC PANEL FUNCTION IS BEING REQUESTED.

307. MNEMONIC CONVENTIONS

TO-FIELD AND FROM-FIELD CONTROL SIGNALS

ON A TYPICAL MICROCYCLE THE MICROPROGRAM CONTROL GATES FROM A SOURCE REGISTER TO A DESTINATION USING TWO 4-OUT-OF-8 ENCODED FIELDS READ OUT OF THE MICROSTORE. THESE FIELDS ARE NAMED THE TO-FIELD AND THE FROM-FIELDS. DECODING IS PERFORMED BY SPLITTING THE 8-BIT FIELDS INTO TWO 4-BIT HALVES, NAMED THE LEFT HALF AND THE RIGHT HALF. THE BIT COMBINATIONS FOR EACH OF THE 70 VALID 4-OUT-OF-8 CODES PARTITIONED IN 4-BIT HALVES CAN BE ENUMERATED AS FOLLOWS:

(1) 4 ONES ON LEFT, 0 ONES ON THE RIGHT (1 COMBINATION).
(2) 3 ONES ON LEFT, 1 ONE ON THE RIGHT (16 COMBINATIONS).
(3) 2 ONES ON LEFT, 2 ONES ON THE RIGHT (36 COMBINATIONS).
(4) 1 ONE ON LEFT, 3 ONES ON THE RIGHT (16 COMBINATIONS).
(5) 0 ONES ON LEFT, 4 ONES ON THE RIGHT (1 COMBINATION).

307. (CONT)

AS SHOWN ON SHEET B1G7, THE DECODING IS ONLY PARTIALLY PERFORMED ON THE TO-FIELD AND FROM-FIELD CIRCUIT PACKS. THE DECODED CONTROL SIGNALS SEEN ON THE BACKPLANE REPRESENT THE PARTIAL DECODING OF THE LEFT AND RIGHT HALF, RESPECTIVELY. THE FINAL STAGE OF DECODING IS PERFORMED ON THE BOARD ON WHICH THE FUNCTION IS TO BE USED (THERE ARE A FEW EXCEPTIONS). THE MNEMONIC DEFINITIONS OF THE TO-FIELD AND FROM-FIELD CONTROL SIGNALS WHICH ARE ON THE BACKPLANE ARE NAMED TO REFLECT THE 4-OUT-OF-8 CODE THAT PRODUCED THEM.

FOR EXAMPLE, THE 4-OUT-OF-8 CODE 1100 0101 WOULD HAVE THE CONTROL LEADS F204ICO AND F204R50 ACTIVE IF IT WAS A FROM-FIELD CODE. FOR A TO-FIELD CODE IT WOULD BE T204LCO AND T204R5C. THE MNEMONIC FIELD FOR THE TO AND THE FROM CONTROL LEADS CAN BE BROKEN DOWN INTO SIX DIFFERENT FIELDS AS FOLLOWS:

F 204 L C 0 B

FIELD 1 - F → FROM-FIELD.
T → TO-FIELD.

FIELD 2 - 204 → 2 ONES IN THE 4-BIT SUBFIELD.
104 → 1 ONE IN THE 4-BIT SUBFIELD.
304 → 3 ONES IN THE 4-BIT SUBFIELD.
404 → 4 ONES IN THE 4-BIT SUBFIELD.

FIELD 3 - L → LEFT HALF 4-BIT SUBFIELD.
R → RIGHT HALF 4-BIT SUBFIELD.

FIELD 4 - C → HEXIDECIMAL REPRESENTATION OF THE CONTENTS OF THE 4-BIT SUBFIELD THAT CAUSES THE CONTROL SIGNAL TO BE ACTIVE.

FIELD 5 - 0 → CONTROL SIGNAL IS LOW WHEN ACTIVE.
1 → CONTROL SIGNAL IS HIGH WHEN ACTIVE.

FIELD 6 - BLANK - ONLY ONE FANOUT PHASE.
A → FIRST FANOUT PHASE OF A MULTIPLE FANOUT SIGNAL.
B → SECOND FANOUT PHASE OF A MULTIPLE FANOUT SIGNAL.
C → THIRD FANOUT PHASE OF A MULTIPLE FANOUT SIGNAL.

FIELDS 5 AND 6 ARE THE SAME FOR ALL BACKPLANE NETS (EXCEPT P AND N LEADS, SEE I/O SUBCHANNEL SIGNALS MNEMONICS) IN THE 3A CC.

MISCELLANEOUS DECODER SIGNALS

MISCELLANEOUS DECODER SIGNALS THAT ENTER THE BACKPLANE ARE NORMALLY PREFIXED BY THE LETTERS MD. THE REMAINING CHARACTER POSITIONS OF THE MNEMONIC ATTEMPT TO DESCRIBE ITS FUNCTIONAL PURPOSE AND WHERE POSSIBLE AGREES WITH THE SYMBOL USED BY THE MICROPROGRAM LISTINGS. FOR EXAMPLE:

MD . Z PT 0

FIELD 1 - MD → INDICATES A MISCELLANEOUS DECODER CROSSPOINT.

FIELD 2 - . → A DELIMITER TO IMPROVE MNEMONIC CLARITY.

FIELD 3 - Z → ZERO OR CLEAR FUNCTION.

FIELD 4 - PT → INDICATES THAT THE PROGRAM TIMER IS TO BE ZEROED.

FIELD 5 - 0 → INDICATES THAT A LOW SIGNAL ON THIS LEAD WILL ZERO OR CLEAR THE PROGRAM TIMER.

MAIN STORE BUS SIGNALS

THOSE SIGNALS THAT INTERFACE TO THE MAIN STORE USE THE FOLLOWING CONVENTION:

A. SA 0 11 I 0

FIELD 1 - SA → DEFINES THESE LEADS AS BEING STORE ADDRESS LEADS.

FIELD 2 - 0 → DEFINES WHICH MAIN STORE BUS IS DEFINED.
0 → "MY STORE BUS".
1 → "OTHER STORE BUS".

FIELD 3 - 11 → DEFINES THIS LEAD AS BEING BIT 11 OF THE STORE ADDRESS BUS.

FIELD 4 - I → DEFINES WHETHER THIS LEAD IS AN INPUT TO OR AN OUTPUT FROM THE STORE BUS REPEATER IN THE 3A CC. WHEN THE STORE ADDRESS BUS SIGNALS LEAVE A 3A CC THEY ARE DIRECTED TOWARDS THE MAIN STORE. THEREFORE, THESE NETS HAVE AN O (FOR OUTPUT) IN THIS FIELD OF THIS MNEMONIC. THE INPUT TO THE STORE BUS REPEATER FROM THE OTHER 3A CC WILL HAVE AN I.

FIELD 5 - 0 → INDICATES THAT A ONE IS IN BIT 11 OF THE STORE ADDRESS IF THIS LEAD IS LOW.

307. (CONT)

B. WHEN THE MAIN STORE BUS LEADS CROSSCOUPLE BETWEEN THE 3A CCS SO THAT ONE 3A CC CAN ACCESS THE OTHER 3A CC'S MEMORY BUS, THESE SIGNALS MUST BE FUSED. (SEE SHEET B13GA). THESE MAIN STORE BUS LEADS BEFORE ENTERING THE FUSE ARE DESIGNATED AS FOLLOWS:

SA 0 11 I X 0 (SEE SHEET 0B)

C. THE STORE DATA LEADS USE A 2-WAY BUS AND, THEREFORE, THE DEFINITION OF AN INPUT TO OR AN INPUT FROM THE BUS REPEATER HAS TO BE DEFINED. THE STORE DATA LEADS USE THE SAME CONVENTION AS THE STORE ADDRESS LEADS. THEREFORE, SD 0 13 O 0 DEFINES BIT 13 OF THE STORE DATA BUS ASSOCIATED WITH "MY STORE" AND IT IS AN OUTPUT FROM THE 3A CC BUS REPEATER TO ITS ASSOCIATED STORE.

D. THE OTHER SIGNALS (CONTROL, HANDSHAKING, AND ERROR LEADS) IN THE 3A CC MAIN STORE BUS BEGIN WITH AN "S". THE SECOND CHARACTER POSITION USES A "0" OR A "1" TO INDICATE "MY STORE BUS" OR "OTHER STORE BUS" RESPECTIVELY. THE NEXT CHARACTER FIELD DEFINES THE FUNCTION OF THAT LEAD WHICH IS DESCRIBED IN EACH INDIVIDUAL MNEMONIC DESCRIPTION. THE NEXT CHARACTER FIELD INDICATES AN INPUT (I) OR AN OUTPUT (O) TO THE BUS REPEATER. ON THOSE SIGNALS SUCH AS THE STORE GO SIGNAL THAT ARE DIRECTED FROM THE 3A CC TO THE STORE, AN O IS USED (i.e. S 0 GO O 0, SAME AS THE ADDRESS AND THE DATA LEADS). FOR THOSE SIGNALS SUCH AS THE STORE COMPLETE SIGNAL THAT ARE DIRECTED FROM THE STORE TO THE 3A CC AN "I" IS USED (i.e. S 0 CM I 0).

I/O SUBCHANNEL SIGNALS

ALL I/O SUBCHANNEL PORTS ARE PREFIXED WITH SC. THEY ALSO USE A DIFFERENT CONVENTION FOR DEFINING THE SIGNAL POLARITY WHEN ACTIVE. THAT IS:

SC 00 R 14 N

FIELD 1 - SC* → INDICATES A SUBCHANNEL PORT.

FIELD 2 - 00 → DEFINES THIS SUBCHANNEL PORT AS BEING CONTAINED IN I/O MAIN CHANNEL 00. I/O CHANNELS ARE NUMBERED 00-02.†

FIELD 3 - R → DEFINES WHETHER THE SUBCHANNEL PORT IS A SEND OR A RECEIVE PORT.
R → RECEIVE.
S → SEND.

FIELD 4 - 14 → DEFINES THIS PORT TO BE SUBCHANNEL 14. SUBCHANNELS ARE NUMBERED 00-19.

FIELD 5 - N → THE I/O SUBCHANNELS SEND INFORMATION OUT ON A TRANSMISSION LINE CABLE (COAX). THE SIGNAL USES A BIPOLAR PULSE TO TRANSMIT THE DATA. THE N LEAD IS CONNECTED TO THE SHIELD OF THE COAX LINE (NORMALLY GROUNDED AT ONE END) AND THE P LEAD IS CONNECTED TO THE SIGNAL LEAD.

REGISTER OUTPUTS

WHERE REGISTER OUTPUTS APPEAR ON THE BACKPLANE THE NAME OF THE REGISTER IS GIVEN EXPLICITLY. THE POLARITY OF THE SIGNAL LEAD IN THE CASE OF A REGISTER OUTPUT IS DEFINED AS THE POLARITY OF THE SIGNAL (HIGH OR LOW) WHEN A ONE IS IN THE NAMED BIT OF THE REGISTER. FOR EXAMPLE:

BR 0 07 0

FIELD 1 - BR → DEFINES THE REGISTER AS THE BR REGISTER IN THE DML.

FIELD 2 - 0 → INDICATES THAT THIS IS THE BR0 REGISTER CONTAINED IN DML COPY 0.

FIELD 3 - 07 → DEFINES THIS BIT AS BIT 7 OF THE BR0 REGISTER.

FIELD 4 - 0 → DEFINES THIS NET TO BE LOW WHEN THERE IS A ONE IN BIT 7 OF THE BR0 REGISTER.

3-VOLT POWER SYSTEM

THE 3A CC USES THE STANDARD 1A 3-VOLT POWER SYSTEM. A 3-VOLT POWER LEAD AND A GROUND RETURN ARE NORMALLY ROUTED TO EACH INDIVIDUAL CIRCUIT PACK VIA A BACKPLANE MULTILAYER SYSTEM. THE FOLLOWING IS A PARTIAL LIST OF THE TYPES OF NETS ASSOCIATED WITH THAT SYSTEM IN THE 3A CC:

A. 3VG 02 03 T

FIELD 1 - 3VG → THIS PREFIX IS USED FOR ALL GROUND NETS THAT ARE WIRED "INDIRECTLY" TO THE MULTILAYER GROUND PLANE VIA NORMAL 30 # WIRING. PINS 200 AND 319 ARE STANDARD GROUND PINS ON EACH CIRCUIT PACK AND THEY ARE ALWAYS CONNECTED DIRECTLY TO THE MULTILAYER GROUND. IF ADDITIONAL PINS ON THE PACK ARE TO BE GROUNDED, THEY ARE WIRED WITH 30 # WIRE TO EITHER PINS 200 OR 319 ON THAT PACK.

307. (CONT)

FIELD 2 - 02 → INDICATES THE CIRCUIT PACK LEVEL IN WHICH THIS PACK IS LOCATED IN THE 3A CC.

FIELD 3 - 03 → INDICATES THE CIRCUIT PACK POSITION IN THE DESIGNATED LEVEL.

FIELD 4 - T → INDICATES THE PIN TO BE GROUNDED IS IN THE TOP HALF OF THE CIRCUIT PACK CONNECTOR AND, HENCE, CONNECTED TO THE STANDARD GROUND PIN 319.
B → INDICATES THE PIN TO BE GROUNDED IS IN THE BOTTOM HALF OF THE CIRCUIT PACK CONNECTOR AND, HENCE, CONNECTED TO THE STANDARD GROUND PIN 200.

B. 3T 054 0

FIELD 1 - 3T → THIS PREFIX IS USED FOR CIRCUIT PACK PINS THAT ARE CONNECTED DIRECTLY TO THE MULTILAYER GROUND PLANE. THEREFORE, THE STANDARD GROUND PINS ON ALL PACKS ARE CONNECTED THIS WAY. IN ADDITION, A FEW PINS ARE GROUNDED DIRECTLY TO THE MULTILAYER GROUND VIA THIS METHOD. THE REASON ALL GROUND PINS ARE NOT CONNECTED THIS WAY IS TO PROVIDE A LESS PAINFUL WAY TO CHANGE GROUND PIN ASSIGNMENTS EARLY IN THE DESIGN PROCESS.

FIELD 2 - 054 → INDICATED THE "RELATIVE" LEVEL POSITION WITHIN THE 3A CC OF THIS POWER NET. 054 IS LEVEL 2 IN THE 3A CC.

FIELD 3 - D → SEQUENCES A, B, C, AND D INDICATE WHICH 3-VOLT CONVERTER MODULE ON A GIVEN LEVEL IS ATTACHED TO THIS GROUND NET.

C. 3V 062 B

FIELD 1 - 3V → THIS PREFIX IS USED FOR ALL CIRCUIT PACKS THAT ARE CONNECTED DIRECTLY TO THE MULTILAYER 3-VOLT POWER NET. THE STANDARD POWER PINS ON EACH PACK (000 AND 119) ARE ATTACHED IN THIS MANNER. THE MICROSTORE PACKS (ED'S) AND THE POWER REGULATOR PACKS (FC21) ATTACH ADDITIONAL PINS TO THIS MULTILAYER NET.

FIELD 2 - 062 → INDICATES THE "RELATIVE" LEVEL POSITION WITHIN THE 3A CC OF THIS POWER NET. 062 IS LEVEL 10 IN THE 3A CC.

FIELD 3 - B → SEQUENCES A, B, C, AND D INDICATE WHICH 3-VOLT CONVERTER MODULE ON A GIVEN LEVEL IS ATTACHED TO THIS GROUND NET.

D. OGD 06 43 B

FIELD 1 - OGD → THIS PREFIX IS USED FOR ALL COAX TERMINATING FIELD (CTF) PINS THAT ARE CONNECTED TO THE MULTILAYER GROUND PLANE.

FIELD 2 - 06 — INDICATES THE LEVEL POSITION OF THIS GROUND NET WITHIN THE 3A CC.

FIELD 3 - 43 → INDICATES THE CIRCUIT PACK POSITION OF THIS GROUND NET IN THE DESIGNATED LEVEL.

FIELD 4 - B → INDICATES THE BOTTOM ROW OF CTF GROUND PINS IN THIS DESIGNATED LEVEL.
T → INDICATES THE TOP ROW OF CTF GROUND PINS IN THIS DESIGNATED LEVEL.

NOTES:

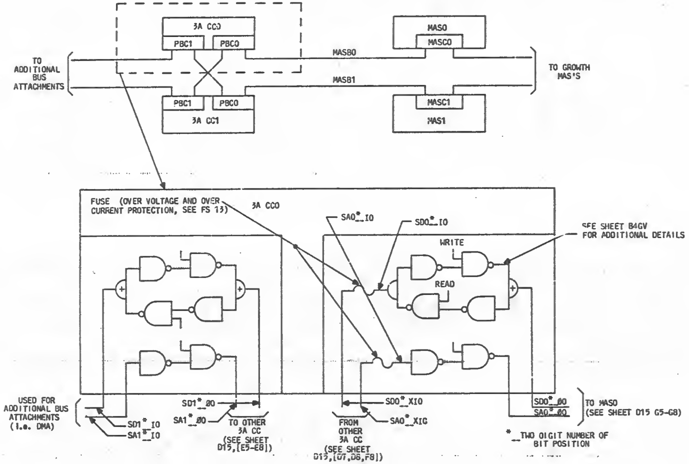
*THAT SC PREFIX IS NOT EXCLUSIVELY RESERVED FOR I/O SUBCHANNELS. THAT IS, OTHER NET NAMES ALSO START WITH SC.

†ONLY THREE I/O MAIN CHANNELS ARE CONTAINED IN THE STANDARD 3A CC.

3A CENTRAL CONTROL ②		DWG SIZE 65	ISSUE 3A
BELL LABORATORIES	SD-1C900-01		D7

INFORMATION NOTES: (CONT)

307(CONT). 3A CC MAIN STORE BUS MNEMONICS


3A CC0
PBC1
PBC0
MAS0
MASC0
MASB0
MASB1
TO ADDITIONAL BUS ATTACHMENTS
TO GROWTH MAS'S
PBC1
PBC0
3A CC1
MASC1
MAS1
FUSE (OVER VOLTAGE AND OVER CURRENT PROTECTION, SEE FS 13)
3A CC0
SA0*__IO
SD0*__IO
SEE SHEET B4GV FOR ADDITIONAL DETAILS
WRITE
READ
USED FOR ADDITIONAL BUS ATTACHMENTS (i.e. DMA)
SD1*__IO
SA1*__IO
SD1*__00
SA1*__00
TO OTHER 3A CC (SEE SHEET D15,[E5-E8])
SD0*__XIO
SA0*__XIO
FROM OTHER 3A CC (SEE SHEET D15,[D7,D8,F8])
SD0*__00
SA0*__00
TO MAS0 (SEE SHEET D15 G5-G8)
*__TWO DIGIT NUMBER OF BIT POSITION

3A CENTRAL CONTROL ②

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

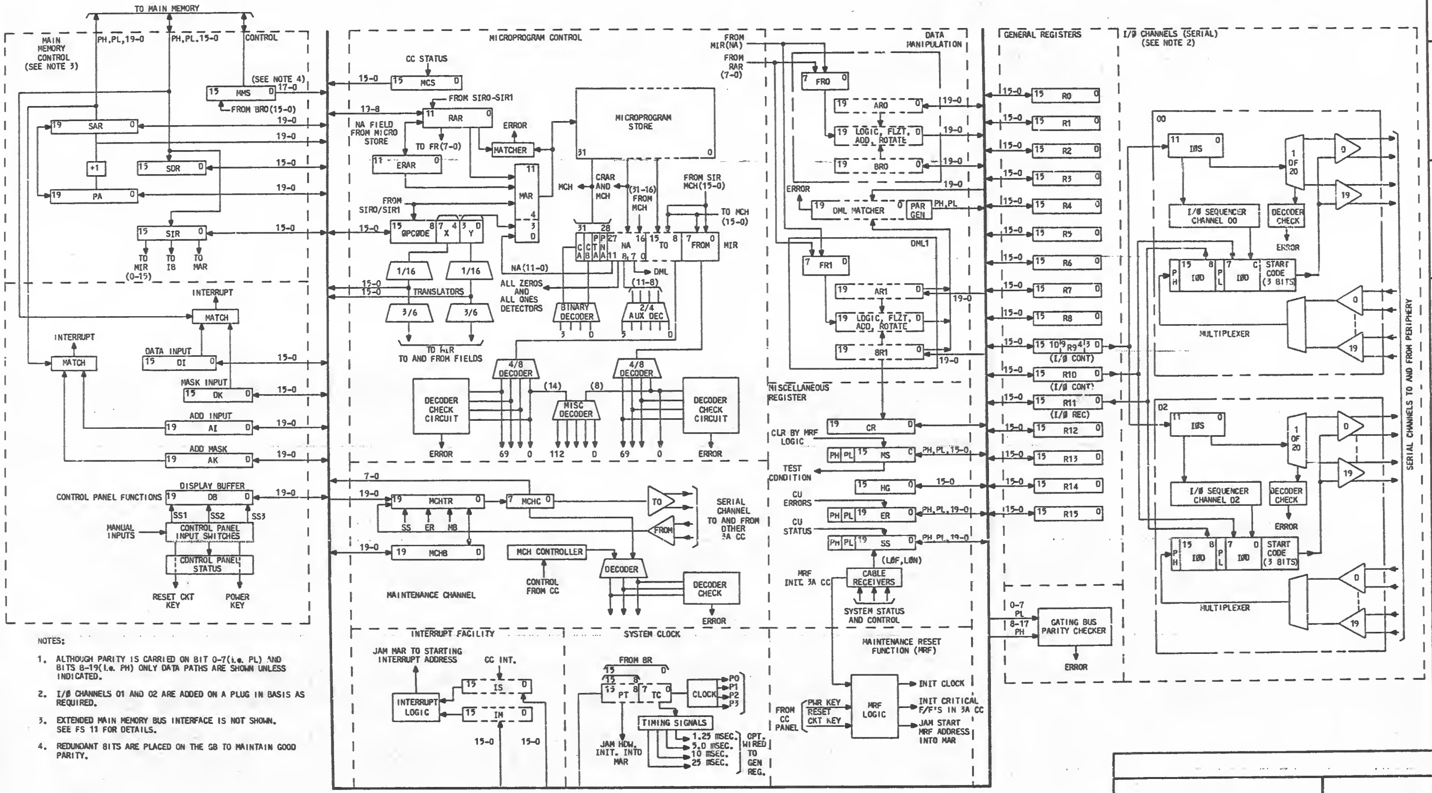
SD-1C900-01

D8

INFORMATION NOTES: (CONT)

308. BASIC GATING PATHS IN 3A CC

3A CENTRAL CONTROL



NOTES:

1. ALTHOUGH PARITY IS CARRIED ON BIT 0-7(i.e. PL) AND BITS 8-19(i.e. PH) ONLY DATA PATHS ARE SHOWN UNLESS INDICATED.
2. I/O CHANNELS 01 AND 02 ARE ADDED ON A PLUG IN BASIS AS REQUIRED.
3. EXTENDED MAIN MEMORY BUS INTERFACE IS NOT SHOWN. SEE FS 11 FOR DETAILS.
4. REDUNDANT BITS ARE PLACED ON THE GB TO MAINTAIN GOOD PARITY.

3A CENTRAL CONTROL

DWG SIZE
6S

ISSUE
3A

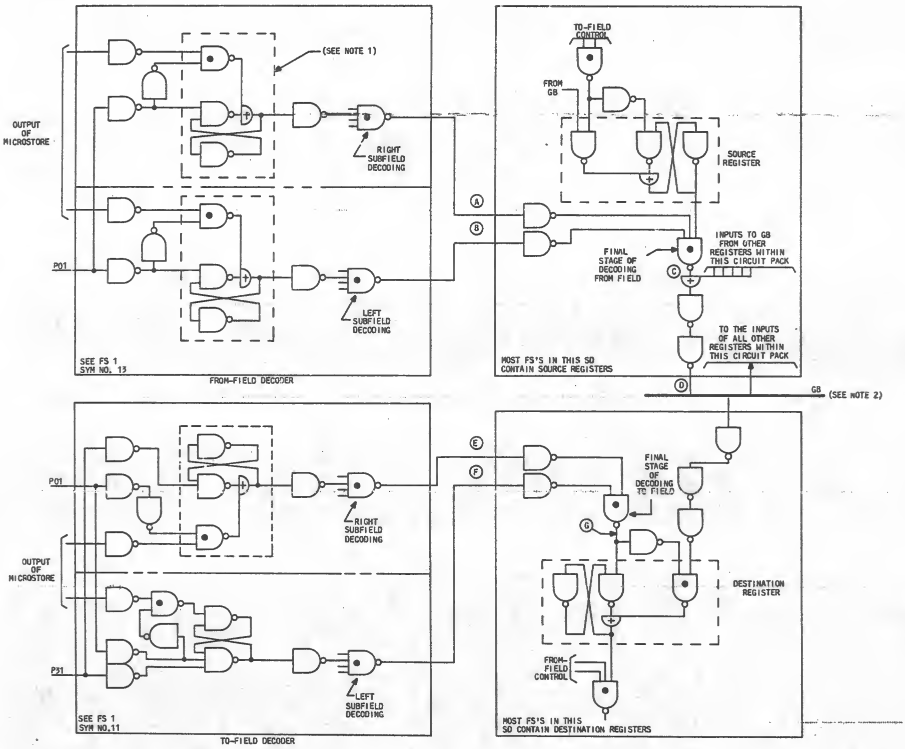
BELL LABORATORIES

SD-1C900-01

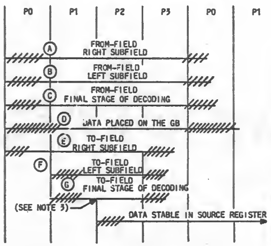
D9

INFORMATION NOTES: (CONT)

309. TYPICAL 3A CC REGISTER TO REGISTER GATING



REGISTER TO REGISTER TIMING


P0
P1
P2
P3
P0
P1
P2
Ⓐ FROM-FIELD RIGHT SUBFIELD
Ⓑ FROM-FIELD LEFT SUBFIELD
Ⓒ FROM-FIELD FINAL STAGE OF DECODING
Ⓓ DATA PLACED ON THE GB
Ⓔ TO-FIELD RIGHT SUBFIELD
Ⓕ TO-FIELD LEFT SUBFIELD
Ⓖ TO-FIELD FINAL STAGE OF DECODING
(SEE NOTE 3)
DATA STABLE IN SOURCE REGISTER

NOTES:

1. THESE GATES ARE TYPICALLY CONTAINED WITHIN A 2-BIT REGISTER DEVICE (SEE B3GB)
2. THE GB IS THE COMMON POINT THROUGH WHICH ALMOST ALL REGISTERS TO REGISTER DATA TRANSFERS TAKE PLACE. IT REPRESENTS A POINT WHERE THE DATA IS "OR"ED FROM ALL SOURCES AND THEN FANOUTS TO ALL REGISTERS IN THE 3A CC.
3. THE INPUT TO THE SOURCE REGISTER FROM THE GB MUST BE STABLE BY THIS POINT IN TIME.

3A CENTRAL CONTROL ②

DWG SIZE 6S

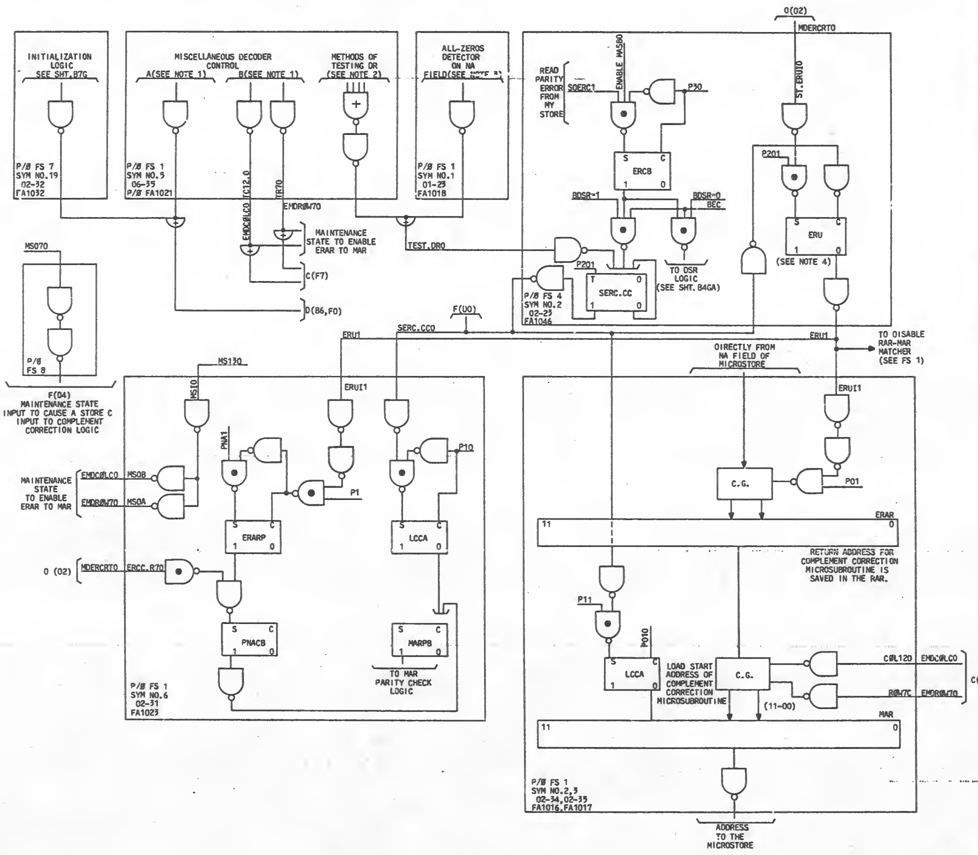
ISSUE 5A

BELL LABORATORIES SD-1C900-01 D10

INFORMATION NOTES: (CONT)

310.

COMPLEMENT CORRECTION LOGIC


INITIALIZATION LOGIC SEE SHT.B7G
P/Ø FS 7
SYM NO.19
02-32
FA1032
MISCELLANEOUS DECODER CONTROL
A(SEE NOTE 1)
B(SEE NOTE 1)
P/Ø FS 1
SYM NO.5
06-35
P/Ø FA1021
METHODS OF TESTING DR (SEE NOTE 2)
ALL-ZEROS DETECTOR ON NA FIELD(SEE NOTE 3)
P/Ø FS 1
SYM NO.1
01-23
FA1018
EMDCØLCO TC12.0
TR70
EMDRØW70
MAINTENANCE STATE TO ENABLE ERAR TO MAR
C(F7)
D(B6,F0)
TEST.DR0
MS070
P/Ø
FS 8
F(D4)
MAINTENANCE STATE INPUT TO CAUSE A STORE C INPUT TO COMPLEMENT CORRECTION LOGIC
READ PARITY ERROR FROM MY STORE
SOERC1
ENABLE MAS80
P30
ERCB
S
C
1
0
BDSR=1
BDSR=0
BEC
TO DSR LOGIC (SEE SHT. B4GA)
P201
SERC.CC
T
P/Ø FS 4
SYM NO.2
02-23
FA1046
0(02)
MDERCRTO
ST.ERUI0
P201
ERU
(SEE NOTE 4)
F(D0)
SERC.CC0
ERU1
ERU1
TO DISABLE RAR-MAR MATCHER (SEE FS 1)
MS130
MSI0
ERUI1
PWA1
P10
P1
MAINTENANCE STATE TO ENABLE ERAR TO MAR
EMDCØLCO
MS0B
EMDRØW70
MS0A
0 (02)
MDERCRTO
ERCC.R70
ERARP
LCCA
PNACB
MARPB
TO MAR PARITY CHECK LOGIC
P/Ø FS 1
SYM NO.6
02-31
FA1023
DIRECTLY FROM NA FIELD OF MICROSTORE
ERUI1
C.G.
P01
ERAR
11
0
RETURN ADDRESS FOR COMPLEMENT CORRECTION MICROSUBROUTINE IS SAVED IN THE RAR.
P11
P010
LCCA
LOAD START ADDRESS OF COMPLEMENT CORRECTION MICROSUBROUTINE
C.G.
CØL120
EMDCØLCO
RØW7C
EMDRØW70
C(D2)
(11-00)
MAR
11
0
P/Ø FS 1
SYM NO.2,3
02-34,02-35
FA1016,FA1017
ADDRESS TO THE MICROSTORE

CIRCUIT OPERATION

THE COMPLEMENT CORRECTION LOGIC IS USED TO CORRECT AUTOMATICALLY MAIN STORE (MAS) WORDS THAT HAVE BEEN ACCESSED WITH A READ PARITY ERROR INDICATION WHEN THE CU IS IN THE SIMPLEX MODE (i.e. NOT IN THE UPDATE MODE WHERE MAS0 AND MAS1 DO NOT HAVE IDENTICAL COPIES OF DATA). THE COMPLEMENT CORRECTION LOGIC IS SHOWN IN THE D SECTION OF THIS SD BECAUSE THE HARDWARE TO IMPLEMENT IT IS DISTRIBUTED ACROSS A NUMBER OF FS'S. IN ADDITION TO THE COMPLEMENT CORRECTION LOGIC, THERE IS THE DOUBLE STORE READ (DSR) LOGIC. IT IS USED TO CORRECT AUTOMATICALLY MAS WORDS THAT HAVE BEEN ACCESSED WITH A READ PARITY ERROR INDICATION WHEN THE CU COMPLEX IS IN THE DUPLEX MODE (i.e. ON UPDATE AND BOTH MAS0 AND MAS1 HAVE IDENTICAL COPIES OF DATA). FOR A GENERAL DESCRIPTION OF MAS CORRECTION TECHNIQUES AND A DETAILED DESCRIPTION OF THE DSR TECHNIQUE SEE SHEET B4GM FOR A DETAILED DESCRIPTION OF THE COMPLEMENT CORRECTION TECHNIQUE SEE SHEET D12. NOTE THAT THE LOGIC SHOWN ON THIS SHEET (D11) IS USED ONLY TO PERFORM THE COMPLEMENT CORRECTION FUNCTION WHEN IN THE SIMPLEX MODE. COMPLEMENT CORRECTION CAN ALSO BE PERFORMED BY A MACRO-LEVEL INSTRUCTION WITHOUT THE USE OF THIS HARDWARE WHEN THE SYSTEM IS IN THE DUPLEX MODE.

THE COMPLEMENT CORRECTION HARDWARE SHOWN, PERFORMS ITS FUNCTION BY INTERRUPTING THE MICROPROGRAM EXECUTION FLOW AT THE POINT WHERE IT IS TESTING FOR A MEMORY COMPLETION (TESTING THE DR FLIP-FLOP). IF A READ PARITY ERROR INDICATION IS RECEIVED (i.e. STORE ERROR C), THE MICROPROGRAM CONTROL WILL SAVE THE PRESENT MICROPROGRAM ADDRESS IN THE ERROR RETURN ADDRESS REGISTER (ERAR) AND BRANCH TO A MICROSUBROUTINE. THIS WILL PERFORM THE COMPLEMENT CORRECTION FUNCTION ON THE PRESENT MAS LOCATION DEFINED BY THE STORE ADDRESS REGISTER (SAR). AT THE TERMINATION OF THIS MICROSUBROUTINE, THE CONTENTS OF THE ERAR WILL BE GATED TO THE MICROPROGRAM STORE ADDRESS REGISTER (MAR) AND THE MICROPROGRAM EXECUTION FLOW WILL CONTINUE.

NOTES:

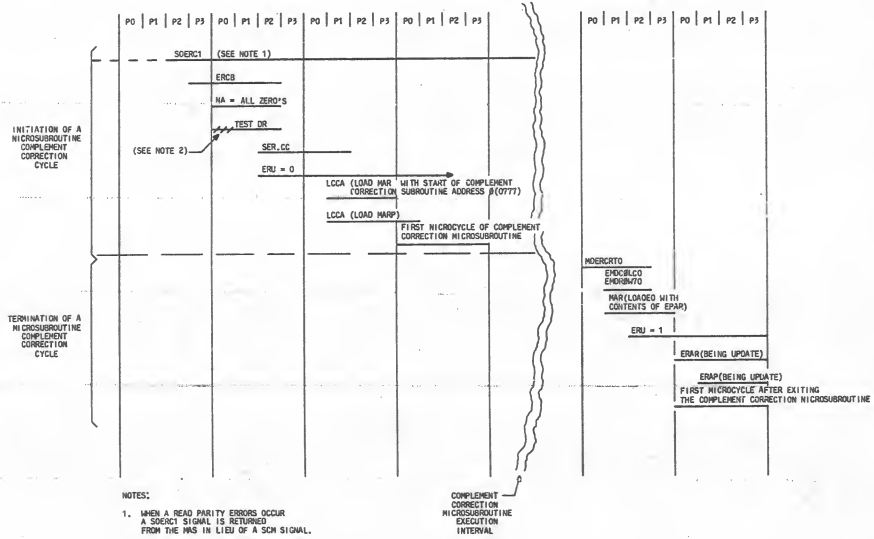
1. CONTROL AT A IS LOGICALLY EQUIVALENT TO THE CONTROL AT B. A REPRESENTS THE NORMAL DECODING OF THE MISCELLANEOUS DECODER CROSSPOINT INDICATING THE END OF A COMPLEMENT CORRECTION MICROSUBROUTINE. CONTROL B IS THE "FAST" MISCELLANEOUS DECODER CONTROL OF THE SAME FUNCTION (SEE FS 1 FOR A DESCRIPTION OF THE MISCELLANEOUS DECODER CONTROL).
2. A NUMBER OF METHODS ARE USED TO TEST THE DR FLIP-FLOP (i.e. SIRC, SDRC, SARI, SARD, AND TDR) TO DETERMINE IF A MAIN STORE CYCLE HAS BEEN COMPLETED.
3. THE ALL-ZEROS DETECTOR ON THE NA FIELD IS USED TO INDICATE AN INSTRUCTION SEQUENCE HAS ENDED AND HENCE THE COMPLETION OF THE NEXT INSTRUCTION FETCH BY THE MAIN STORE CAN BE TESTED.
4. WHEN CLEARED THE ERU (1) SAVES THE PRESENT CONTENTS OF THE ERAR AND ITS PARITY ERARP (2) DISABLES MAR-RAR MATCHER.

3A CENTRAL CONTROL ②	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	D11

INFORMATION NOTES: (CONT)

311.

TIMING DIAGRAM FOR THE COMPLEMENT
CORRECTION LOGIC OPERATIONS


P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3
SOERC1 (SEE NOTE 1)
ERCB
NA = ALL ZERO'S
TEST DR
(SEE NOTE 2)
SER.CC
ERU = 0
LCCA (LOAD MAR WITH START OF COMPLEMENT CORRECTION SUBROUTINE ADDRESS 0(0777)
LCCA (LOAD MARP)
FIRST MICROCYCLE OF COMPLEMENT CORRECTION MICROSUBROUTINE
INITIATION OF A MICROSUBROUTINE COMPLEMENT CORRECTION CYCLE
TERMINATION OF A MICROSUBROUTINE COMPLEMENT CORRECTION CYCLE
P0 | P1 | P2 | P3 | P0 | P1 | P2 | P3
MDERCRTO
EMDC0LCO
EMDR0W70
MAR(LOADED WITH CONTENTS OF ERAR)
ERU = 1
ERAR(BEING UPDATE)
ERAP(BEING UPDATE)
FIRST MICROCYCLE AFTER EXITING THE COMPLEMENT CORRECTION MICROSUBROUTINE
COMPLEMENT CORRECTION MICROSUBROUTINE EXECUTION INTERVAL

NOTES:

1. WHEN A READ PARITY ERRORS OCCUR A SOERC1 SIGNAL IS RETURNED FROM THE MAS IN LIEU OF A SCM SIGNAL.
2. TEST DR DOES NOT START UNTIL P1 FOR SOME METHODS OF TESTING DR.

CIRCUIT OPERATION

THE COMPLEMENT CORRECTION TECHNIQUE IS BASED ON THE ASSUMPTION THAT A SINGLE BIT IN A MEMORY LOCATION HAS FAILED. THIS FAILURE RESULTS IN THIS BIT BEING STUCK IN THE COMPLEMENT OF ITS CORRECT STATE. THEREFORE, IF ALL THE OTHER BITS OF THAT WORD ARE INVERTED, THEN THAT WORD CAN BE CORRECTED AND STORED IN THAT LOCATION IN ITS CORRECT BUT COMPLEMENTED STATE. THE CIRCUITRY SHOWN ON SHEET 011 IS USED TO INVOKE A MICROSUBROUTINE THAT PERFORMS THIS COMPLEMENT CORRECTION FUNCTION AUTOMATICALLY WHEN A READ PARITY ERROR OCCURS. WHEN A MEMORY LOCATION HAS BEEN COMPLEMENT CORRECTED BOTH PARITY BITS PL AND PH (i.e. WHICH IS THE SAME AS P1 AND P2 FOR 2B APPLICATION) IN THE MAS ARE MARKED BAD. THIS DOUBLE PARITY ERROR IS THEN USED AS A SIGNAL TO THE MASC TO COMPLEMENT A MEMORY LOCATION BEFORE PLACING IT ON THE MAIN STORE BUS (MASB). IN THIS MANNER, THE COMPLEMENT CORRECTION SUBROUTINE IS ONLY USED WHEN A BAD LOCATION IS FIRST DETECTED WHEN IN THE SIMPLEX MODE. NOTE THAT SINCE THE CU'S ARE NORMALLY RUN IN DUPLEX, THE AUTOMATIC MICRO-LEVEL CORRECTION IS NOT THE MOST FREQUENT METHOD OF INVOKING COMPLEMENT CORRECTION. THAT IS, A MACRO-LEVEL INSTRUCTION IS USED WITHIN A MEMORY AUDIT ROUTINE TO COMPLEMENT CORRECT LOCATIONS THAT HAVE INCURRED A SINGLE-BIT ERROR WHEN THE SYSTEM IS IN DUPLEX MODE.

THE INITIATION OF THE AUTOMATIC COMPLEMENT CORRECTION FUNCTION IS PERFORMED WHEN THE STORE ERROR C SIGNAL INDICATES A READ PARITY ERROR. THE STORE ERROR C SIGNAL IS STROBED INTO THE ERCB FLIP-FLOP AND THIS OPERATION SYNCHRONIZES THIS MAS SIGNAL WITH THE 3A CC CLOCK. THE DETERMINATION BY SYSTEM SOFTWARE OF WHETHER THE CU IS IN SIMPLEX OR DUPLEX, RESULTS IN THE BLOCK DOUBLE STORE READ (BDSR) BIT BEING SET OR CLEARED. IF THE BDSR BIT IS SET, COMPLEMENT CORRECTION IS INVOKED. THE OUTPUT OF THE ERCB FLIP-FLOP IS THEN GATED INTO THE SERC.CC FLIP-FLOP AT THE TIME THE MICROPROGRAM CONTROL INDICATES IT IS TESTING THE DR. HENCE, IT IS WAITING FOR THE WORD THAT HAS BEEN ACCESSED FROM THE MAS. IN THIS INSTANCE THE WORD IS IN ERROR AND MUST BE CORRECTED. THE SETTING OF THE SERC.CC FLIP-FLOP RESULTS IN CLEARING THE ERU FLIP-FLOP AND THE LOADING OF THE STARTING ADDRESS OF THE COMPLEMENT CORRECTION MICROSUBROUTINE VIA THE LCCA (LOAD COMPLEMENT CORRECTION ADDRESS) FLIP-FLOP. THE LCCA CONTROL MUST ALSO CLEAR THE MAR PARITY BIT SINCE THE STARTING MICROPROGRAM ADDRESS IS ODD [0(0777)]. THE PURPOSE OF CLEARING THE ERU IS TO SAVE THE PRESENT MICROPROGRAM ADDRESS IN THE ERAR. NOTE THAT THE ERAR AND THE ERU OPERATE IN THE SAME MANNER AS THE RAR AND THE RU AS DESCRIBED IN FS 1. THAT IS, THE NEXT ADDRESS FIELD FROM THE MICROPROGRAM STORE IS GATED TO THE ERAR AND THE PNA PARITY BIT IS GATED TO THE ERAR BIT ON EVERY MICROCYCLE AS LONG AS THE ERU (ERROR RETURN ADDRESS UPDATE BIT) IS SET. WHEN THE ERU IS CLEARED THE PRESENT CONTENTS OF THE ERAR AND THE ERARP ARE PRESERVED. THE CLEARING OF THE ERU ALSO RESULTS IN THE DISABLING OF THE RAR-MAR MATCHER.

AT LOCATION 0(0777) THE MICROPROGRAM STARTS A SPECIAL MICROSUBROUTINE THAT PERFORMS THE COMPLEMENT CORRECTION FUNCTION. IN ORDER TO PERFORM THIS FUNCTION, THE PRESENT STATE OF THE MAIN MEMORY STATUS (MMS) REGISTER MUST BE SAVED IN A SPARE REGISTER AND THE MMS MUST BE RELOADED WITH A SPECIAL STATE TO ISSUE THE COMPLEMENT WRITE REQUEST. A COMPLEMENT WRITE RESULTS IN A SPECIAL MASB SIGNAL (SCW) BEING ACTIVATED, FOLLOWED BY A WRITE REQUEST. THIS WRITE WILL CAUSE THE MAIN STORE CONTROLLER (MASC) TO COMPLEMENT THE BAD WORD READ OUT OF THE MAS AND TO WRITE THE COMPLEMENTED WORD INTO THE LOCATION FROM WHICH IT WAS READ. IN THIS PROCESS, THE TWO PARITY BITS THAT ARE STORED WITH THIS COMPLEMENTED WORD ARE NOW IN ERROR. IN ADDITION, NEITHER THE ORIGINAL BAD PARITY WORD OR THE COMPLEMENTED BAD PARITY WORD RESIDE IN THE 3A CC. THE RESULT IS THAT THE LOCATION THAT WAS IN ERROR HAS BEEN COMPLEMENT CORRECTED, THE 3A CC IS RESTORED TO ITS ORIGINAL STATE AND NO INTERNAL ERRORS IN THE 3A CC HAVE RESULTED FROM THE BAD MAS LOCATION. THE ONLY ERROR IN THE 3A CC ER REGISTER WILL BE THE MAS READ PARITY ERROR (BIT 10).

WHEN THE COMPLEMENT CORRECTION MICROSUBROUTINE HAS COMPLEMENTED THE WORD IT WILL REREAD THE SAME LOCATION. ON THIS REREAD THE MASC WILL COMPLEMENT THE DATA IT IS BEING READ OUT AND IT WILL CORRECT THE PARITY BITS ACCORDINGLY. NOTE THAT THE INDICATION FOR THE MASC TO AUTOMATICALLY COMPLEMENT A MEMORY LOCATION IS GIVEN BY THE MASB SIGNAL SAC (STORE AUTOMATIC CORRECTION). THE SAC SIGNAL TOGETHER WITH THE TWO BAD PARITY BITS RESULT IN THE CORRECTION OF A MEMORY LOCATION THAT HAS EARLIER BEEN COMPLEMENTED. NOTE THAT THIS LOCATION WILL NO LONGER INVOKE THE COMPLEMENT CORRECTION MICROSUBROUTINE IF ITS DATA DOES NOT CHANGE. IN OTHER WORDS, THE READ PARITY ERROR INDICATION (STORE ERROR C) IS NOT GIVEN FOR THOSE LOCATIONS THAT HAVE DOUBLE PARITY ERRORS AND WHERE THE SAC SIGNAL IS ACTIVE.

THE LAST MICROINSTRUCTION IN THE COMPLEMENT CORRECTION MICROSUBROUTINE WILL THEN ISSUE A MISCELLANEOUS DECODER FUNCTION THAT WILL GATE THE ERAR TO THE MAR AND THE ERARP TO THE MARB SO THAT THE ORIGINAL MICROPROGRAM FLOW WILL CONTINUE. IN ADDITION, THE ERU FLIP-FLOP WILL BE SET SO THAT THE ERAR REGISTER WILL CONTAIN CONTINUOUSLY UPDATED LOCATION OF THE MICROPROGRAM ADDRESS IN THE EVENT OF ANOTHER READ PARITY ERROR. NOTE THAT THE MISCELLANEOUS DECODER FUNCTION IS DUPLICATED AS DESCRIBED IN FS 1. THIS IS DONE IN ORDER TO ACHIEVE THE SPEED AS WELL AS TO PROVIDE THE SELF-CHECKING ASPECT WHEN PERFORMING THE ERROR RETURN FUNCTION FROM THE COMPLEMENT CORRECTION MICROSUBROUTINE

3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES | SD-1C900-01 | D12

INFORMATION NOTES: (CONT)

312.

3A CC
FROM – FIELD DECODING ASSIGNMENTS

104L & 304R

	F304R7	F304RB	F304RD	F304RE
F104L1	RAR(0-11) =>GB(8-19) [ZEROS IN GB(0-7)]	SPARE	SPARE SIR7	SIRD=>GB (18) (NOTE 1)
F104L2	MCHC(0-7) =>GB(0-7) (NOTE 3)	SPARE	SPARF SDR1	SDRD=>GB (18)
F104L4	R12=>GB (18)	R13=>GB (18)	R14=>GB (18)	R15=>GB (18)
F104L8	IM=>GB [MR12] (18) (NOTE 1,6)	IS(0-15) =>GB(0-15) [MR13]	MS=>GB [MR14] (18)	SS=>GB [MR15] (18)

204L & 204R

	F204R3	F204R5	F204R6	F204R9	F204RA	F204RC
F204L3	CR=>GB (22) (NOTE 2)	HG=>GB (18) (NOTE 1)	MISC DEC ROW 2	MISC DEC ROW 3	MISC DEC ROW 4	MISC DEC ROW 5
F204L5	RD=>GB (18)	R1=>GB (18)	R2=>GB (18)	R3=>GB (18)	R4=>GB (18)	R5=>GB (18)
F204L6	R6=>GB (18)	R7=>GB (18)	R8=>GB (18)	R9=>GB (18)	R10=>GB (18)	R11=>GB (18)
F204L9	TI(0-15) =>GB(0-15) [MR0] (NOTE 3,6)	SAR=>GB [MR1] (22)	PA=>GB [MR2] (22)	MCHB=>GB [MR3] (22)	MMS(0-11) =>GB(0-11, PL, PH) [MR4]	AK=>GB [MR5] (22)
F204LA	AI=>GB [MR6] (22)	DK=>GB [MR9] (18)	DI=>GB [MR8] (18)	DB=>GB [MR9] (22)	ER=>GB [MR10] (22) (NOTE 3)	SPARE [MR11]
F204LC	SIRC=>GB (18) (NOTE 5)	SDRC=>GB (18) (NOTE 5)	IB=>GB (18)	MISC DEC ROW 6	MISC DEC ROW 7	PA+1

304L & 104R

	F104R1	F104R2	F104R4	F104RB
F304L7	AR=>GB (22) (NOTE 2)	SPARE	MCS=>GB (22)	SPARE
F304L8	AR(0-15, PL) =>GB(0-15, PL) AR(PH) ⊕ AR(PH4) =>GB(PH)	SPARE	DML=>GB (22)	AR(16-19, PH4) =>GB(0-3, PL) [ZEROS IN GB(4-19) =>GB(PH) = 1]
F304LD	AR(0-19) =>GB(0-19) PL=>PL AR(PH) ⊕ AR(PH4) =>GB(PH)	IBYT=>GB (18) (NOTE 1)	IBXT=>GB (18)	MISC DEC ROW 0
F304LE	MIRH12=>GB MIR(NA) (0-11),PNA) =>GB(8-19, PH) [ZEROS IN G3(0-7) =>GB(PL) = 1]	BR=>GB (22)	MIRL8=>GB MIR(NA) (0-7, PNA) =>GB(0-7, PL) [ZEROS IN GB(8-19) =>GB(PH) = 1]	MISC DEC ROW 1

F404LO

NOP

(NO OPERATION OCCURS)
EXCEPT THAT BUS PARITY
CHECK IS DISABLED FOR
THIS MICROCYCLE

F404RD

SPARE

NOTES:

1. (18) IMPLIES AN 18 BIT GATING PATH (BITS 0-15, PL, PH).
2. (22) IMPLIES A 22 BIT GATING PATH (BITS 0-19, PL, PH).
3. REGISTER DOES NOT MAINTAIN PARITY => BUS PARITY CHECK SHOULD BE INHIBITED WHEN USING THIS GATING PATH.
4. THIS GATING IS CONDITIONAL ON THE DISPLAY BIT (BIT 17 OF THE SS).
5. THIS GATING IS CONDITIONAL ON THE DR FLIP FLOP = 1 (ie MAIN MEMORY CYCLE COMPLETE).
6. [MR0-15] REFER TO A SET OF MAINTENANCE REGISTERS AND ARE ACCESSED NORMALLY BY THE 3-OUT-OF-6 TRANSLATORS ATTACHED TO THE IB.
7. THE GB MUST BE IDLE ON THE MICROCYCLE PRECEDING THIS OPERATION.

3A CC
TO-FIELD DECODING ASSIGNMENTS

104L & 304R

	T304R7	T304RB	T304RD	T304RE
T104L1	GB(8-19, PH) => RAR(0-11, PH)	MISC DEC COL 13	MISC DEC COL 3	GB=>SIRD (18) (NOTE 1)
T104L2	MISC DEC COL 0	MISC DEC COL 1	MISC DEC COL 2	GB=>SDRD (18)
T104L4	GB=>R12 (18)	GB=>R13 (18)	GB=>R14 (18)	GB=>R15 (18)
T104L8	GB=>IM [MR12] (18) (NOTE 6)	GB=>SS_CL [MR13] (22) (NOTE 7)	GB=>MS [MR14] (18)	GB=>SS_ST [MR15] (22) (NOTE 7)

204L & 204R

	T204R3	T204R5	T204R6	T204R9	T204RA	T204RC
T204L3	GB=>CR (22) (NOTE 2)	GB=>HG (18) (NOTE 1)	GB=>IS_CL (18) (NOTE 7)	GB=>IS_S (18) (NOTE 7)	MISC DEC COL 8	MISC DEC COL 9
T204L5	GB=>RD (18)	GB=>R1 (18)	GB=>R2 (18)	GB=>R3 (18)	GB=>R4 (18)	GB=>R5 (18)
T204L6	GB=>R6 (18)	GB=>R7 (18)	GB=>R8 (18)	GB=>R9 (18)	GB=>R10 (18)	GB=>R11 (18)
T204L9	GB=>MCHTR [MR0] (22) (NOTE 6)	GB=>SAR [MR1] (22)	GB=>PA [MR2] (22)	GB=>MCHB [MR3] (22)	SPARE [MR4]	GB=>AK [MR5] (22)
T204LA	GB=>AI [MR6] (22)	GB=>DK [MR7] (18)	GB=>DI [MR8] (18)	GB=>DB [MR0] (22)	GB=>ER [MR10] (22)	GB=>DBC [MR11] (22) (NOTE 4)
T204LC	GB=>SARD (22) (NOTE 5)	GB=>SARI (22) (NOTE 5)	GB=>IB (18)	GB=>MISC DEC COL 12	MISC DEC COL 11	MISC DEC COL 10

304L & 104R

	T104R1	T104R2	T104R4	T104R8
T304L7	GB=>BR (22) (NOTE 2)	GB(0-7,PL) =>BR(0-7,PL) [ALL OTHER BITS OF BR ARE UNCHANGED]	GB(0-3) => BR(0-3) [ALL OTHER BITS OF BR ARE UNCHANGED]	MISC DEC COL 6
T304L8	GB=>AR (22)	GB=>ARD (22)	GB(0-15,PL,PH)=> AR(0-15,PL,PH) [AR(16-19) ARE UNCHANGED]	MISC DEC COL 5
T304LD	GB(0-3) =>AR(16-19) [NO PARITY BITS LOADED]	SPARE	GB(0,1) =>AR(0,1) [ALL OTHER BITS OF AR ARE UNCHANGED]	MISC DEC COL 4
T304LE	GB(0-7) =>MCHC(0-7) [NO PARITY IS LOADED]	GB=>SIB1 (18) (NOTE 1)	GB=>SDR1 (18)	MISC DEC COL 7

T404LD

NOP
(NO OPERATION OCCURS)

T404RD

GATE BR(15) TO
BR(16-19)

ISSUE 5A

3A CENTRAL CONTROL

SD-1C900-01-D13

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

INFORMATION NOTES: (CONT)

313.

3A CC
MISCELLANEOUS DECODER ASSIGNMENTS

		COL 0 T1O4L2 T3O4R7	COL 1 T1O4L2 T3O4RB	COL 2 T1O4L2 T3O4RD	COL 3 T1O4L1 T3O4RD	COL 4 T3O4LD T1O4RB	COL 5 T3O4LB T1O4R8	COL 6 T3O4L7 T1O4RB	COL 7 T3O4LE T1O4RB	COL 8 T2O4L3 T2O4RA	COL 9 T2O4L3 T2O4RC	COL 10 T2O4LC T2O4RC	COL 11 T2O4LC T2O4RA	COL 12 T2O4LC T2O4R9	COL 13 T1O4L1 T3O4RB
ROW 0	F3O4LD F1O4RB		PYMCN	NMRF	TMCN	IDLMCN	STMCN				SOPF	ZOPF	2I	TI	SI
ROW 1	F3O4LE F1O4RB		ZER	ZMINT	IOCC	ZMS	ZPT				TTR2	TDR	TY	TX	ZRU
ROW 2	F2O4L3 F2O4R6		IOD=>R11	S1DB	IMTC	BR=>TI	DML1=>CR	MD4 STCN	MD0 IDCD		TTR1	DS=>CF	TDS	TCF	TFL2
ROW 3	F2O4L3 F2O4R9		SBTC	S2DB	SDIS	INCTC	INCPR	MD5 EIOS	MD1 CNTN	ENB	SCF	SDS	STR1	STR2	SDR
ROW 4	F2O4L3 F2O4RA			MCNB=>MCNTR	S3DB	RAR=>FN	MCLSTR	MD6 RAIO	MD2 CNTM	ENA	2CF	2DS	2TR1	2TR2	ZDR
ROW 5	F2O4L3 F2O4RC	ABRG	ABR4	ABRB	ABR12			MD7 SPA	MD3 CHC		TBRO	TINT	TPAR	SIB=>SIR1	TCH
ROW 6	F2O4LC F2O4R9	BARO	BAR1	BAR2	BAR3	2DIDK	DK1=>SDR1 (NOTE 1)	DI1=>SDR1 (NOTE 1)	BR=>PT		OPF=>DS			TMARP	EXEC
ROW 7	F2O4LC F2O4RA	SBR	ZBR	IDSWQ	SSTP	STPASW	SBA	SD=>DK+DK1 SA=>AK (NOTE 2)	SD=>DI+DI1 (NOTE 2)	SRW	DFETCH	SSEIZ	BR=>MMS	ERAR=>MAR	SPBC

NOTES:

1. THIS GATING 'OR'S THE CONTENTS OF THE DK1 OR THE DI1 INTO SDR1 (I.E., THIS IS NOT A CLEAR AND GATE OPERATION).
2. THIS MISCELLANEOUS DECODER CROSSPOINT PERFORMS THE SAME FUNCTION AS THE ERROR SIGNAL C CIRCUITRY WHICH FIRES WHEN A READ PARITY ERROR OCCURS AND ODSR=0.

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-C!

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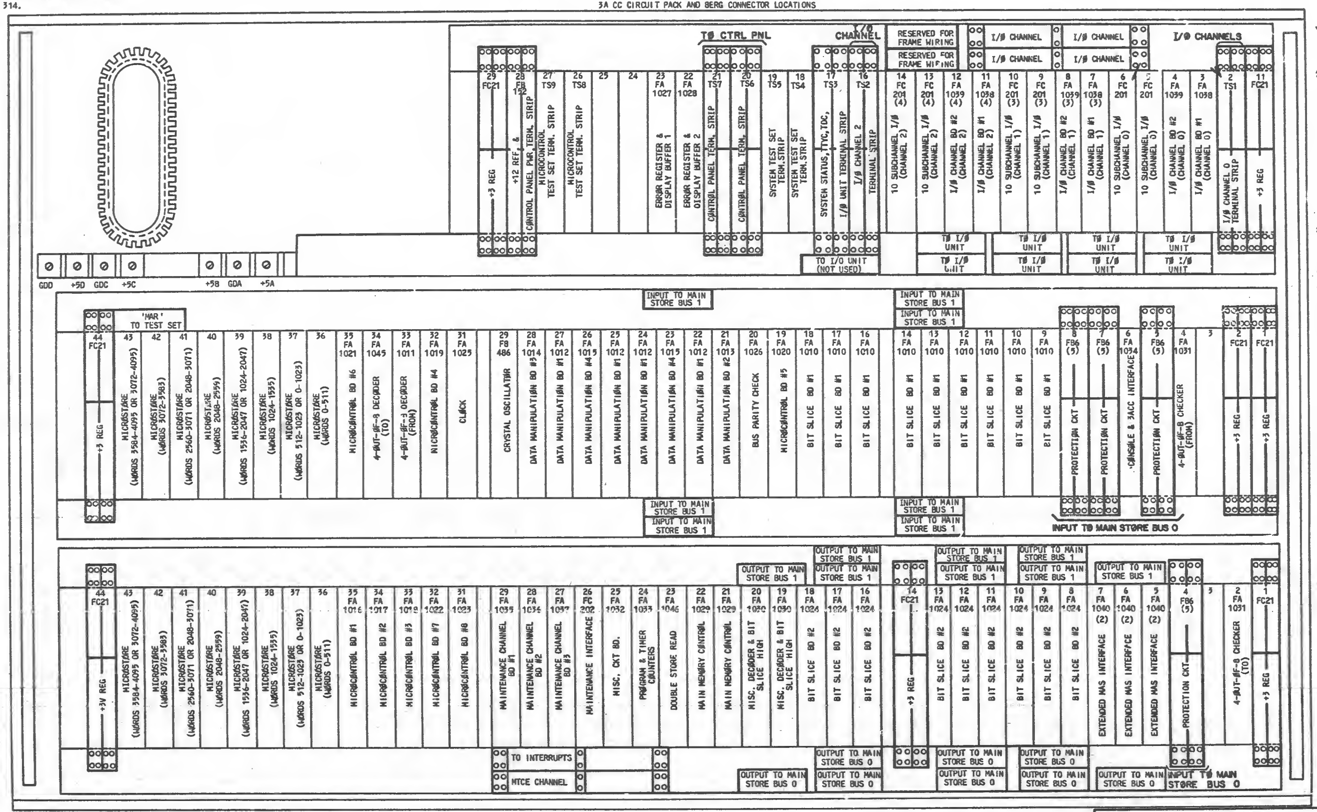
INFORMATION NOTES: (CONT)
314.

3A CC CIRCUIT PACK AND BERG CONNECTOR LOCATIONS



TO CTRL PNL
I/O CHANNEL
RESERVED FOR FRAME WIRING
I/O CHANNEL
I/O CHANNELS
29 FC21 +3 REG
28 FB 152 +12 REF. & CONTROL PANEL PWR. TERM. STRIP
27 TS9 MICROCONTROL TEST SET TERM. STRIP
26 TS8 MICROCONTROL TEST SET TERM. STRIP
25
24
23 FA 1027 ERROR REGISTER & DISPLAY BUFFER 1
22 FA 1028 ERROR REGISTER & DISPLAY BUFFER 2
21 TS7 CONTROL PANEL TERM. STRIP
20 TS6 CONTROL PANEL TERM. STRIP
19 TS5 SYSTEM TEST SET TERM. STRIP
18 TS4 SYSTEM TEST SET TERM. STRIP
17 TS3 SYSTEM STATUS, TTYC, TDC, I/O UNIT TERMINAL STRIP
16 TS2 I/O CHANNEL 2 TERMINAL STRIP
14 FC 201 (4) 10 SUBCHANNEL I/O (CHANNEL 2)
13 FC 201 (4) 10 SUBCHANNEL I/O (CHANNEL 2)
12 FA 1039 (4) I/O CHANNEL BD #2 (CHANNEL 2)
11 FA 1038 (4) I/O CHANNEL BD #1 (CHANNEL 2)
10 FC 201 (3) 10 SUBCHANNEL I/O (CHANNEL 1)
9 FC 201 (3) 10 SUBCHANNEL I/O (CHANNEL 1)
8 FA 1039 (3) I/O CHANNEL BD #2 (CHANNEL 1)
7 FA 1038 (3) I/O CHANNEL BD #1 (CHANNEL 1)
6 FC 201 10 SUBCHANNEL I/O (CHANNEL 0)
5 FC 201 10 SUBCHANNEL I/O (CHANNEL 0)
4 FA 1039 I/O CHANNEL BD #2 (CHANNEL 0)
3 FA 1038 I/O CHANNEL BD #1 (CHANNEL 0)
2 TS1 I/O CHANNEL 0 TERMINAL STRIP
1 FC21 +3 REG
TO I/O UNIT (NOT USED)
TO I/O UNIT
GDD +5D GDC +5C +5B GDA +5A
11
10
09
'MAR' TO TEST SET
INPUT TO MAIN STORE BUS 1
44 FC21 +3 REG
43 MICROSTORE (WORDS 3584-4095 OR 3072-4095)
42 MICROSTORE (WORDS 3072-3583)
41 MICROSTORE (WORDS 2560-3071 OR 2048-3071)
40 MICROSTORE (WORDS 2048-2559)
39 MICROSTORE (WORDS 1536-2047 OR 1024-2047)
38 MICROSTORE (WORDS 1024-1535)
37 MICROSTORE (WORDS 512-1023 OR 0-1023)
36 MICROSTORE (WORDS 0-511)
35 FA 1021 MICROCONTROL BD #6
34 FA 1045 4-OUT-OF-8 DECODER (TO)
33 FA 1011 4-OUT-OF-8 DECODER (FROM)
32 FA 1019 MICROCONTROL BD #4
31 FA 1025 CLOCK
29 FB 486 CRYSTAL OSCILLATOR
28 FA 1014 DATA MANIPULATION BD #3
27 FA 1012 DATA MANIPULATION BD #1
26 FA 1015 DATA MANIPULATION BD #4
25 FA 1012 DATA MANIPULATION BD #1
24 FA 1012 DATA MANIPULATION BD #1
23 FA 1015 DATA MANIPULATION BD #4
22 FA 1012 DATA MANIPULATION BD #1
21 FA 1013 DATA MANIPULATION BD #2
20 FA 1026 BUS PARITY CHECK
19 FA 1020 MICROCONTROL BD #5
18 FA 1010 BIT SLICE BD #1
17 FA 1010 BIT SLICE BD #1
16 FA 1010 BIT SLICE BD #1
14 FA 1010 BIT SLICE BD #1
13 FA 1010 BIT SLICE BD #1
12 FA 1010 BIT SLICE BD #1
11 FA 1010 BIT SLICE BD #1
10 FA 1010 BIT SLICE BD #1
9 FA 1010 BIT SLICE BD #1
8 FB6 (5) PROTECTION CKT
7 FB6 (5) PROTECTION CKT
6 FA 1034 CONSOLE & 3ACC INTERFACE
5 FB6 (5) PROTECTION CKT
4 FA 1031 4-OUT-OF-8 CHECKER (FROM)
3
2 FC21 +3 REG
1 FC21 +3 REG
INPUT TO MAIN STORE BUS 0
07
06
05
OUTPUT TO MAIN STORE BUS 1
44 FC21 +3V REG
43 MICROSTORE (WORDS 3584-4095 OR 3072-4095)
42 MICROSTORE (WORDS 3072-3583)
41 MICROSTORE (WORDS 2560-3071 OR 2048-3071)
40 MICROSTORE (WORDS 2048-2559)
39 MICROSTORE (WORDS 1536-2047 OR 1024-2047)
38 MICROSTORE (WORDS 1024-1535)
37 MICROSTORE (WORDS 512-1023 OR 0-1023)
36 MICROSTORE (WORDS 0-511)
35 FA 1016 MICROCONTROL BD #1
34 FA 1017 MICROCONTROL BD #2
33 FA 1018 MICROCONTROL BD #3
32 FA 1022 MICROCONTROL BD #7
31 FA 1023 MICROCONTROL BD #8
29 FA 1035 MAINTENANCE CHANNEL BD #1
28 FA 1036 MAINTENANCE CHANNEL BD #2
27 FA 1037 MAINTENANCE CHANNEL BD #3
26 FC 202 MAINTENANCE INTERFACE
25 FA 1032 MISC. CKT BD.
24 FA 1033 PROGRAM & TIMER COUNTERS
23 FA 1046 DOUBLE STORE READ
22 FA 1029 MAIN MEMORY CONTROL
21 FA 1029 MAIN MEMORY CONTROL
20 FA 1030 MISC. DECODER & BIT SLICE HIGH
19 FA 1030 MISC. DECODER & BIT SLICE HIGH
18 FA 1024 BIT SLICE BD #2
17 FA 1024 BIT SLICE BD #2
16 FA 1024 BIT SLICE BD #2
14 FC21 +3 REG
13 FA 1024 BIT SLICE BD #2
12 FA 1024 BIT SLICE BD #2
11 FA 1024 BIT SLICE BD #2
10 FA 1024 BIT SLICE BD #2
9 FA 1024 BIT SLICE BD #2
8 FA 1024 BIT SLICE BD #2
7 FA 1040 (2) EXTENDED MAS INTERFACE
6 FA 1040 (2) EXTENDED MAS INTERFACE
5 FA 1040 (2) EXTENDED MAS INTERFACE
4 FB6 (5) PROTECTION CKT
3
2 FA 1031 4-OUT-OF-8 CHECKER (TO)
1 FC21 +3 REG
TO INTERRUPTS
MTCE CHANNEL
OUTPUT TO MAIN STORE BUS 0
INPUT TO MAIN STORE BUS 0
03
02
01

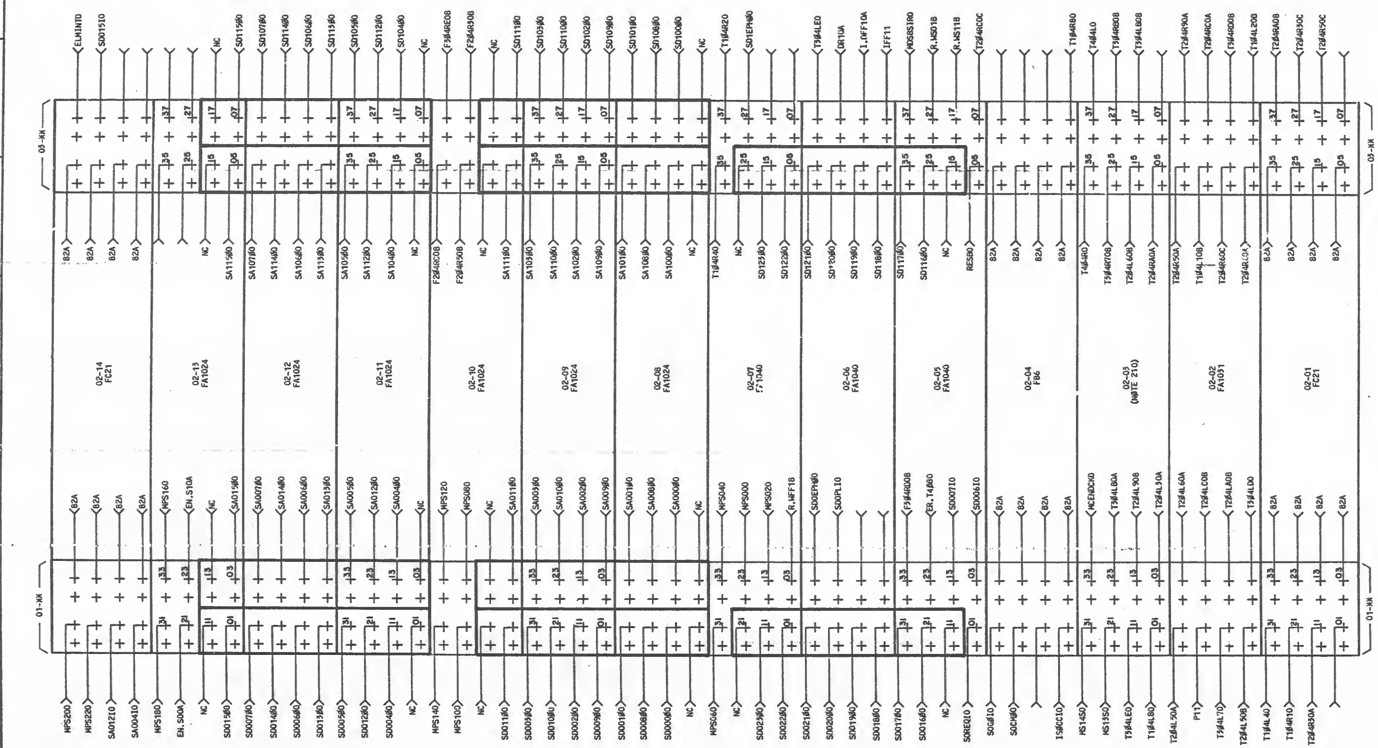
(REAR VIEW)

3A CENTRAL CONTROL
②
BELL LABORATORIES
SD-1C900-01
DWG SIZE 6S
ISSUE 6D
D15

I8080173

INFORMATION NOTES: (CONT)

314. (CONT)



(REAR VIEW)

3A CENTRAL CONTROL ②

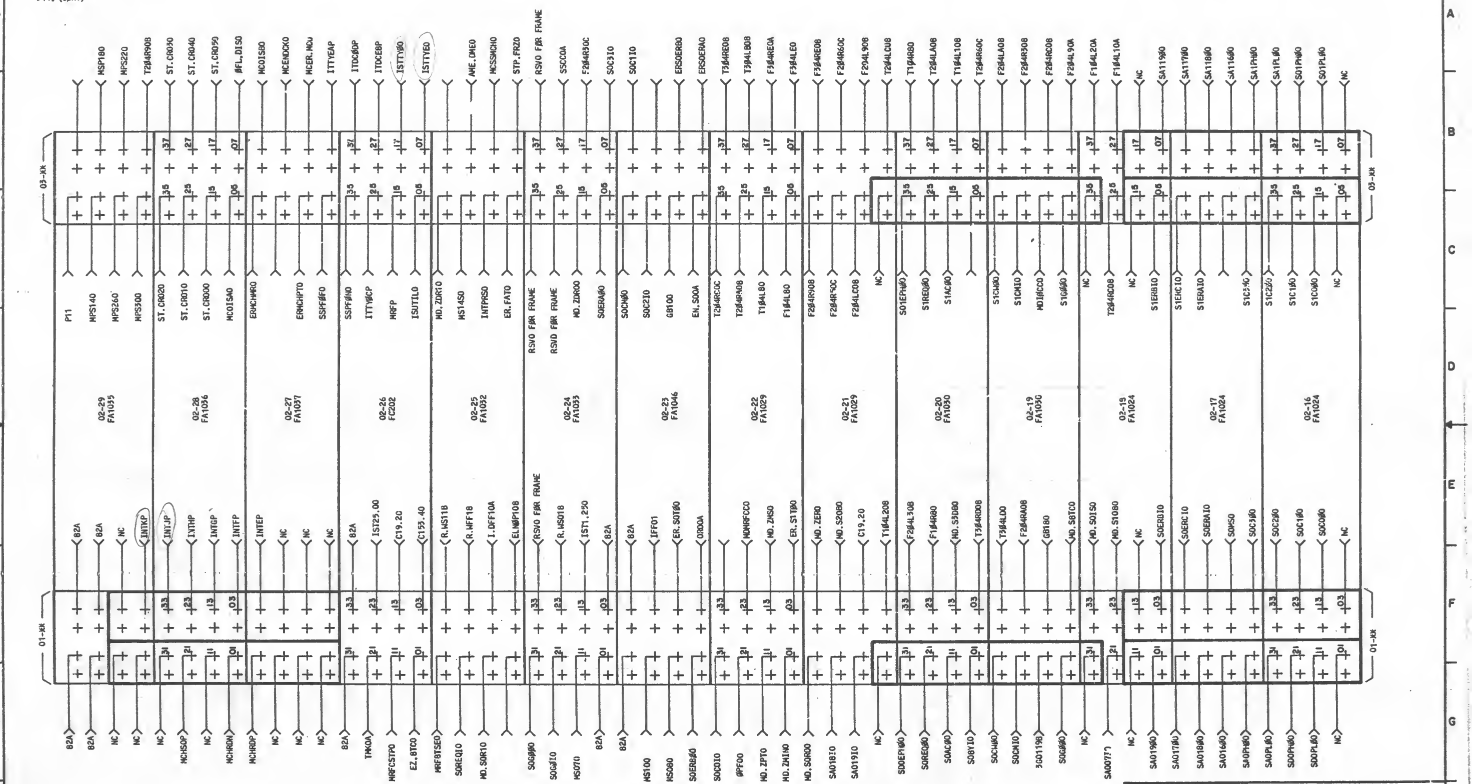
DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES SD-1C900-01 D16

8262-110173

INFORMATION NOTES: (CONT)

314. (CONT)

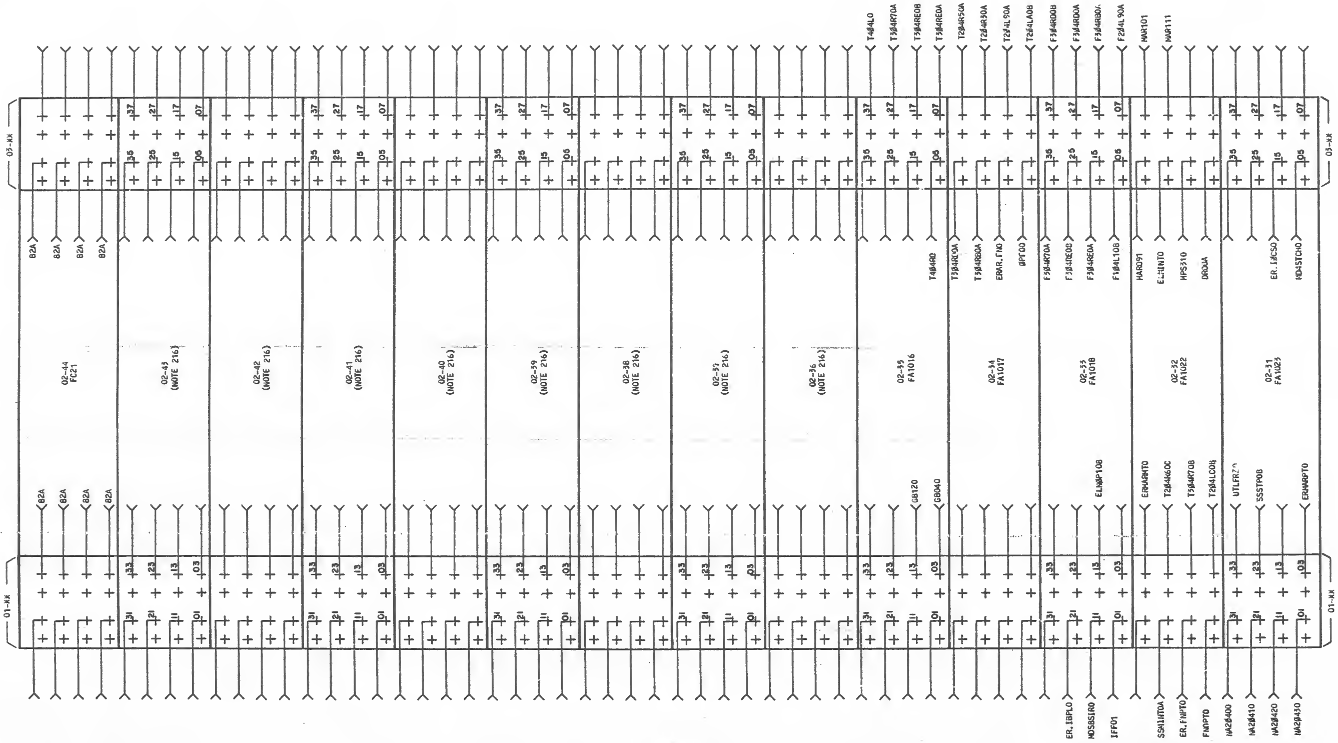


(REAR VIEW)

3A CENTRAL CONTROL	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	D17

8262-110173

INFORMATION NOTES: (CONT)
314. (CONT)



(REAR VIEW)

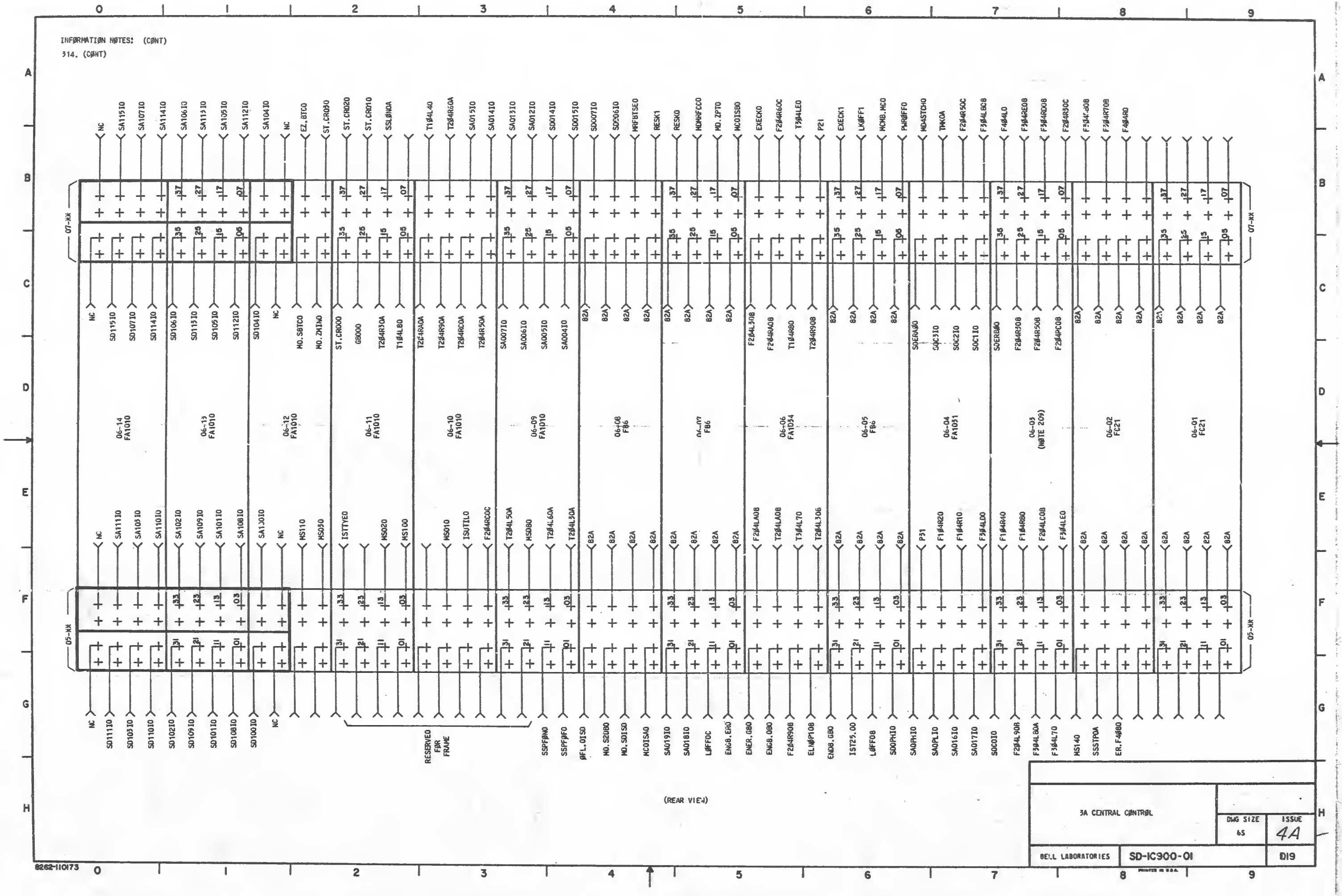
3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES SD-1C900-01 D18

8262-110173

INFORMATION NOTES: (CONT)
314. (CONT)



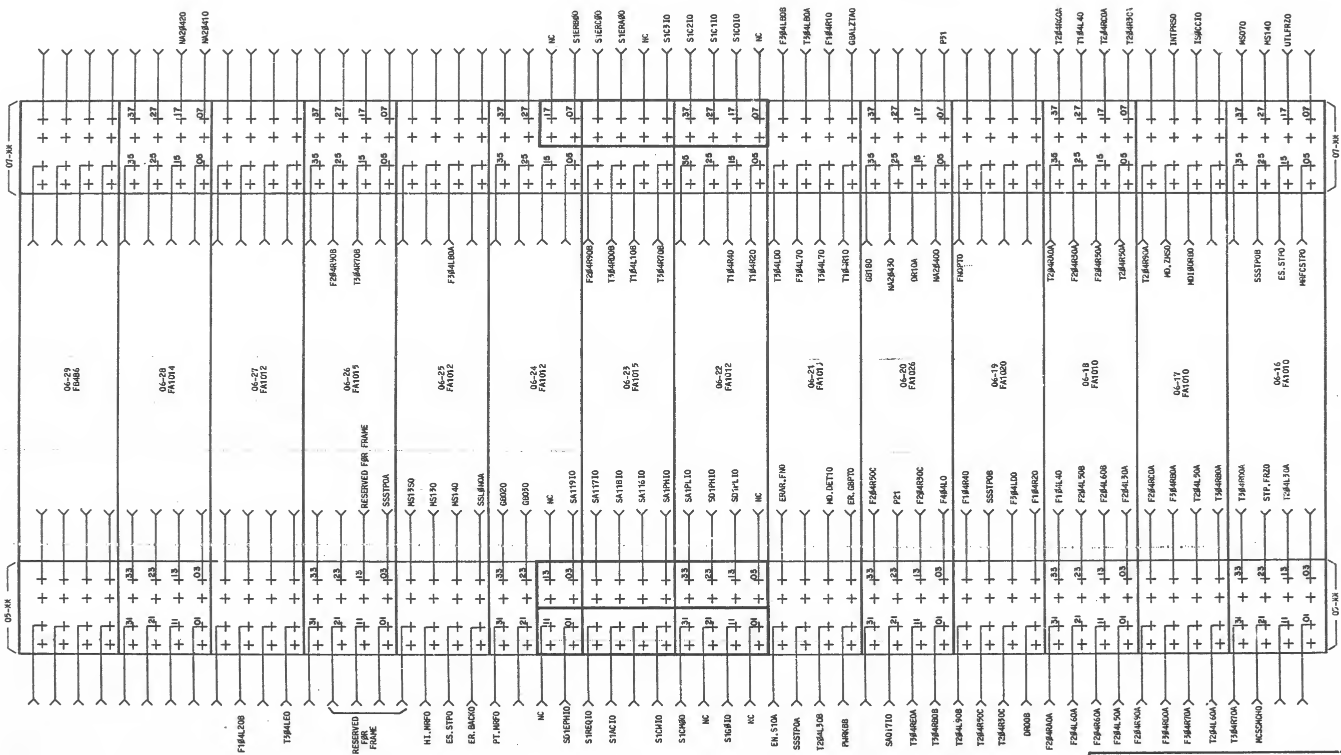
3A CENTRAL CONTROL

DWG SIZE	ISSUE
6S	4A

BELL LABORATORIES SD-1C900-01 019

8262-110173

INFORMATION NOTES: (CONT)
314. (CONT)



(REAR VIEW)

5A CENTRAL CONTROL
②

DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES SD-1C900-01 D20

8262-110173

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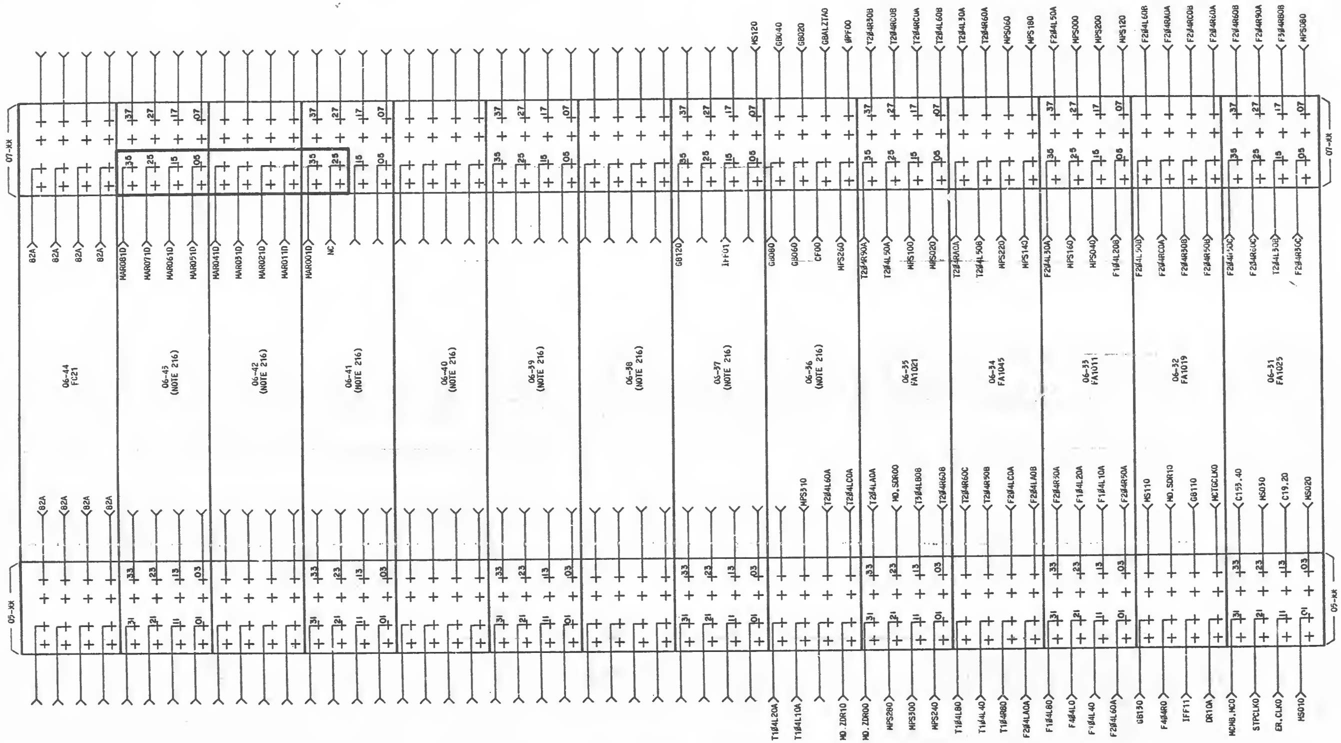
INFORMATION NOTES: (CONT)

314. (CONT)



(REAR VIEW)

3A CENTRAL CONTROL ②

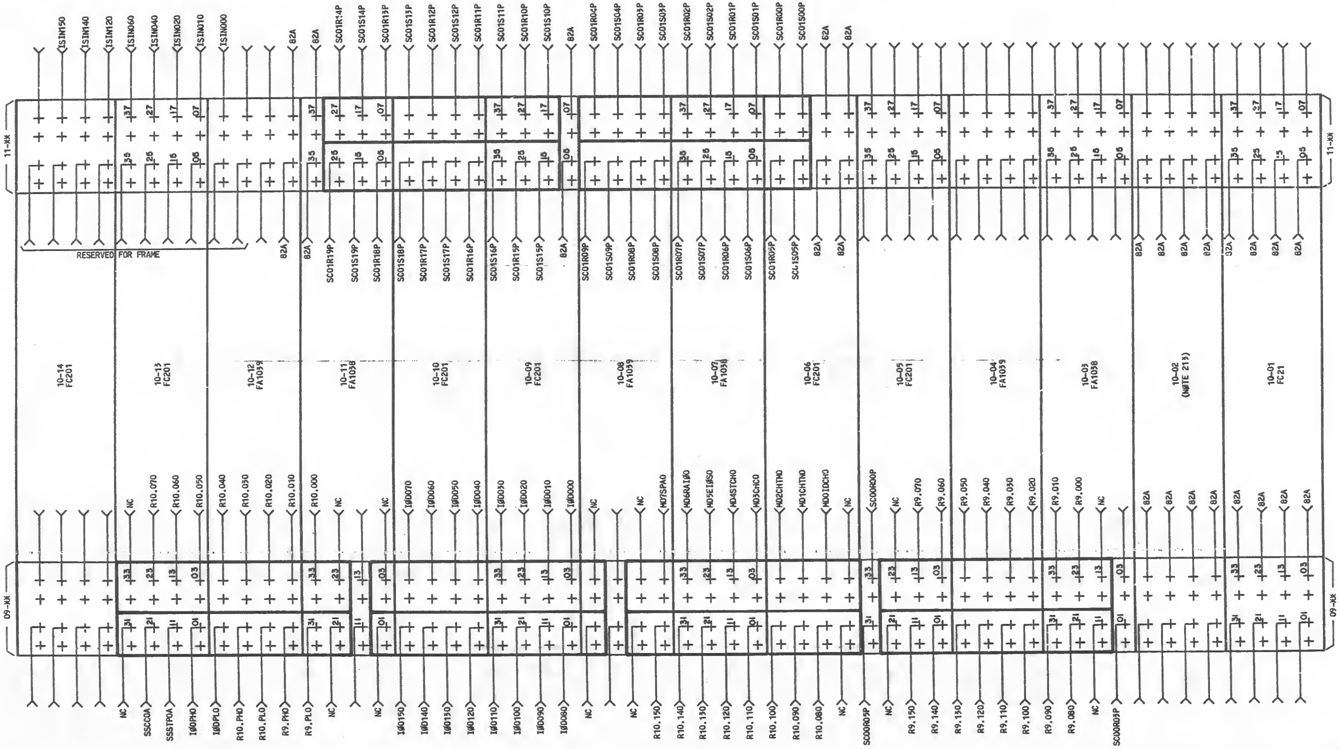
DWG SIZE	ISSUE
6S	3A

BELL LABORATORIES SD-1C900-01 D21

8262-110173

INFORMATION NOTES: (CONT)

314. (CONT)



(REAR VIEW)

3A CENTRAL CONTROL ②

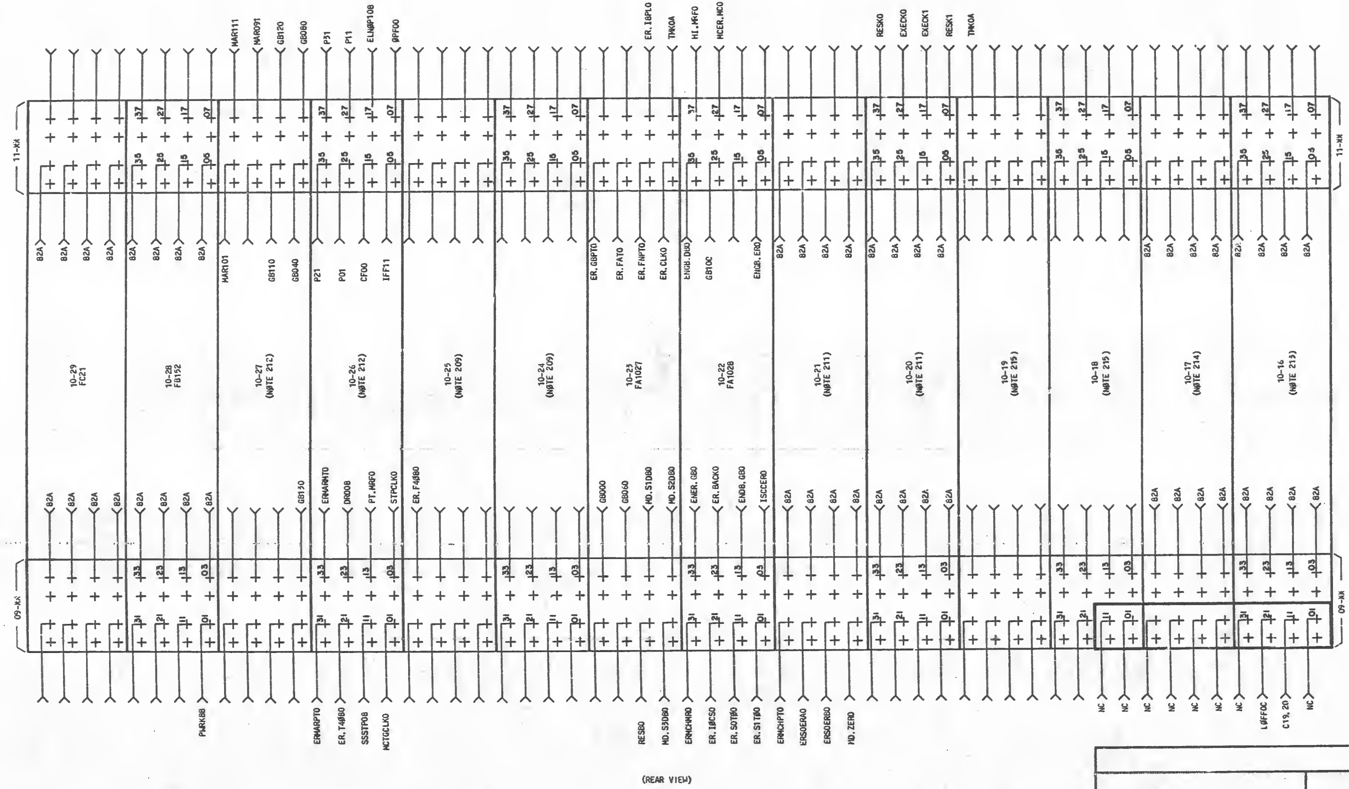
DWG SIZE	ISSUE
6S	5A

BELL LABORATORIES SD-1C900-01 D22

8262-110173

INFORMATION NOTES: (CONT)

314. (CONT)



(REAR VIEW)

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

023

8262-110173

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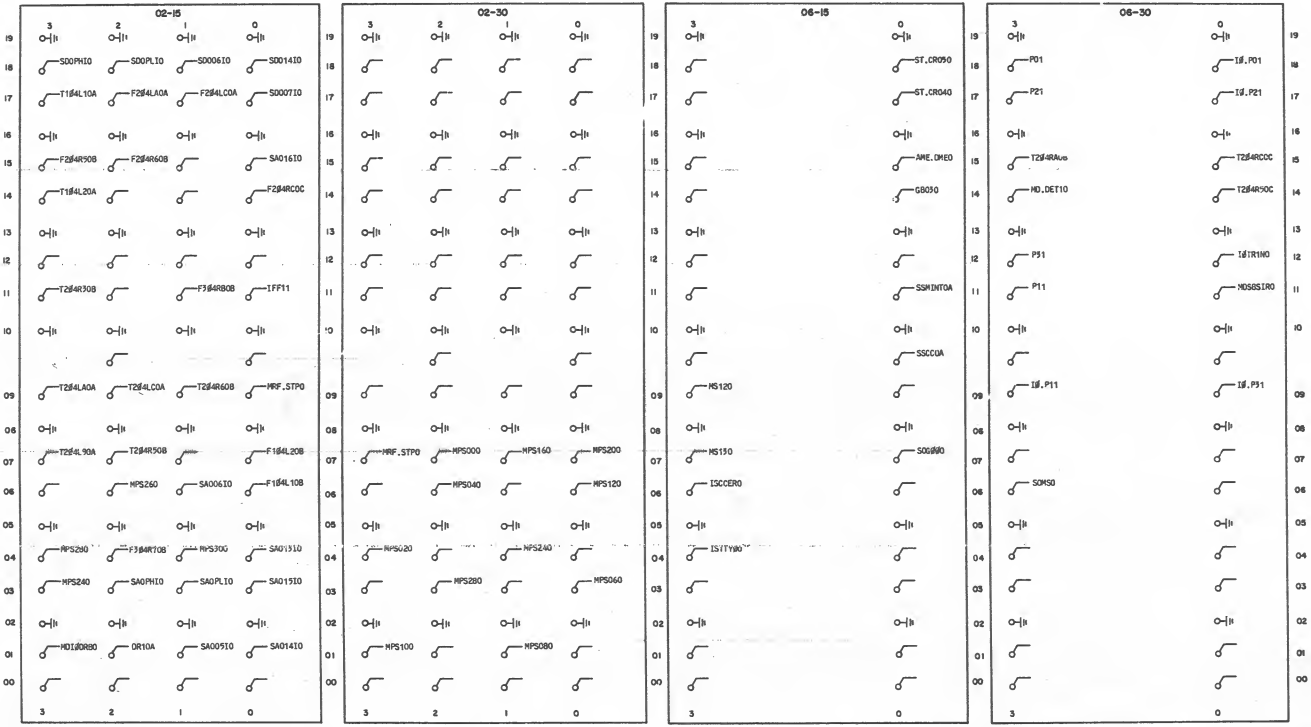
INFORMATION NOTES: (CONT)

314. (CONT)



(REAR VIEW)

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

D24

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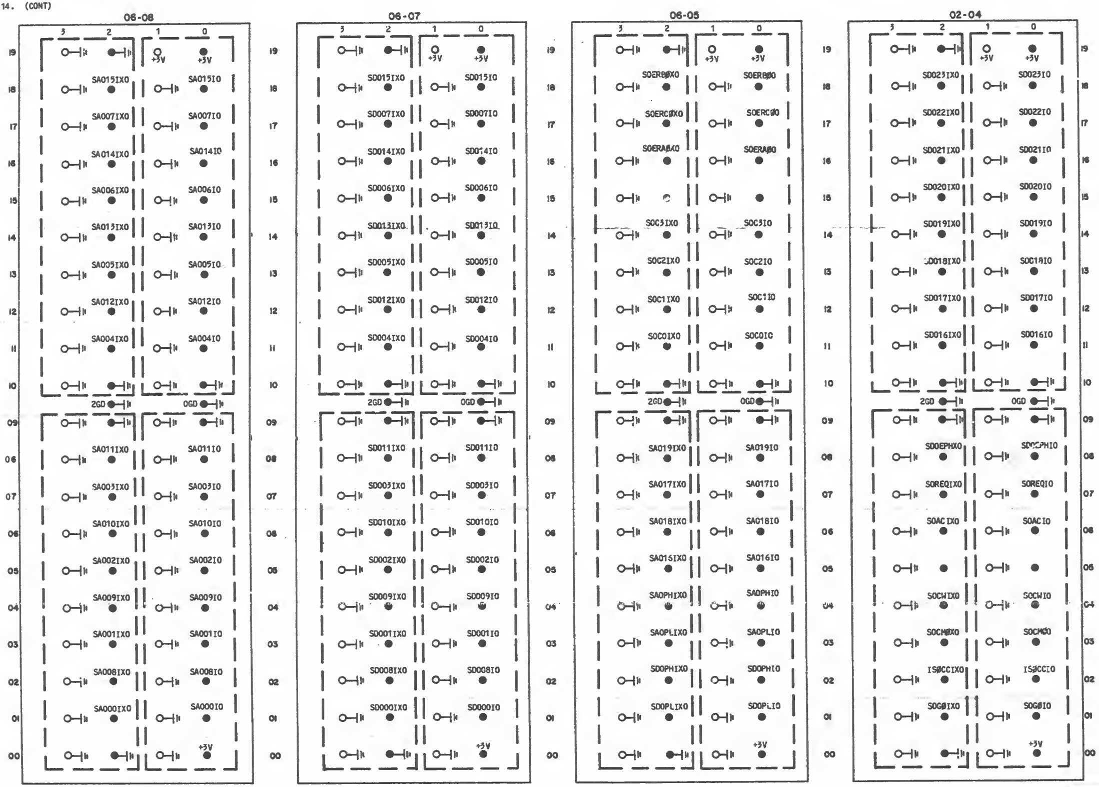
INFØRMATIØN NØTES: (CONT)

314. (CONT)



● CIRCUIT PACK TERMINALS

(REAR VIEW)

3A CENTRAL CONTRØL

	DWG SIZE 6S	ISSUE 5A
BELL LABORATORIES	SD-1C900-01	025

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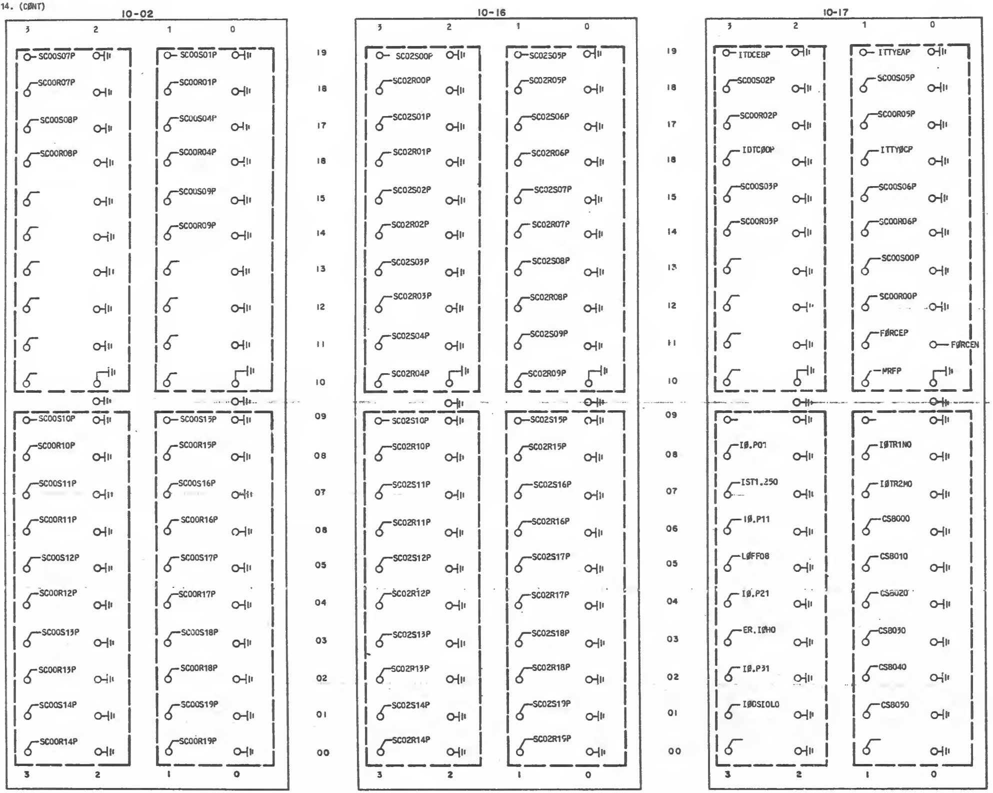
INFORMATION NOTES: (CONT)
314. (CONT)



(REAR VIEW)

3A CENTRAL CONTROL

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

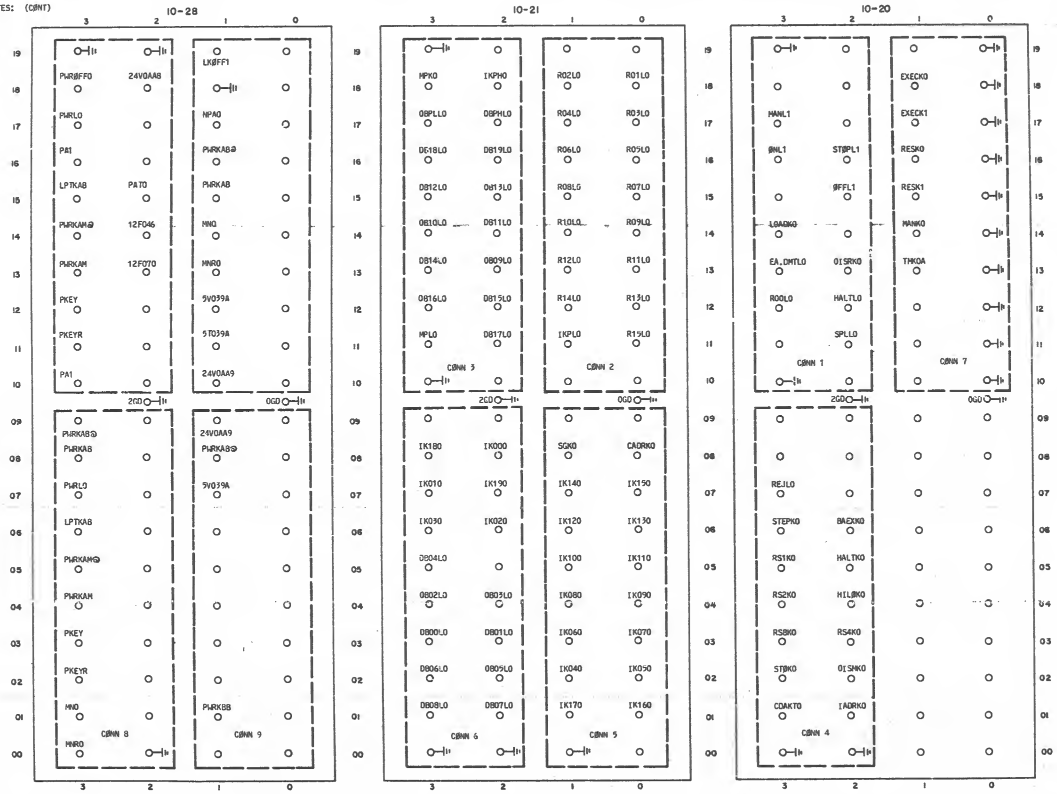
SD-1C900-01

D26

IH080173

INFØRMATIØN NØTES: (CØNT)

314. (CØNT)



10-28

	3	2	1	0
19	⏚	⏚	LKØFF1	
18	PWRØFFO	24V0AA8	⏚	
17	PWRLO		NPAO	
16	PA1		PWRKAB@	
15	LPTKAB	PAT0	PWRKAB	
14	PWRKAM@	12F046	MNO	
13	PWRKAM	12F070	MNRO	
12	PKEY		5V039A	
11	PKEYR		5T039A	
10	PA1		24V0AA9	
	CØNN 8		CØNN 9	
		2GD ⏚		0GD ⏚
09	PWRKAB@		24V0AA9	
08	PWRKAB		PWRKAB@	
07	PWRLO		5V039A	
06	LPTKAB			
05	PWRKAM@			
04	PWRKAM			
03	PKEY			
02	PKEYR			
01	MNO		PWRKBB	
00	MNRO	⏚		

10-21

	3	2	1	0
19	⏚			
18	MPKO	IKPHO	R02LO	R01LO
17	DBPLLO	DBPHLO	R04LO	R03LO
16	DB18LO	DB19LO	R06LO	R05LO
15	DB12LO	DB13LO	R08LO	R07LO
14	DB10LO	DB11LO	R10LO	R09LO
13	DB14LO	DB09LO	R12LO	R11LO
12	DB16LO	DB15LO	R14LO	R13LO
11	MPLO	DB17LO	IKPLO	R15LO
10	⏚			
	CØNN 3		CØNN 2	
		2GD ⏚		0GD ⏚
09				
08	IK180	IK000	SGKO	CADRKO
07	IK010	IK190	IK140	IK150
06	IK030	IK020	IK120	IK130
05	DB04LO		IK100	IK110
04	DB02LO	DB03LO	IK080	IK090
03	DB00LO	DB01LO	IK060	IK070
02	DB06LO	DB05LO	IK040	IK050
01	DB08LO	DB07LO	IK170	IK160
00	⏚	⏚	⏚	
	CØNN 6		CØNN 5	

10-20

	3	2	1	0
19	⏚			⏚
18			EXECKO	⏚
17	MANL1		EXECK1	⏚
16	ØNL1	STØPL1	RESKO	⏚
15		ØFFL1	RESK1	⏚
14	LOADKO		MANKO	⏚
13	EA.DMTLO	OISRKO	TMKOA	⏚
12	ROOLO	HALTLO		⏚
11		SPLLO		⏚
10	⏚			⏚
	CØNN 1		CØNN 7	
		2GD ⏚		0GD ⏚
09				
08				
07	REJLO			
06	STEPKO	BAEXKO		
05	RS1KO	HALTKO		
04	RS2KO	HILØKO		
03	RS8KO	RS4KO		
02	STØKO	OISMKO		
01	CDAKTO	IADRKO		
00	⏚	⏚		
	CØNN 4			

(REAR VIEW)

3A CENTRAL CØNTRØL ②

DWG SIZE 6S

ISSUE 3A

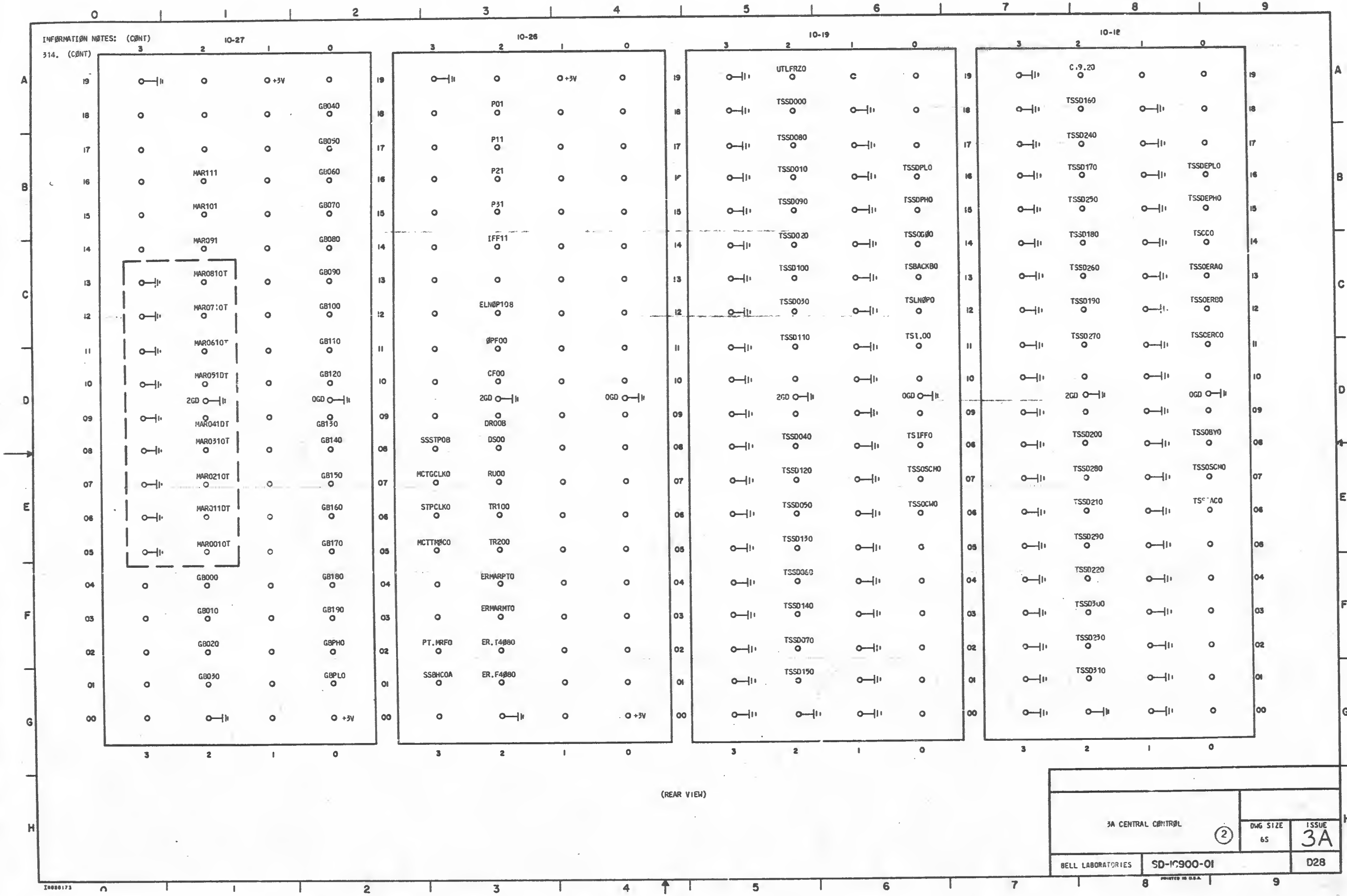
BELL LABORATORIES

SD-1C900-01

D27

INFØRMATIØN NØTES: (CØNT)

314. (CØNT)



10-27

	3	2	1	0
19	⏚	○	○ +3V	○
18	○	○	○	GB040
17	○	○	○	GB050
16	○	MAR111	○	GB060
15	○	MAR101	○	GB070
14	○	MAR091	○	GB080
13	⏚	MAR0810T	○	GB090
12	⏚	MAR0710T	○	GB100
11	⏚	MAR0610T	○	GB110
10	⏚	MAR051DT	○	GB120
		2GD ⏚		0GD ⏚
09	⏚	MAR041DT	○	GB130
08	⏚	MAR0310T	○	GB140
07	⏚	MAR0210T	○	GB150
06	⏚	MAR011DT	○	GB160
05	⏚	MAR0010T	○	GB170
04	○	GB000	○	GB180
03	○	GB010	○	GB190
02	○	GB020	○	GBPH0
01	○	GB030	○	GBPL0
00	○	⏚	○	○ +3V

10-26

	3	2	1	0
19	⏚	○	○ +3V	○
18	○	P01	○	○
17	○	P11	○	○
16	○	P21	○	○
15	○	P31	○	○
14	○	IFF11	○	○
13	○	○	○	○
12	○	ELNØP108	○	○
11	○	ØPF00	○	○
10	○	CF00	○	○
		2GD ⏚		0GD ⏚
09	○	DR00B	○	○
08	SSSTP0B	DS00	○	○
07	MCTGCLK0	RU00	○	○
06	STPCLK0	TR100	○	○
05	MCTTMØC0	TR200	○	○
04	○	ERMARPT0	○	○
03	○	ERMARMT0	○	○
02	PT.MRF0	ER.T4Ø80	○	○
01	SSBHC0A	ER.F4Ø80	○	○
00	○	⏚	○	○ +3V

10-19

	3	2	1	0
19	⏚	UTLFRZ0	○	○
18	⏚	TSSD000	⏚	○
17	⏚	TSSD080	⏚	○
16	⏚	TSSD010	⏚	TSSDPL0
15	⏚	TSSD090	⏚	TSSDPH0
14	⏚	TSSD020	⏚	TSSOGØ0
13	⏚	TSSD100	⏚	TSBACKB0
12	⏚	TSSD030	⏚	TSLNØP0
11	⏚	TSSD110	⏚	TS1.00
10	⏚	○	⏚	○
		2GD ⏚		0GD ⏚
09	⏚	○	⏚	○
08	⏚	TSSD040	⏚	TSIFF0
07	⏚	TSSD120	⏚	TSSOSCM0
06	⏚	TSSD050	⏚	TSSOCW0
05	⏚	TSSD130	⏚	○
04	⏚	TSSD060	⏚	○
03	⏚	TSSD140	⏚	○
02	⏚	TSSD070	⏚	○
01	⏚	TSSD150	⏚	○
00	⏚	⏚	⏚	○

10-12

	3	2	1	0
19	⏚	C.9.20	○	○
18	⏚	TSSD160	⏚	○
17	⏚	TSSD240	⏚	○
16	⏚	TSSD170	⏚	TSSDEPL0
15	⏚	TSSD250	⏚	TSSDEPH0
14	⏚	TSSD180	⏚	TSCC0
13	⏚	TSSD260	⏚	TSSOERA0
12	⏚	TSSD190	⏚	TSSOERB0
11	⏚	TSSD270	⏚	TSSCERC0
10	⏚	○	⏚	○
		2GD ⏚		0GD ⏚
09	⏚	○	⏚	○
08	⏚	TSSD200	⏚	TSSOBY0
07	⏚	TSSD280	⏚	TSSOSCM0
06	⏚	TSSD210	⏚	TS[illegible]AC0
05	⏚	TSSD290	⏚	○
04	⏚	TSSD220	⏚	○
03	⏚	TSSD300	⏚	○
02	⏚	TSSD230	⏚	○
01	⏚	TSSD310	⏚	○
00	⏚	⏚	⏚	○

(REAR VIEW)

3A CENTRAL CØNTRØL ②

DWG SIZE 6S

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

D28

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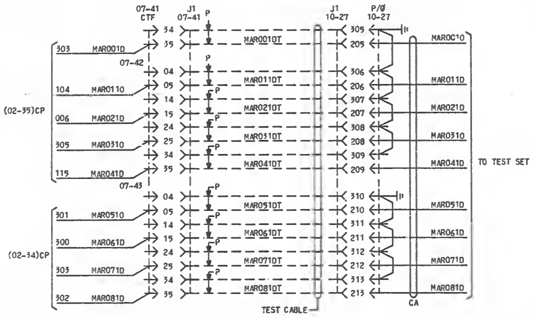
INFORMATION NOTES: (CONT)

315. CABLING BETWEEN MICROSTORE 'MAR' LEADS AND TEST POSITION 10-27 IS ACCOMPLISHED VIA A TEST SET CABLE AND WILL BE CONNECTED ONLY DURING TEST. SEE DIAGRAM BELOW.



3A CENTRAL CONTROL

DWG SIZE 65

ISSUE 3A

BELL LABORATORIES

SD-1C900-01

D29

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NOTES:

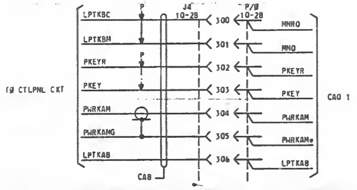
1. THE FOLLOWING ABBREVIATIONS ARE USED IN CADS:

ABBREVIATION	CIRCUIT NAME
CTLPNL CKT	3ACC CONTROL PANEL CKT

2. THIS TERMINAL HAS A COMMON GROUND THROUGH THE MLPWB GROUND PLANE.

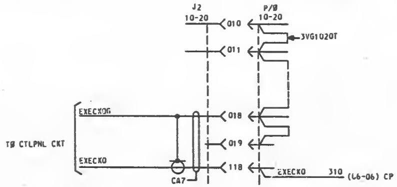
3. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION.

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....	J4			10-28	JACK/CP	(NOTE 3).............	....		
TO CTLPNL CKT	LPTKBC	CA8	P2	300	MNRO	CAD 1			
|	LPTKBM	CA8	P2	301	MNO	CAD 1			
|	PKEYR	CA8	P3	302	PKEYR	CAD 1			
|	PKEY	CA8	P3	303	PKEY	CAD 1			
|	PWRKAM	CA8	CX1	304	PWRKAM	CAD 1			
|	PWRKAMG	CA8	CX1	305	PWRXAMe	CAD 1			
TO CTLPNL CKT	LPTKAB	CA8		306	LPTKAB	CAD 1			



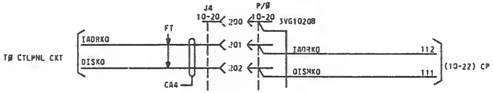
4. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION.

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....	J2			10-20	JACK/CONN	(NOTE 4).............	....		
	NC			010	3VG1020T	10-20 CONN	011		
	NC			011	3VG1020T	10-20 CONN	012		
TO CTLPNL CKT	EXECKOG	CA7	CX6	018	3VG1020T	10-20 CONN	019		
	NC			019	3VG1020T	10-20 CONN	319		
TO CTLPNL CKT	EXECKO	CA7	CK6	118	EXECKO	06-06 CP	310		



5. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENATATION.

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIPE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....	J4			10-20	JACK/CONN	(NOTE 5).............	....		
	NC			200	3VG10208	10-20 CONN	300		
TO CTLPNL CKT	IADRKO	CA4	FT	201	IADRKO	10-22 CP	112		
|	DISKO	CA4	FT	202	DISMKO	10-22 CP	111		

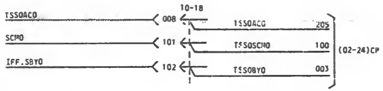


6. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION.

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....	+5A			09-36T	LUG	(NOTE 6).............	....		
TO CONN CKT	SV061A			+5A	SV061A				

7. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION.

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....	TS4			10-18	CONNECTOR	(NOTE 7).............	....		
	TSSOACO			006	TSSOACD	02-24 CP	205		
	SCMO			007	TSSOSCMO	02-24 CP	100		
	IFF.SBYO			008	TSSOBYO	02-24 CP	003		



3A

3A CENTRAL CONTROL

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

SD-1C900-01-GB1

CAD 1

UNIT SYMBOL

ELEMENT IDENTIFIER

A

MAIN STORE BUS 0(OUTPUT)

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
SA0PH00	0	01-17-01	02-18-102	4/5	
SA0PL00	0	01-16-31	02-18-003	4/5	
SA00000	0	01-08-13	02-08-003	4/15	
SA00100	0	01-08-33	02-09-003	4/14	
SA00200	0	01-09-13	02-10-003	4/13	
SA00300	0	01-09-33	02-11-003	4/12	
SA00400	0	01-11-13	02-12-003	4/11	
SA00500	0	01-11-33	02-13-003	4/10	
SA00600	0	01-12-13	02-16-003	4/9	
SA00700	0	01-12-33	02-17-003	4/8	
SA00800	0	01-08-23	02-08-102	4/15	
SA00900	0	01-09-03	02-09-102	4/14	
SA01000	0	01-09-23	02-10-102	4/13	
SA01100	0	01-10-03	02-11-102	4/12	
SA01200	0	01-11-23	02-12-102	4/11	
SA01300	0	01-12-03	02-13-102	4/10	
SA01400	0	01-12-23	02-16-102	4/9	
SA01500	0	01-13-03	02-17-102	4/8	
SA01600	0	01-17-11	02-19-101	4/7	
SA01700	0	01-17-31	02-20-101	4/6	
SA01800	0	01-17-21	02-19-201	4/7	
SA01900	0	01-18-01	02-20-201	4/6	
SD0EPH00	0I	01-20-31	02-07-209	11/1	
SD0PH00	0I	01-16-21	02-18-218	4/5	
SD0PL00	0I	01-16-11	02-18-317	4/5	
SD00000	0I	01-08-11	02-08-317	4/15	
SD00100	0I	01-08-31	02-09-317	4/14	
SD00200	0I	01-09-11	02-10-317	4/13	
SD00300	0I	01-09-31	02-11-317	4/12	
SD00400	0I	01-11-11	02-12-317	4/11	
SD00500	0I	01-11-31	02-13-317	4/10	
SD00600	0I	01-12-11	02-16-317	4/9	
SD00700	0I	01-12-31	02-17-317	4/8	
SD00800	0I	01-08-21	02-08-218	4/15	
SD00900	0I	01-09-01	02-09-218	4/14	
SD01000	0I	01-09-21	02-10-218	4/13	
SD01100	0I	01-10-01	02-11-218	4/12	
SD01200	0I	01-11-21	02-12-218	4/11	
SD01300	0I	01-12-01	02-13-218	4/10	
SD01400	0I	01-12-21	02-16-218	4/9	
SD01500	0I	01-13-01	02-17-218	4/8	
SD01600	0I	01-05-21	02-06-203	11/2	
SD01700	0I	01-05-31	02-06-305	11/2	
SD01800	0I	01-06-01	02-06-108	11/2	
SD01900	0I	01-06-11	02-06-209	11/2	
SD02000	0I	01-06-21	02-07-007	11/1	
SD02100	0I	01-06-31	02-07-207	11/1	
SD02200	0I	01-07-01	02-07-203	11/1	
SD02300	0I	01-07-11	02-07-305	11/1	
S0AC00	0	01-20-11	02-23-111	4/2	
S0BYI0	I	01-20-01	02-24-017	7/3	
S0CMI0	I0	01-19-21	02-21-302	4/1	
S0CW00	0	01-19-31	02-23-009	4/2	
S0C000	0	01-16-13	02-21-012	4/1	
S0C100	0	01-16-23	02-21-110	4/1	
S0C200	0	01-16-33	02-21-108	4/1	
S0C300	0I	01-17-03	02-21-311	4/1	
S0ERAI0	I	01-17-23	02-23-219	4/2	
S0ERBI0	I	01-18-03	02-23-019	4/2	
S0ERCI0	I	01-17-33	02-23-014	4/2	
S0G000	0I	01-19-01	02-21-209	4/1	
S0MS0	0	01-17-13	06-31-306	8/3	
S0REQ00	0	01-20-21	02-21-008	4/1	
3C0119B	G	01-19-11			

ELEMENT IDENTIFIER

B

MAIN STORE BUS 0(INPUT)

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
ISDCCIX0	0	02-04-202	02-04-202	13/4	
SA0PHIX0	0	06-05-204	06-05-204	13/1	
SA0PLIX0	0	06-05-203	06-05-203	13/1	
SA000IX0	0	06-08-201	06-08-201	13/3	
SA001IX0	0	06-08-203	06-08-203	13/3	
SA002IX0	0	06-08-205	06-08-205	13/3	
SA003IX0	0	06-08-207	06-08-207	13/3	
SA004IX0	0	06-08-211	06-08-211	13/3	
SA005IX0	0	06-08-213	06-08-213	13/3	
SA006IX0	0	06-08-215	06-08-215	13/3	
SA007IX0	0	06-08-217	06-08-217	13/3	
SA008IX0	0	06-08-202	06-08-202	13/3	
SA009IX0	0	06-08-204	06-08-204	13/3	
SA010IX0	0	06-08-206	06-08-206	13/3	
SA011IX0	0	06-08-208	06-08-208	13/3	
SA012IX0	0	06-08-212	06-08-212	13/3	
SA013IX0	0	06-08-214	06-08-214	13/3	
SA014IX0	0	06-08-216	06-08-216	13/3	
SA015IX0	0	06-08-218	06-08-218	13/3	
SA016IX0	0	06-05-205	06-05-205	13/1	
SA017IX0	0	06-05-207	06-05-207	13/1	
SA018IX0	0	06-05-206	06-05-206	13/1	
SA019IX0	0	06-05-208	06-05-208	13/1	
SD0EPHX0	0	02-04-208	02-04-208	13/4	
SD0PHIX0	0	06-05-202	06-05-202	13/1	
SD0PLIX0	0	06-05-201	06-05-201	13/1	
SD000IX0	0	06-07-201	06-07-201	13/2	
SD001IX0	0	06-07-203	06-07-203	13/2	
SD002IX0	0	06-07-205	06-07-205	13/2	
SD003IX0	0	06-07-207	06-07-207	13/2	
SD004IX0	0	06-07-211	06-07-211	13/2	
SD005IX0	0	06-07-213	06-07-213	13/2	
SD006IX0	0	06-07-215	06-07-215	13/2	
SD007IX0	0	06-07-217	06-07-217	13/2	
SD008IX0	0	06-07-202	06-07-202	13/2	
SD009IX0	0	06-07-204	06-07-204	13/2	
SD010IX0	0	06-07-206	06-07-206	13/2	
SD011IX0	0	06-07-208	06-07-208	13/2	
SD012IX0	0	06-07-212	06-07-212	13/2	
SD013IX0	0	06-07-214	06-07-214	13/2	
SD014IX0	0	06-07-216	06-07-216	13/2	
SD015IX0	0	06-07-218	06-07-218	13/2	
SD016IX0	0	02-04-211	02-04-211	13/4	
SD017IX0	0	02-04-212	02-04-212	13/4	
SD018IX0	0	02-04-213	02-04-213	13/4	
SD019IX0	0	02-04-214	02-04-214	13/4	
SD020IX0	0	02-04-215	02-04-215	13/4	
SD021IX0	0	02-04-216	02-04-216	13/4	
SD022IX0	0	02-04-217	02-04-217	13/4	
SD023IX0	0	02-04-218	02-04-218	13/4	
S0ACIX0	0	02-04-206	02-04-206	13/4	
S0CM0X0	0	02-04-203	02-04-203	13/4	
S0CWIX0	0	02-04-204	02-04-204	13/4	
S0C0IX0	0	06-05-211	06-05-211	13/1	
S0C1IX0	0	06-05-212	06-05-212	13/1	
S0C2IX0	0	06-05-213	06-05-213	13/1	
S0C3IX0	0	06-05-214	06-05-214	13/1	
S0ERA0X0	0	06-05-216	06-05-216	13/1	
S0ERB0X0	0	06-05-218	06-05-218	13/1	
S0ERC0X0	0	06-05-217	06-05-217	13/1	
S0G0IX0	0	02-04-201	02-04-201	13/4	
S0RE0IX0	0	02-04-207	02-04-207	13/4	

ELEMENT IDENTIFIER

C

MAIN STORE BUS 0(INPUT)
(BYPASS FUSE PACKS)

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
ISDCCI0	I	02-04-002	06-17-106	5/7	
SA0PHI0	I	06-05-004	02-18-202	4/5	
SA0PLI0	I	06-05-003	02-18-002	4/5	
SA00010	I	06-08-001	02-08-002	4/15	
SA00110	I	06-08-003	02-09-002	4/14	
SA00210	I	06-08-005	02-10-002	4/13	
SA00310	I	06-08-007	02-11-002	4/12	
SA00410	I	06-08-011	02-12-002	4/11	
SA00510	I	06-08-013	02-13-002	4/10	
SA00610	I	06-08-015	02-16-002	4/9	
SA00710	I	06-08-017	02-17-002	4/8	
SA00810	I	06-08-002	02-08-202	4/15	
SA00910	I	06-08-004	02-09-202	4/14	
SA01010	I	06-08-006	02-10-202	4/13	
SA01110	I	06-08-008	02-11-202	4/12	
SA01210	I	06-08-012	02-12-202	4/11	
SA01310	I	06-08-014	02-13-202	4/10	
SA01410	I	06-08-016	02-16-202	4/9	
SA01510	I	06-08-018	02-17-202	4/8	
SA01610	I	06-05-005	02-19-217	4/7	
SA01710	I	06-05-007	02-20-217	4/6	
SA01810	I	06-05-006	02-19-207	4/7	
SA01910	I	06-05-008	02-20-207	4/6	
SD0EPHI0	0I	02-04-008	02-07-302	11/1	
SD0PHI0	0I	06-05-002	02-18-018	4/5	
SD0PLI0	0I	06-05-001	02-18-117	4/5	
SD00010	0I	06-07-001	02-08-117	4/15	
SD00110	0I	06-07-003	02-09-117	4/14	
SD00210	0I	06-07-005	02-10-117	4/13	
SD00310	0I	06-07-007	02-11-117	4/12	
SD00410	0I	06-07-011	02-12-117	4/11	
SD00510	0I	06-07-013	02-13-117	4/10	
SD00610	0I	06-07-015	02-16-117	4/9	
SD00710	0I	06-07-017	02-17-117	4/8	
SD00810	0I	06-07-002	02-08-018	4/15	
SD00910	0I	06-07-004	02-09-018	4/14	
SD01010	0I	06-07-006	02-10-018	4/13	
SD01110	0I	06-07-008	02-11-018	4/12	
SD01210	0I	06-07-012	02-12-018	4/11	
SD01310	0I	06-07-014	02-13-018	4/10	
SD01410	0I	06-07-016	02-16-018	4/9	
SD01510	0I	06-07-018	02-17-018	4/8	
SD01610	0I	02-04-011	02-06-003	11/2	
SD01710	0I	02-04-012	02-06-105	11/2	
SD01810	0I	02-04-013	02-06-208	11/2	
SD01910	0I	02-04-014	02-06-302	11/2	
SD02010	0I	02-04-015	02-07-006	11/1	
SD02110	0I	02-04-016	02-07-008	11/1	
SD02210	0I	02-04-017	02-07-003	11/1	
SD02310	0I	02-04-018	02-07-105	11/1	
S0ACI0	I	02-04-006	02-23-213	4/2	
S0CM00	0	02-04-003	02-21-210	4/1	
S0CWI0	I	02-04-004	02-23-212	4/2	
S0C0I0	I	06-05-011	02-21-102	4/1	
S0C1I0	I	06-05-012	02-21-017	4/1	
S0C2I0	I	06-05-013	02-21-316	4/1	
S0C3I0	I	06-05-014	02-21-219	4/1	
S0ERA00	0	06-05-016	02-23-312	4/2	
S0ERB00	0	06-05-018	02-23-112	4/2	
S0ERC00	0	06-05-017	02-23-115	4/2	
S0G0I0	I	02-04-001	02-21-306	4/1	
S0REQI0	I	02-04-007	02-21-106	4/1	

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	5A

BELL LABORATORIES | SD-1C900-01 | GB2

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CAD 1

UNIT SYMBOL

ELEMENT IDENTIFIER

O

MAIN STORE BUS 1(OUTPUT)

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
MDIOCC0	0	03-19-15	02-20-205	1/14	
SA1PH00	0	03-17-07	02-18-203	4/5	
SA1PL00	0	03-16-37	02-18-103	4/5	
SA10000	0	03-08-15	02-08-103	4/15	
SA10100	0	03-08-35	02-09-103	4/14	
SA10200	0	03-09-15	02-10-103	4/13	
SA10300	0	03-09-35	02-11-103	4/12	
SA10400	0	03-11-15	02-12-103	4/11	
SA10500	0	03-11-35	02-13-103	4/10	
SA10600	0	03-12-15	02-16-103	4/9	
SA10700	0	03-12-35	02-17-103	4/8	
SA10800	0	03-08-25	02-08-203	4/15	
SA10900	0	03-09-05	02-09-203	4/14	
SA11000	0	03-09-25	02-10-203	4/13	
SA11100	0	03-10-05	02-11-203	4/12	
SA11200	0	03-11-25	02-12-203	4/11	
SA11300	0	03-12-05	02-13-203	4/10	
SA11400	0	03-12-25	02-16-203	4/9	
SA11500	0	03-13-05	02-17-203	4/8	
SA11600	0	03-17-17	02-19-001	4/7	
SA11700	0	03-17-37	02-20-001	4/6	
SA11800	0	03-17-27	02-19-300	4/7	
SA11900	0	03-18-07	02-20-300	4/6	
SD1EPH00	0I	03-20-35	02-07-112	11/1	
S01PH00	0I	03-16-27	02-18-219	4/5	
S01PL00	0I	03-16-17	02-18-318	4/5	
S010000	0I	03-08-17	02-08-318	4/15	
S010100	0I	03-08-37	02-09-318	4/14	
S010200	0I	03-09-17	02-10-318	4/13	
S010300	0I	03-09-37	02-11-318	4/12	
SD10400	0I	03-11-17	02-12-318	4/11	
S010500	0I	03-11-37	02-13-318	4/10	
SD10600	0I	03-12-17	02-16-318	4/9	
S010700	0I	03-12-37	02-17-318	4/8	
S010800	0I	03-08-27	02-08-219	4/15	
SD10900	0I	03-09-07	02-09-219	4/14	
S011000	0I	03-09-27	02-10-219	4/13	
SD11100	0I	03-10-07	02-11-219	4/12	
S011200	0I	03-11-27	02-12-219	4/11	
S011300	0I	03-12-07	02-13-219	4/10	
SD11400	0I	03-12-27	02-16-219	4/9	
S011500	0I	03-13-07	02-17-219	4/8	
S011600	0I	03-05-25	02-06-013	11/2	
SD11700	0I	03-05-35	02-06-113	11/2	
SD11800	0I	03-06-05	02-06-315	11/2	
SD11900	0I	03-06-15	02-06-112	11/2	
S012000	0I	03-06-25	02-07-014	11/1	
S012100	0I	03-06-35	02-07-308	11/1	
SD12200	0I	03-07-05	02-07-013	11/1	
SD12300	0I	03-07-15	02-07-113	11/1	
S1AC00	0	03-20-15	02-23-106	4/2	
S1CMI0	I0	03-19-25	02-22-302	4/3	
S1CW00	0	03-19-35	02-23-209	4/2	
S1C000	0	03-16-15	02-22-012	4/3	
S1C100	0	03-16-25	02-22-110	4/3	
S1C200	0	03-16-35	02-22-108	4/3	
S1C300	0I	03-17-05	02-22-311	4/3	
S1ERAI0	I	03-17-25	02-23-012	4/2	
S1ERBI0	I	03-18-05	02-23-005	4/2	
S1ERCI0	I	03-17-35	02-23-318	4/2	
S1G000	0	03-19-05	02-22-208	4/3	
S1RE000	0	03-20-25	02-22-008	4/3	

ELEMENT IDENTIFIER

E

MAIN STORE BUS 1(INPUT)

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
SA1PHI0	I	05-23-03	02-18-301	4/5	
SA1PLI0	I	05-22-33	02-18-101	4/5	
SA100I0	I	05-12-33	02-08-101	4/15	
SA101I0	I	05-13-13	02-09-101	4/14	
SA102I0	I	05-13-33	02-10-101	4/13	
SA103I0	I	05-14-13	02-11-101	4/12	
SA104I0	I	07-12-37	02-12-101	4/11	
SA105I0	I	07-13-17	02-13-101	4/10	
SA106I0	I	07-13-37	02-16-101	4/9	
SA107I0	I	07-14-17	02-17-101	4/8	
SA108I0	I	05-13-03	02-08-301	4/15	
SA109I0	I	05-13-23	02-09-301	4/14	
SA110I0	I	05-14-03	02-10-301	4/13	
SA111I0	I	05-14-23	02-11-301	4/12	
SA112I0	I	07-13-07	02-12-301	4/11	
SA113I0	I	07-13-27	02-13-301	4/10	
SA114I0	I	07-14-07	02-16-301	4/9	
SA115I0	I	07-14-27	02-17-301	4/8	
SA116I0	I	05-23-13	02-19-019	4/7	
SA117I0	I	05-23-33	02-20-019	4/6	
SA118I0	I	05-23-23	02-19-219	4/7	
SA119I0	I	05-24-03	02-20-219	4/6	
S01EPHI0	0I	05-24-01	02-07-212	11/1	
S01PHI0	0I	05-22-23	02-18-019	4/5	
S01PLI0	0I	05-22-13	02-18-118	4/5	
S0100I0	0I	05-12-31	02-08-118	4/15	
S0101I0	0I	05-13-11	02-09-118	4/14	
S0102I0	0I	05-13-31	02-10-118	4/13	
S0103I0	0I	05-14-11	02-11-118	4/12	
SD104I0	0I	07-12-35	02-12-118	4/11	
S0105I0	0I	07-13-15	02-13-118	4/10	
S0106I0	0I	07-13-35	02-16-118	4/9	
SD107I0	0I	07-14-15	02-17-118	4/8	
SD108I0	0I	05-13-01	02-08-019	4/15	
S0109I0	0I	05-13-21	02-09-019	4/14	
S0110I0	0I	05-14-01	02-10-019	4/13	
SD111I0	0I	05-14-21	02-11-019	4/12	
SD112I0	0I	07-13-05	02-12-019	4/11	
SD113I0	0I	07-13-25	02-13-019	4/10	
S0114I0	0I	07-14-05	02-16-019	4/9	
S0115I0	0I	07-14-25	02-17-019	4/8	
S1ACI0	I	05-23-21	02-23-309	4/2	
S1CM00	0	05-22-31	02-22-210	4/3	
S1CWI0	I	05-23-01	02-23-306	4/2	
S1C0I0	I	07-22-17	02-22-102	4/3	
S1C1I0	I	07-22-27	02-22-017	4/3	
S1C2I0	I	07-22-37	02-22-316	4/3	
S1C3I0	I	07-23-07	02-22-219	4/3	
S1ERA00	0	07-23-27	02-23-217	4/2	
S1ERB00	0	07-24-07	02-23-017	4/2	
S1ERC00	0	07-23-37	02-23-316	4/2	
S1G0I0	I	05-22-11	02-22-306	4/3	
S1RE0I0	I	05-23-31	02-22-106	4/3	

ELEMENT IDENTIFIER

F

I/O MAIN CHANNELS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
CSB000	0	10-17-106	10-03-111	10/1	
CSB010	0	10-17-105	10-03-307	10/1	
CSB020	0	10-17-104	10-04-202	10/2	
CSB030	0	10-17-103	10-08-202	10/6	
CSB040	I	10-17-102	02-31-109	6/5	
CSB050	I	10-17-101	02-31-309	6/5	
C19.20	0	09-16-11	06-31-103	8/3	
ER.IOH0	0	10-17-303	06-20-214	2/9	
IO.P01	0I	10-17-308	06-31-218	8/3	
IO.P11	0I	10-17-306	06-31-010	8/3	
IO.P21	0	10-17-304	06-29-207	8/5	
IO.P31	0	10-17-302	06-29-205	8/5	
IODPH0	0	09-13-01	10-04-013	10/2	
IODPL0	0	09-12-31	10-04-009	10/2	
IODSIOL0	0	10-17-301	10-03-014	10/1	
IOD000	0	09-09-03	10-03-301	10/1	
IOD010	0	09-09-13	10-03-101	10/1	
IOD020	0	09-09-23	10-03-201	10/1	
IOD030	0	09-09-33	10-03-001	10/1	
IOD040	0	09-10-03	10-03-300	10/1	
IOD050	0	09-10-13	10-03-100	10/1	
IOD060	0	09-10-23	10-03-218	10/1	
IOD070	0	09-10-33	10-03-018	10/1	
IOD080	0	09-09-01	10-03-219	10/1	
IOD090	0	09-09-11	10-03-019	10/1	
IOD100	0	09-09-21	10-03-318	10/1	
IOD110	0	09-09-31	10-03-118	10/1	
IOD120	0	09-10-01	10-04-309	10/2	
IOD130	0	09-10-11	10-04-109	10/2	
IOD140	0	09-10-21	10-04-209	10/2	
IOD150	0	09-10-31	10-04-213	10/2	
IOTR1N0	0	10-17-108	10-04-002	10/2	
IOTR2M0	0	10-17-107	10-04-003	10/2	
IST1.250	0	10-17-307	02-24-004	8/4	
LOFF0B	0I	10-17-305	06-06-203	7/20	
LOFF0C	0I	09-16-21	06-06-100	7/20	
MD0IOCH0	0	09-06-13	06-06-110	1/9	
MD1CHTN0	0	09-06-23	06-06-204	1/9	
MD2CHTM0	0	09-06-33	06-06-318	1/9	
MD3CHC0	0	09-07-03	06-06-118	1/9	
MD4STCH0	0	09-07-13	06-06-317	1/9	
MD5EIOS0	0	09-07-23	06-06-117	1/9	
MD6RAI00	0	09-07-33	06-06-218	1/9	
MD7SPA0	0	09-08-03	06-06-018	1/9	
R10.PH0	0	09-12-21	06-18-215	3/1	
R10.PL0	0	09-12-11	06-18-313	3/1	
R10.000	0	09-11-33	06-09-313	3/9	
R10.010	0	09-12-03	06-10-313	3/8	
R10.020	0	09-12-13	06-11-313	3/7	
R10.030	0	09-12-23	06-12-313	3/6	
R10.040	0	09-12-33	06-13-313	3/5	
R10.050	0	09-13-03	06-14-313	3/4	
R10.060	0	09-13-13	06-16-313	3/3	
R10.070	0	09-13-23	06-17-313	3/2	
R10.080	0	09-06-11	06-09-215	3/9	
R10.090	0	09-06-21	06-10-215	3/8	
R10.100	0	09-06-31	06-11-215	3/7	
R10.110	0	09-07-01	06-12-215	3/6	
R10.120	0	09-07-11	06-13-215	3/5	
R10.130	0	09-07-21	06-14-215	3/4	
R10.140	0	09-07-31	06-16-215	3/3	
R10.150	0	09-08-01	06-17-215	3/2	
R9.PH0	0	09-12-01	06-18-015	3/1	
R9.PL0	0	09-11-31	06-16-014	3/1	
R9.000	0	09-03-23	06-09-014	3/9	
R9.010	0	09-03-33	06-10-014	3/8	

ELEMENT IDENTIFIER (CONT)

F

I/O MAIN CHANNELS

TERM. MODIFIER	FUNC	ACCESS TERM.	TERM.	LOC FS/SYM	NOTE
R9.020	0	09-04-03	06-11-014	3/7	
R9.030	0	09-04-13	06-12-014	3/6	
R9.040	0	09-04-23	06-13-014	3/5	
R9.050	0	09-04-33	06-14-014	3/4	
R9.060	0	09-05-03	06-16-014	3/3	
R9.070	0	09-05-13	06-17-014	3/2	
R9.080	0	09-03-21	06-09-015	3/9	
R9.090	0	09-03-31	06-10-015	3/8	
R9.100	0	09-04-01	06-11-015	3/7	
R9.110	0	09-04-11	06-12-015	3/6	
R9.120	0	09-04-21	06-13-015	3/5	
R9.130	0	09-04-31	06-14-015	3/4	
R9.140	0	09-05-01	06-16-015	3/3	
R9.150	0	09-05-11	06-17-015	3/2	
SSCC0A	0	09-13-21	06-13-210	5/10	
SSSTP0A	0	09-13-11	06-16-115	5/8	

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 5A

BELL LABORATORIES

SD-1C900-01

GB3

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CAD 1

UNIT SYMBOL

ELEMENT IDENTIFIER

G

I/O SUBCHANNELS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
SC00R00N	G	10-17-012			2
SC00R00P	I	10-17-112	10-05-104	10/3	
SC00R01N	G	10-02-018			2
SC00R01P	I	10-02-118	10-05-103	10/3	
SC00R02N	G	10-17-217			2
SC00R02P	I	10-17-317	10-05-312	10/3	
SC00R03N	G	10-17-214			2
SC00R03P	I	10-17-314	10-05-102	10/3	
SC00R04N	G	10-02-016			2
SC00R04P	I	10-02-116	10-05-110	10/3	
SC00R05N	G	10-17-017			2
SC00R05P	I	10-17-117	10-05-109	10/3	
SC00R06N	G	10-17-014			2
SC00R06P	I	10-17-114	10-05-313	10/3	
SC00R07N	G	10-02-218			2
SC00R07P	I	10-02-318	10-05-101	10/3	
SC00R08N	G	10-02-216			2
SC00R08P	I	10-02-316	10-05-316	10/3	
SC00R09N	G	10-02-014			2
SC00R09P	I	10-02-114	10-05-201	10/3	
SC00R10N	G	10-02-208			2
SC00R10P	I	10-02-308	10-06-103	10/4	
SC00R11N	G	10-02-206			2
SC00R11P	I	10-02-306	10-06-312	10/4	
SC00R12N	G	10-02-204			2
SC00R12P	I	10-02-304	10-06-102	10/4	
SC00R13N	G	10-02-202			2
SC00R13P	I	10-02-302	10-06-316	10/4	
SC00R14N	G	10-02-200			2
SC00R14P	I	10-02-300	10-06-201	10/4	
SC00R15N	G	10-02-008			2
SC00R15P	I	10-02-108	10-06-109	10/4	
SC00R16N	G	10-02-006			2
SC00R16P	I	10-02-106	10-06-110	10/4	
SC00R17N	G	10-02-004			2
SC00R17P	I	10-02-104	10-06-104	10/4	
SC00R18N	G	10-02-002			2
SC00R18P	I	10-02-102	10-06-313	10/4	
SC00R19N	G	10-02-000			2
SC00R19P	I	10-02-100	10-06-101	10/4	
SC00S00N	G	10-17-013			2
SC00S00P	O	10-17-113	10-05-117	10/3	
SC00S01N	G	10-02-019			2
SC00S01P	O	10-02-119	10-05-114	10/3	
SC00S02N	G	10-17-218			2
SC00S02P	O	10-17-318	10-05-113	10/3	
SC00S03N	G	10-17-215			2
SC00S03P	O	10-17-315	10-05-112	10/3	
SC00S04N	G	10-02-017			2
SC00S04P	O	10-02-117	10-05-116	10/3	
SC00S05N	G	10-17-018			2
SC00S05P	O	10-17-118	10-05-115	10/3	
SC00S06N	G	10-17-015			2
SC00S06P	O	10-17-115	10-05-318	10/3	
SC00S07N	G	10-02-219			2
SC00S07P	O	10-02-319	10-05-111	10/3	
SC00S08N	G	10-02-217			2
SC00S08P	O	10-02-317	10-05-317	10/3	
SC00S09N	G	10-02-015			2
SC00S09P	O	10-02-115	10-05-118	10/3	
SC00S10N	G	10-02-209			2
SC00S10P	O	10-02-309	10-06-114	10/4	
SC00S11N	G	10-02-207			2
SC00S11P	O	10-02-307	10-06-113	10/4	
SC00S12N	G	10-02-205			2
SC00S12P	O	10-02-305	10-06-112	10/4	

ELEMENT IDENTIFIER (CONT)

G

I/O SUBCHANNELS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
SC00S13N	G	10-02-203			2
SC00S13P	O	10-02-303	10-06-317	10/4	
SC00S14N	G	10-02-201			2
SC00S14P	O	10-02-301	10-06-118	10/4	
SC00S15N	G	10-02-009			2
SC00S15P	O	10-02-109	10-06-115	10/4	
SC00S16N	G	10-02-007			2
SC00S16P	O	10-02-107	10-06-116	10/4	
SC00S17N	G	10-02-005			2
SC00S17P	O	10-02-105	10-06-117	10/4	
SC00S18N	G	10-02-003			2
SC00S18P	O	10-02-103	10-06-318	10/4	
SC00S19N	G	10-02-001			2
SC00S19P	O	10-02-101	10-06-111	10/4	
SC01R00N	G	11-06-36			2
SC01R00P	I	11-06-37	10-09-104	10/7	
SC01R01N	G	11-07-16			2
SC01R01P	I	11-07-17	10-09-103	10/7	
SC01R02N	G	11-07-36			2
SC01R02P	I	11-07-37	10-09-312	10/7	
SC01R03N	G	11-08-16			2
SC01R03P	I	11-08-17	10-09-102	10/7	
SC01R04N	G	11-08-36			2
SC01R04P	I	11-08-37	10-09-110	10/7	
SC01R05N	G	11-06-34			2
SC01R05P	I	11-06-35	10-09-109	10/7	
SC01R06N	G	11-07-14			2
SC01R06P	I	11-07-15	10-09-313	10/7	
SC01R07N	G	11-07-34			2
SC01R07P	I	11-07-35	10-09-101	10/7	
SC01R08N	G	11-08-14			2
SC01R08P	I	11-08-15	10-09-316	10/7	
SC01R09N	G	11-08-34			2
SC01R09P	I	11-08-35	10-09-201	10/7	
SC01R10N	G	11-09-26			2
SC01R10P	I	11-09-27	10-10-103	10/8	
SC01R11N	G	11-10-06			2
SC01R11P	I	11-10-07	10-10-312	10/8	
SC01R12N	G	11-10-26			2
SC01R12P	I	11-10-27	10-10-102	10/8	
SC01R13N	G	11-11-06			2
SC01R13P	I	11-11-07	10-10-316	10/8	
SC01R14N	G	11-11-26			2
SC01R14P	I	11-11-27	10-10-201	10/8	
SC01R15N	G	11-09-24			2
SC01R15P	I	11-09-25	10-10-109	10/8	
SC01R16N	G	11-10-04			2
SC01R16P	I	11-10-05	10-10-110	10/8	
SC01R17N	G	11-10-24			2
SC01R17P	I	11-10-25	10-10-104	10/8	
SC01R18N	G	11-11-04			2
SC01R18P	I	11-11-05	10-10-313	10/8	
SC01R19N	G	11-11-24			2
SC01R19P	I	11-11-25	10-10-101	10/8	
SC01S00N	G	11-06-26			2
SC01S00P	O	11-06-27	10-09-117	10/7	
SC01S01N	G	11-07-06			2
SC01S01P	O	11-07-07	10-09-114	10/7	
SC01S02N	G	11-07-26			2
SC01S02P	O	11-07-27	10-09-113	10/7	
SC01S03N	G	11-08-06			2
SC01S03P	O	11-08-07	10-09-112	10/7	
SC01S04N	G	11-08-26			2
SC01S04P	O	11-08-27	10-09-116	10/7	
SC01S05N	G	11-06-24			2
SC01S05P	O	11-06-25	10-09-115	10/7	

ELEMENT IDENTIFIER (CONT)

G

I/O SUBCHANNELS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
SC01S06N	G	11-07-04			2
SC01S06P	O	11-07-05	10-09-318	10/7	
SC01S07N	G	11-07-24			2
SC01S07P	O	11-07-25	10-09-111	10/7	
SC01S08N	G	11-08-04			2
SC01S08P	O	11-08-05	10-09-317	10/7	
SC01S09N	G	11-08-24			2
SC01S09P	O	11-08-25	10-09-118	10/7	
SC01S10N	G	11-09-16			2
SC01S10P	O	11-09-17	10-10-114	10/8	
SC01S11N	G	11-09-36			2
SC01S11P	O	11-09-37	10-10-113	10/8	
SC01S12N	G	11-10-16			2
SC01S12P	O	11-10-17	10-10-112	10/8	
SC01S13N	G	11-10-36			2
SC01S13P	O	11-10-37	10-10-317	10/8	
SC01S14N	G	11-11-16			2
SC01S14P	O	11-11-17	10-10-118	10/8	
SC01S15N	G	11-09-14			2
SC01S15P	O	11-09-15	10-10-115	10/8	
SC01S16N	G	11-09-34			2
SC01S16P	O	11-09-35	10-10-116	10/8	
SC01S17N	G	11-10-14			2
SC01S17P	O	11-10-15	10-10-117	10/8	
SC01S18N	G	11-10-34			2
SC01S18P	O	11-10-35	10-10-318	10/8	
SC01S19N	G	11-11-14			2
SC01S19P	O	11-11-15	10-10-111	10/8	
SC02R00N	G	10-16-218			2
SC02R00P	I	10-16-318	10-13-104	10/11	
SC02R01N	G	10-16-216			2
SC02R01P	I	10-16-316	10-13-103	10/11	
SC02R02N	G	10-16-214			2
SC02R02P	I	10-16-314	10-13-312	10/11	
SC02R03N	G	10-16-212			2
SC02R03P	I	10-16-312	10-13-102	10/11	
SC02R04N	G	10-16-210			2
SC02R04P	I	10-16-310	10-13-110	10/11	
SC02R05N	G	10-16-018			2
SC02R05P	I	10-16-118	10-13-109	10/11	
SC02R06N	G	10-16-016			2
SC02R06P	I	10-16-116	10-13-313	10/11	
SC02R07N	G	10-16-014			2
SC02R07P	I	10-16-114	10-13-101	10/11	
SC02R08N	G	10-16-012			2
SC02R08P	I	10-16-112	10-13-316	10/11	
SC02R09N	G	10-16-010			2
SC02R09P	I	10-16-110	10-13-201	10/11	
SC02R10N	G	10-16-208			2
SC02R10P	I	10-16-308	10-14-103	10/12	
SC02R11N	G	10-16-206			2
SC02R11P	I	10-16-306	10-14-312	10/12	
SC02R12N	G	10-16-204			2
SC02R12P	I	10-16-304	10-14-102	10/12	
SC02R13N	G	10-16-202			2
SC02R13P	I	10-16-302	10-14-316	10/12	
SC02R14N	G	10-16-200			2
SC02R14P	I	10-16-300	10-14-201	10/12	
SC02R15N	G	10-16-008			2
SC02R15P	I	10-16-108	10-14-109	10/12	
SC02R16N	G	10-16-006			2
SC02R16P	I	10-16-106	10-14-110	10/12	
SC02R17N	G	10-16-004			2
SC02R17P	I	10-16-104	10-14-104	10/12	
SC02R18N	G	10-16-002			2
SC02R18P	I	10-16-102	10-14-313	10/12	

ELEMENT IDENTIFIER (CONT)

G

I/O SUBCHANNELS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
SC02R19N	G	10-16-000			2
SC02R19P	I	10-16-100	10-14-101	10/12	
SC02S00N	G	10-16-219			2
SC02S00P	G	10-16-319	10-13-117	10/11	
SC02S01N	G	10-16-217			2
SC02S01P	O	10-16-317	10-13-114	10/11	
SC02S02N	G	10-16-215			2
SC02S02P	O	10-16-315	10-13-113	10/11	
SC02S03N	G	10-16-213			2
SC02S03P	O	10-16-313	10-13-112	10/11	
SC02S04N	G	10-16-211			2
SC02S04P	O	10-16-311	10-13-116	10/11	
SC02S05N	G	10-16-019			2
SC02S05P	O	10-16-119	10-13-115	10/11	
SC02S06N	G	10-16-017			2
SC02S06P	O	10-16-117	10-13-318	10/11	
SC02S07N	G	10-16-015			2
SC02S07P	O	10-16-115	10-13-111	10/11	
SC02S08N	G	10-16-013			2
SC02S08P	O	10-16-113	10-13-317	10/11	
SC02S09N	G	10-16-011			2
SC02S09P	O	10-16-111	10-13-118	10/11	
SC02S10N	G	10-16-209			2
SC02S10P	O	10-16-309	10-14-114	10/12	
SC02S11N	G	10-16-207			2
SC02S11P	O	10-16-307	10-14-113	10/12	
SC02S12N	G	10-16-205			2
SC02S12P	O	10-16-305	10-14-112	10/12	
SC02S13N	G	10-16-203			2
SC02S13P	O	10-16-303	10-14-317	10/12	
SC02S14N	G	10-16-201			2
SC02S14P	O	10-16-301	10-14-118	10/12	
SC02S15N	G	10-16-009			2
SC02S15P	O	10-16-109	10-14-115	10/12	
SC02S16N	G	10-16-007			2
SC02S16P	O	10-16-107	10-14-116	10/12	
SC02S17N	G	10-16-005			2
SC02S17P	O	10-16-105	10-14-117	10/12	
SC02S18N	G	10-16-003			2
SC02S18P	O	10-16-103	10-14-318	10/12	
SC02S19N	G	10-16-001			2
SC02S19P	O	10-16-101	10-14-111	10/12	

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 4A

BELL LABORATORIES

SD-1C900-01

GB4

PRINTED IN U. S. A.

12/13/76

CAD 1
UNIT SYMBOL

ELEMENT IDENTIFIER

H

EXTERNAL INTERRUPTS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
INTEN	G	01-27-32			2
INTEP	I	01-27-33	02-26-017	7/21	
INTFN	G	01-28-02			2
INTFP	I	01-28-03	02-26-018	7/21	
INTGN	G	01-28-12			2
INTGP	I	01-28-13	02-26-001	7/21	
INTHN	G	01-28-22			2
INTHP	I	01-28-23	02-26-002	7/21	
INTJN	G	01-28-32			2
INTJP	I	01-28-33	02-26-003	7/21	
INTKN	G	01-29-02			2
INTKP	I	01-29-03	02-26-201	7/21	
ISFO	O	02-26-009	02-26-009	7/21	
ISGO	O	02-26-111	02-26-111	7/21	
ISHO	O	02-26-011	02-26-011	7/21	
ISJO	O	02-26-110	02-26-110	7/21	
ISKO	O	02-26-212	02-26-212	7/21	
ITDCEBN	G	10-17-219			2
ITDCEBP	I	10-17-319	02-26-014	7/21	
ITOCOON	G	10-17-216			2
ITOCOOP	I	10-17-316	02-26-016	7/21	
ITTYEAN	G	10-17-019			2
ITTYEAP	I	10-17-119	02-26-013	7/21	
ITTYOCN	G	10-17-016			2
ITTYOCP	I	10-17-116	02-26-015	7/21	

ELEMENT IDENTIFIER

J

SYSTEM STATUS PANEL

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
FORCEN	I	10-17-011	02-26-210	7/21	
FORCEP	I	10-17-111	02-26-310	7/21	
MRFN	G	10-17-010			2
MRFP	I	10-17-110	02-26-202	7/21	

ELEMENT IDENTIFIER

K

MAINTENANCE CHANNEL

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
MCHRDN	I	01-28-01	02-26-107	9/1	
MCHRDP	I	01-27-31	02-26-007	9/1	
MCHSDN	G	01-28-20			2
MCHSDP	O	01-28-21	02-26-108	9/1	

3A CENTRAL CONTROL

DWG SIZE C2
ISSUE 4A

BELL LABORATORIES
SD-1C900-01
GB5
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CAD 1
UNIT SYMBOL

ELEMENT IDENTIFIER

L

CC POWER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
LKOFF1	O	10-28-119	06-06-315	7/20	
LPTKAB	O	10-28-315			
MNRO	O	10-28-113			
MNO	O	10-28-114			
NPAO	I	10-28-117	10-28-201	14/9	
PATO	I	10-28-215	10-28-215	14/9	
PA1	O	10-28-316	10-28-203	14/9	
PA1	O	10-28-310	10-28-203	14/9	
PKEY	O	10-28-312			
PKEYR	O	10-28-311			
PWRKAB	O	10-28-115			
PWRKABa	G	10-28-016			
PWRKABa	G	10-28-116			
PWRKAM	O	10-28-313			
PWRKAMa	G	10-28-314			
PWRLO	I	10-28-317			
PWROFFO	I	10-28-318	06-06-015	7/20	
12F046	O	10-28-214	10-28-214	14/9	
12F054AB	OI	02-01-210	02-01-109	14/1	
12F054AB	OI	02-01-109	02-01-109	14/1	X
12F054CD	OI	02-14-210	02-14-109	14/2	
12F054CD	OI	02-14-109	02-14-109	14/2	X
12F054EF	OI	02-44-109	02-44-109	14/3	
12F054EF	OI	02-44-210	02-44-109	14/3	2
12F058AB	OI	06-01-210	06-01-109	14/4	
12F058AB	OI	06-01-109	06-01-109	14/4	X
12F058CF	OI	06-44-210	06-44-109	14/6	
12F058CF	OI	06-44-109	06-44-109	14/6	2
12F058DE	OI	06-02-109	06-02-109	14/5	
12F058DE	OI	06-02-210	06-02-109	14/5	
12F062AB	OI	10-29-109	10-29-109	14/8	
12F062AB	OI	10-29-210	10-29-109	14/8	X
12F062C	OI	10-01-109	10-01-109	14/7	
12F070	O	10-28-213	10-28-213	14/9	
24V0AA8	P	10-28-218	10-28-218	14/9	
24V0AA9	P	10-28-110			
3F054A	O	02-01-009	02-01-009	14/1	X
3F054B	O	02-01-310	02-01-310	14/1	
3F054C	O	02-14-310	02-14-310	14/2	
3F054D	O	02-14-009	02-14-009	14/2	X
3F054E	O	02-44-009	02-44-009	14/3	
3F054F	O	02-44-310	02-44-310	14/3	2
3F058A	O	06-01-009	06-01-009	14/4	X
3F058B	O	06-01-310	06-01-310	14/4	
3F058C	O	06-44-009	06-44-009	14/6	2
3F058D	O	06-02-310	06-02-310	14/5	
3F058E	O	06-02-009	06-02-009	14/5	
3F058F	O	06-44-310	06-44-310	14/6	
3F062A	O	10-29-310	10-29-310	14/8	
3F062B	O	10-29-009	10-29-009	14/8	X
3F062C	O	10-01-009	10-01-009	14/7	
3G054A	O	02-01-008	02-01-008	14/1	X
3G054B	O	02-01-311	02-01-311	14/1	
3G054C	O	02-14-311	02-14-311	14/2	
3G054D	O	02-14-008	02-14-008	14/2	X
3G054E	O	02-44-008	02-44-008	14/3	
3G054F	O	02-44-311	02-44-311	14/3	2
3G058A	O	06-01-008	06-01-008	14/4	X
3G058B	O	06-01-311	06-01-311	14/4	
3G058C	O	06-44-008	06-44-008	14/6	2
3G058D	O	06-02-311	06-02-311	14/5	
3G058E	O	06-02-008	06-02-008	14/5	
3G058F	O	06-44-311	06-44-311	14/6	
3G062A	O	10-29-311	10-29-311	14/8	
3G062B	O	10-29-008	10-29-008	14/8	X
3G062C	O	10-01-008	10-01-008	14/7	

ELEMENT IDENTIFIER (CONT)

L

CC POWER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
3T054A	G	02-01-100	02-01-200	14/1	X
3T054A	G	02-01-101	02-01-200	14/1	X
3T054A	G	02-01-102	02-01-200	14/1	X
3T054A	G	02-01-103	02-01-200	14/1	X
3T054A	G	02-01-104	02-01-200	14/1	X
3T054A	G	02-01-105	02-01-200	14/1	X
3T054A	G	02-01-106	02-01-200	14/1	X
3T054A	G	02-01-107	02-01-200	14/1	X
3T054A	G	02-01-108	02-01-200	14/1	X
3T054B	G	02-01-319	02-01-319	14/1	
3T054B	G	02-01-313	02-01-319	14/1	
3T054B	G	02-01-312	02-01-319	14/1	
3T054B	G	02-01-316	02-01-319	14/1	
3T054B	G	02-01-315	02-01-319	14/1	
3T054B	G	02-01-211	02-01-319	14/1	
3T054B	G	02-01-314	02-01-319	14/1	
3T054B	G	02-01-318	02-01-319	14/1	
3T054B	G	02-01-317	02-01-319	14/1	
3T054C	G	02-14-211	02-14-319	14/2	
3T054C	G	02-14-319	02-14-319	14/2	
3T054C	G	02-14-315	02-14-319	14/2	
3T054C	G	02-14-314	02-14-319	14/2	
3T054C	G	02-14-313	02-14-319	14/2	
3T054C	G	02-14-312	02-14-319	14/2	
3T054C	G	02-14-318	02-14-319	14/2	
3T054C	G	02-14-317	02-14-319	14/2	
3T054C	G	02-14-316	02-14-319	14/2	
3T054D	G	02-14-103	02-14-200	14/2	X
3T054D	G	02-14-108	02-14-200	14/2	X
3T054D	G	02-14-100	02-14-200	14/2	X
3T054D	G	02-14-101	02-14-200	14/2	X
3T054D	G	02-14-102	02-14-200	14/2	X
3T054D	G	02-14-104	02-14-200	14/2	X
3T054D	G	02-14-105	02-14-200	14/2	X
3T054D	G	02-14-106	02-14-200	14/2	X
3T054D	G	02-14-107	02-14-200	14/2	X
3T054E	G	02-44-103	02-44-200	14/3	
3T054E	G	02-44-102	02-44-200	14/3	
3T054E	G	02-44-101	02-44-200	14/3	
3T054E	G	02-44-100	02-44-200	14/3	
3T054E	G	02-44-108	02-44-200	14/3	
3T054E	G	02-44-107	02-44-200	14/3	
3T054E	G	02-44-106	02-44-200	14/3	
3T054E	G	02-44-105	02-44-200	14/3	
3T054E	G	02-44-104	02-44-200	14/3	
3T054F	G	02-44-211	02-44-319	14/3	2
3T054F	G	02-44-312	02-44-319	14/3	2
3T054F	G	02-44-313	02-44-319	14/3	2
3T054F	G	02-44-318	02-44-319	14/3	2
3T054F	G	02-44-319	02-44-319	14/3	2
3T054F	G	02-44-314	02-44-319	14/3	2
3T054F	G	02-44-315	02-44-319	14/3	2
3T054F	G	02-44-316	02-44-319	14/3	2
3T054F	G	02-44-317	02-44-319	14/3	2
3T058A	G	06-01-102	06-01-200	14/4	X
3T058A	G	06-01-108	06-01-200	14/4	X
3T058A	G	06-01-100	06-01-200	14/4	X
3T058A	G	06-01-101	06-01-200	14/4	X
3T058A	G	06-01-104	06-01-200	14/4	X
3T058A	G	06-01-105	06-01-200	14/4	X
3T058A	G	06-01-106	06-01-200	14/4	X
3T058A	G	06-01-107	06-01-200	14/4	X
3T058A	G	06-01-103	06-01-200	14/4	X
3T058B	G	06-01-319	06-01-319	14/4	
3T058B	G	06-01-211	06-01-319	14/4	
3T058B	G	06-01-318	06-01-319	14/4	

ELEMENT IDENTIFIER (CONT)

L

CC POWER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
3T058B	G	06-01-317	06-01-319	14/4	
3T058B	G	06-01-316	06-01-319	14/4	
~~3T058B~~	G	~~06-01-315~~	06-01-319	14/4	
3T058B	G	06-01-314	06-01-319	14/4	
3T058B	G	06-01-313	06-01-319	14/4	
3T058B	G	06-01-312	06-01-319	14/4	
3T058C	G	06-44-100	06-44-200	14/6	2
3T058C	G	06-44-101	06-44-200	14/6	2
3T058C	G	06-44-102	06-44-200	14/6	2
3T058C	G	06-44-103	06-44-200	14/6	2
3T058C	G	06-44-104	06-44-200	14/6	2
3T058C	G	06-44-106	06-44-200	14/6	2
3T058C	G	06-44-107	06-44-200	14/6	2
3T058C	G	06-44-105	06-44-200	14/6	2
3T058C	G	09-37T-GDA	06-44-200	14/6	
3T058C	G	09-42T-GDC	06-44-200	14/6	
3T058C	G	06-44-108	06-44-200	14/6	2
3T058D	G	06-02-319	06-02-319	14/5	
3T058D	G	06-02-312	06-02-319	14/5	
3T058D	G	06-02-318	06-02-319	14/5	
3T058D	G	06-02-317	06-02-319	14/5	
3T058D	G	06-02-211	06-02-319	14/5	
3T058D	G	06-02-316	06-02-319	14/5	
3T058D	G	06-02-315	06-02-319	14/5	
3T058D	G	06-02-314	06-02-319	14/5	
3T058D	G	06-02-313	06-02-319	14/5	
3T058E	G	06-02-103	06-02-200	14/5	
3T058E	G	06-02-102	06-02-200	14/5	
3T058E	G	06-02-101	06-02-200	14/5	
3T058E	G	06-02-100	06-02-200	14/5	
3T058E	G	06-02-108	06-02-200	14/5	
3T058E	G	06-02-107	06-02-200	14/5	
3T058E	G	06-02-106	06-02-200	14/5	
3T058E	G	06-02-105	06-02-200	14/5	
3T058E	G	06-02-104	06-02-200	14/5	
3T058F	G	06-44-319	06-44-319	14/6	
3T058F	G	06-44-317	06-44-319	14/6	
3T058F	G	06-44-318	06-44-319	14/6	
3T058F	G	06-44-312	06-44-319	14/6	
3T058F	G	06-44-211	06-44-319	14/6	
3T058F	G	06-44-313	06-44-319	14/6	
3T058F	G	06-44-314	06-44-319	14/6	
3T058F	G	06-44-315	06-44-319	14/6	
3T058F	G	06-44-316	06-44-319	14/6	
3T062A	G	10-29-211	10-29-319	14/8	
3T062A	G	10-29-311	10-29-319	14/8	
3T062A	G	10-29-312	10-29-319	14/8	
3T062A	G	10-29-313	10-29-319	14/8	
3T062A	G	10-29-314	10-29-319	14/8	
3T062A	G	10-29-315	10-29-319	14/8	
3T062A	G	10-29-316	10-29-319	14/8	
3T062A	G	10-29-317	10-29-319	14/8	
3T062A	G	10-29-318	10-29-319	14/8	
3T062B	G	10-28-219	10-29-200	14/8	
3T062B	G	10-29-105	10-29-200	14/8	X
3T062B	G	10-29-101	10-29-200	14/8	X
3T062B	G	10-29-107	10-29-200	14/8	X
3T062B	G	10-29-100	10-29-200	14/8	X
3T062B	G	10-29-106	10-29-200	14/8	X
3T062B	G	10-29-103	10-29-200	14/8	X
3T062B	G	10-29-104	10-29-200	14/8	X
3T062B	G	10-28-319	10-29-200	14/8	
3T062B	G	10-29-102	10-29-200	14/8	X
3T062B	G	10-29-108	10-29-200	14/8	X
3T062C	G	10-01-108	10-01-200	14/7	
3T062C	G	10-01-100	10-01-200	14/7	

ELEMENT IDENTIFIER (CONT)

L

CC POWER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
3T062C	G	10-01-104	10-01-200	14/7	
3T062C	G	10-01-103	10-01-200	14/7	
3T062C	G	10-01-102	10-01-200	14/7	
3T062C	G	10-01-101	10-01-200	14/7	
3T062C	G	10-01-107	10-01-200	14/7	
3T062C	G	10-01-106	10-01-200	14/7	
3T062C	G	10-01-105	10-01-200	14/7	
3VG1028T	G	10-28-118	10-28-219	14/9	
3V054A	P	02-01-000	02-01-000	14/1	X
3V054A	P	02-01-007	02-01-000	14/1	X
3V054A	P	02-01-006	02-01-000	14/1	X
3V054A	P	02-01-005	02-01-000	14/1	X
3V054A	P	02-01-004	02-01-000	14/1	X
3V054A	P	02-01-003	02-01-000	14/1	X
3V054A	P	02-01-002	02-01-000	14/1	X
3V054A	P	02-01-001	02-01-000	14/1	X
3V054B	P	02-01-219	02-01-119	14/1	
3V054B	P	02-01-214	02-01-119	14/1	
3V054B	P	02-01-213	02-01-119	14/1	
3V054B	P	02-01-212	02-01-119	14/1	
3V054B	P	02-01-218	02-01-119	14/1	
3V054B	P	02-01-217	02-01-119	14/1	
3V054B	P	02-01-216	02-01-119	14/1	
3V054B	P	02-01-215	02-01-119	14/1	
3V054C	P	02-14-219	02-14-119	14/2	
3V054C	P	02-14-212	02-14-119	14/2	
3V054C	P	02-14-216	02-14-119	14/2	
3V054C	P	02-14-215	02-14-119	14/2	
3V054C	P	02-14-214	02-14-119	14/2	
3V054C	P	02-14-213	02-14-119	14/2	
3V054C	P	02-14-218	02-14-119	14/2	
3V054C	P	02-14-217	02-14-119	14/2	
3V054D	P	02-14-000	02-14-000	14/2	X
3V054D	P	02-14-007	02-14-000	14/2	X
3V054D	P	02-14-006	02-14-000	14/2	X
3V054D	P	02-14-005	02-14-000	14/2	X
3V054D	P	02-14-004	02-14-000	14/2	X
3V054D	P	02-14-003	02-14-000	14/2	X
3V054D	P	02-14-002	02-14-000	14/2	X
3V054D	P	02-14-001	02-14-000	14/2	X
3V054E	P	02-44-000	02-44-000	14/3	
3V054E	P	02-44-007	02-44-000	14/3	
3V054E	P	02-44-006	02-44-000	14/3	
3V054E	P	02-44-005	02-44-000	14/3	
3V054E	P	02-44-004	02-44-000	14/3	
3V054E	P	02-44-003	02-44-000	14/3	
3V054E	P	02-44-002	02-44-000	14/3	
3V054E	P	02-44-001	02-44-000	14/3	
3V054F	P	02-44-219	02-44-119	14/3	2
3V054F	P	02-44-218	02-44-119	14/3	2
3V054F	P	02-44-217	02-44-119	14/3	2
3V054F	P	02-44-216	02-44-119	14/3	2
3V054F	P	02-44-215	02-44-119	14/3	2
3V054F	P	02-44-214	02-44-119	14/3	2
3V054F	P	02-44-213	02-44-119	14/3	2
3V054F	P	02-44-212	02-44-119	14/3	2
3V058A	P	06-01-000	06-01-000	14/4	X

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	7D

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CAD 1

UNIT SYMBOL

ELEMENT IDENTIFIER (CONT)

L

CC POWER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
3V058A	P	06-01-007	06-01-000	14/4	X
3V058A	P	06-01-006	06-01-000	14/4	X
3V058A	P	06-01-005	06-01-000	14/4	X
3V058A	P	06-01-004	06-01-000	14/4	X
3V058A	P	06-01-003	06-01-000	14/4	X
3V058A	P	06-01-002	06-01-000	14/4	X
3V058A	P	06-01-001	06-01-000	14/4	X
3V058B	P	06-01-219	06-01-119	14/4	
3V058B	P	06-01-216	06-01-119	14/4	
3V058B	P	06-01-215	06-01-119	14/4	
3V058B	P	06-01-214	06-01-119	14/4	
3V058B	P	06-01-213	06-01-119	14/4	
3V058B	P	06-01-212	06-01-119	14/4	
3V058B	P	06-01-218	06-01-119	14/4	
3V058B	P	06-01-217	06-01-119	14/4	
3V058C	P	06-44-001	06-44-000	14/6	Z
3V058C	P	06-44-006	06-44-000	14/6	Z
3V058C	P	06-44-007	06-44-000	14/6	Z
3V058C	P	06-44-002	06-44-000	14/6	Z
3V058C	P	06-44-003	06-44-000	14/6	Z
3V058C	P	06-44-004	06-44-000	14/6	Z
3V058C	P	06-44-005	06-44-000	14/6	Z
3V058C	P	06-44-000	06-44-000	14/6	Z
3V058D	P	06-02-218	06-02-119	14/5	
3V058D	P	06-02-217	06-02-119	14/5	
3V058D	P	06-02-216	06-02-119	14/5	
3V058D	P	06-02-215	06-02-119	14/5	
3V058D	P	06-02-214	06-02-119	14/5	
3V058D	P	06-02-213	06-02-119	14/5	
3V058D	P	06-02-212	06-02-119	14/5	
3V058D	P	06-02-219	06-02-119	14/5	
3V058E	P	06-02-000	06-02-000	14/5	
3V058E	P	06-02-006	06-02-000	14/5	
3V058E	P	06-02-005	06-02-000	14/5	
3V058E	P	06-02-007	06-02-000	14/5	
3V058E	P	06-02-004	06-02-000	14/5	
3V058E	P	06-02-003	06-02-000	14/5	
3V058E	P	06-02-002	06-02-000	14/5	
3V058E	P	06-02-001	06-02-000	14/5	
3V058F	P	06-44-219	06-44-119	14/6	
3V058F	P	06-44-212	06-44-119	14/6	
3V058F	P	06-44-213	06-44-119	14/6	
3V058F	P	06-44-214	06-44-119	14/6	
3V058F	P	06-44-215	06-44-119	14/6	
3V058F	P	06-44-216	06-44-119	14/6	
3V058F	P	06-44-217	06-44-119	14/6	
3V058F	P	06-44-218	06-44-119	14/6	
3V062A	P	10-29-219	10-29-119	14/8	
3V062A	P	10-29-212	10-29-119	14/8	
3V062A	P	10-29-213	10-29-119	14/8	
3V062A	P	10-29-214	10-29-119	14/8	
3V062A	P	10-29-215	10-29-119	14/8	
3V062A	P	10-29-216	10-29-119	14/8	
3V062A	P	10-29-217	10-29-119	14/8	
3V062A	P	10-29-218	10-29-119	14/8	
3V062B	P	10-29-000	10-29-000	14/8	X
3V062B	P	10-29-002	10-29-000	14/8	X
3V062B	P	10-29-003	10-29-000	14/8	X
3V062B	P	10-29-004	10-29-000	14/8	X
3V062B	P	10-29-005	10-29-000	14/8	X
3V062B	P	10-29-006	10-29-000	14/8	X
3V062B	P	10-29-007	10-29-000	14/8	X
3V062B	P	10-29-001	10-29-000	14/8	X
3V062C	P	10-01-000	10-01-000	14/7	
3V062C	P	10-01-007	10-01-000	14/7	
3V062C	P	10-01-006	10-01-000	14/7	

ELEMENT IDENTIFIER (CONT)

L

CC POWER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
3V062C	P	10-01-005	10-01-000	14/7	
3V062C	P	10-01-004	10-01-000	14/7	
3V062C	P	10-01-003	10-01-000	14/7	
3V062C	P	10-01-002	10-01-000	14/7	
3V062C	P	10-01-001	10-01-000	14/7	
5T039A	G	10-28-111	10-28-200	14/9	
5V039A	P	10-28-112			
5V061A	P	09-36T-+5A	09-36T-+5A	14/23	
5V061B	P	09-38T-+5B	09-38T-+5B	14/25	2
5V061C	P	09-41T-+5C	09-41T-+5C	14/26	
5V061D	P	09-43T-+5D	09-43T-+5D	14/28	2

ELEMENT IDENTIFIER

M

CC OPTION(CC0 OR CC1)

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
3VG0618T	G	06-18-319	06-18-319	3/1	
3VG0618Y	I	06-18-117	06-18-117	5/4	
3VG0618Z	I	06-18-317	06-18-317	5/4	

ELEMENT IDENTIFIER

N

TIMING COUNTER OUTPUTS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
IST1.250	O	02-24-004	02-24-004	8/4	
IST10.00	O	02-24-201	02-24-201	8/4	
IST25.00	O	06-06-101	02-24-204	8/4	
IST5.00	O	02-24-308	02-24-308	8/4	

ELEMENT IDENTIFIER

P

INTERRUPT REGISTER INPUTS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
ISTTYE0	I	06-11-306	06-11-306	5/12	
ISTTY00	I	06-12-306	06-12-306	5/11	
ISUTIL0	I	06-10-106	06-10-106	5/13	
IS000	I	06-09-106	06-09-106	5/14	
IS020	I	06-11-106	06-11-106	5/12	
IS040	I	06-13-106	06-13-106	5/10	
IS060	I	06-16-106	06-16-106	5/8	
IS080	I	06-09-306	06-09-306	5/14	
IS090	I	06-10-306	06-10-306	5/13	
IS120	I	06-13-306	06-13-306	5/10	
IS140	I	06-16-306	06-16-306	5/8	
IS150	I	06-17-306	06-17-306	5/7	

ELEMENT IDENTIFIER

R

AUXILIARY PROCESSOR EXTERNAL INTERRUPTS

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
ISIN000	I	11-12-37			
ISIN010	I	11-13-07			
ISIN020	I	11-13-17			
ISIN040	I	11-13-27			
ISIN060	I	11-13-37			
ISIN120	I	11-14-07			
ISIN140	I	11-14-17			
ISIN150	I	11-14-27			

3A CENTRAL CONTROL

DWG SIZE C2

ISSUE 7D

BELL LABORATORIES

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CAD 2

CONTROL PANEL TERMINAL STRIP

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............J4				10-28	JACK/CP	(NOTE 3)..................			
TO CTLPNL CKT	LPTKBC	CA8	P2	300	MNRO	CAD 1			
|	LPTKBM	CA8	P2	301	MNO	CAD 1			
|	PKEYR	CA8	P3	302	PKEYR	CAD 1			
|	PKEY	CA8	P3	303	PKEY	CAD 1			
|	PWRKAM	CA8	CX1	304	PWRKAM	CAD 1			
|	PWRKAMG	CA8	CX1	305	PWRKAMG	CAD 1			
|	LPTKAB	CA8		306	LPTKAB	CAD 1			
|	PWRLO	CA8		307	PWRLO	CAD 1			
|	PWRKAB	CA8	P4	308	PWRKAB	CAD 1			
|	PWRKABG	CA8	P4	309	PWRKABG	CAD 1			
............J3				10-28	JACK/CP	(NOTE 3)..................			
TO CTLPNL CKT	PWRKBB	CA8		101	PWRKBB	02-20 CP	315		
|	+5V	CA8		107	5V039A	CAD 1			
|	GRDB	CA8	P1	108	PWRKABG	CAD 1			
|	+24V	CA8	P1	109	24V0AA9	CAD 1			

CAD 3

CONTROL PANEL TERMINAL STRIP

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............J1				10-20	JACK/CONN	(NOTE 5)..................			
TO CTLPNL CKT	SPLLO	CA1	FT	211	SPLLO	02-24 CP	301		
|	HALTLO	CA1	FT	212	HALTLO	06-14 CP	315		
|	0ISRKO	CA1	FT	213	0ISRKO	10-23 CP	312		
|	OFFL1	CA1	FT	215	OFFL1	06-13 CP	115		
|	STOPL1	CA1	FT	216	STOPL1	02-25 CP	210		
|	GRDA	CA1	FT	310	3VG1020T	10-20 CONN	010		
|	ROLO	CA1	FT	312	ROOLO	02-31 CP	203		
|	EA.DMTLO	CA1	FT	313	EA.DMTLO	02-23 CP	007		
|	LOADKO	CA1	FT	314	LOADKO	10-23 CP	213		
|	ONL1	CA1	FT	316	ONL1	06-06 CP	016		
|	MANL1	CA1	FT	317	MANL1	02-25 CP	303		
	NC			319	3VG1020T	10-20 CONN	019		
............J4				10-20	JACK/CONN	(NOTE 5)..................			
	NC			200	3VG1020B	10-20 CONN	300		
TO CTLPNL CKT	IADRKO	CA4	FT	201	IADRKO	10-22 CP	112		
|	0ISKO	CA4	FT	202	0ISMKO	10-22 CP	111		
|	RS4KO	CA4	FT	203	RS4KO	10-23 CP	104		
|	HILOKO	CA4	FT	204	HILOKO	10-22 CP	205		
|	HALTKO	CA4	FT	205	HALTKO	10-23 CP	304		
|	BAEXKO	CA4	FT	206	BAEXKO	10-23 CP	315		
|	GRDA	CA4	FT	300	3VG1020B	10-20 CONN	200		
|	COATKO	CA4	FT	301	CDAKTO	10-23 CP	110		
|	STOKO	CA4	FT	302	STOKO	10-22 CP	212		
|	RS8KO	CA4	FT	303	RS8KO	10-23 CP	012		
|	RS2KO	CA4	FT	304	RS2KO	10-23 CP	303		
|	RS1KO	CA4	FT	305	RS1KO	10-23 CP	003		
|	SPEPKO	CA4	FT	306	STEPKO	10-23 CP	004		
|	REJLO	CA4	FT	307	REJLO	06-14 CP	115		
............J2				10-20	JACK/CONN	(NOTE 4)..................			
	NC			010	3VG1020T	10-20 CONN	011		
	NC			011	3VG1020T	10-20 CONN	012		
	NC			012	3VG1020T	10-20 CONN	013		
TO CTLPNL CKT	TMKOG	CA7	CX1	013	3VG1020T	10-20 CONN	014		
|	MANKOG	CA7	CX2	014	3VG1020T	10-20 CONN	015		
|	RESK1G	CA7	CX3	015	3VG1020T	10-20 CONN	016		
|	RESKOG	CA7	CX4	016	3VG1020T	10-20 CONN	017		
|	EXECK1G	CA7	CX5	017	3VG1020T	10-20 CONN	018		
|	EXECKOG	CA7	CX6	018	3VG1020T	10-20 CONN	019		
	NC			019	3VG1020T	10-20 CONN	319		
TO CTLPNL CKT	TMKO	CA7	CX1	113	TMKOA	06-06 CP	114		
|	MANKO	CA7	CX2	114	MANKO	06-06 CP	314		
|	RESK1	CA7	CX3	115	RESK1	06-06 CP	311		
|	RESKO	CA7	CX4	116	RESKO	06-06 CP	111		
|	EXECK1	CA7	CX5	117	EXECK1	06-06 CP	011		

CAD 3

(CONT'D)

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............J2				10-20 (CONT'D)	JACK/CONN	(NOTE 4)..................			
|	EXECKO	CA7	CX6	118	EXECKO	06-06 CP	310		

CAD 4

CONTROL PANEL TERMINAL STRIP

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............J1				10-21	JACK/CONN	(NOTE 5)..................			
TO CTLPNL CKT	DB17LO	CA3	FT	211	DB17LO	10-22 CP	115		
|	DB15LO	CA3	FT	212	DB15LO	10-22 CP	018		
|	DB9LO	CA3	FT	213	DB09LO	10-23 CP	017		
|	DB11LO	CA3	FT	214	DB11LO	10-22 CP	014		
|	DB13LO	CA3	FT	215	DB13LO	10-22 CP	114		
|	DB19LO	CA3	FT	216	DB19LO	10-22 CP	318		
|	PHLO	CA3	FT	217	DBPHLO	10-22 CP	219		
|	PHKO	CA3	FT	218	IKPHO	10-22 CP	317		
|	GRDA	CA3	FT	310	3VG1021T	10-21 CONN	319		
|	MPLO	CA3	FT	311	MPLO	02-24 CP	104		
|	DB16LO	CA3	FT	312	DB16LO	10-22 CP	118		
|	DB14LO	CA3	FT	313	DB14LO	10-22 CP	218		
|	DB10LO	CA3	FT	314	DB10LO	10-22 CP	214		
|	DB12LO	CA3	FT	315	DB12LO	10-22 CP	215		
|	DB18LO	CA3	FT	316	DB18LO	10-22 CP	019		
|	PLLO	CA3	FT	317	D3PLLO	10-22 CP	315		
|	MPKO	CA3	FT	318	MPKO	10-23 CP	203		
	NC			319	3VG1021T	10-21 CONN	310		
............J2				10-21	JACK/CONN	(NOTE 5)..................			
TO CTLPNL CKT	R15LO	CA2	FT	011	R15LO	02-31 CP	106		
|	R13LO	CA2	FT	012	R13LO	02-31 CP	007		
|	R11LO	CA2	FT	013	R11LO	02-31 CP	008		
|	R9LO	CA2	FT	014	R09LO	02-31 CP	108		
|	R7LO	CA2	FT	015	R07LO	02-31 CP	103		
|	R5LO	CA2	FT	016	R05LO	02-31 CP	004		
|	R3LO	CA2	FT	017	R03LO	02-31 CP	104		
|	R1LO	CA2	FT	018	R01LO	02-31 CP	006		
|	GRDA	CA2	FT	110	3VG1021T	10-21 CONN	310		
|	PLKO	CA2	FT	111	IKPLO	10-22 CP	117		
|	R14LO	CA2	FT	112	R14LO	02-31 CP	306		
|	R12LO	CA2	FT	113	R12LO	02-31 CP	207		
|	R10LO	CA2	FT	114	R10LO	02-31 CP	208		
|	R8LO	CA2	FT	115	R08LO	02-31 CP	206		
|	R6LO	CA2	FT	116	R06LO	02-31 CP	303		
|	R4LO	CA2	FT	117	R04LO	02-31 CP	204		
|	R2LO	CA2	FT	118	R02LO	02-31 CP	305		
............J3				10-21	JACK/CONN	(NOTE 5)..................			
TO CTLPNL CKT	I16KO	CA5	FT	001	IK160	10-22 CP	116		
|	I5KO	CA5	FT	002	IK050	10-23 CP	013		
|	I7KO	CA5	FT	003	IK070	10-23 CP	309		
|	I9KO	CA5	FT	004	IK090	10-23 CP	310		
|	I11KO	CA5	FT	005	IK110	10-22 CP	211		
|	I13KO	CA5	FT	006	IK130	10-22 CP	012		
|	I15KO	CA5	FT	007	IK150	10-22 CP	216		
|	CADRKO	CA5	FT	008	CADRKO	10-23 CP	011		
|	GRDA	CA5	FT	100	3VG1021B	10-21 CONN	200		
|	I17KO	CA5	FT	101	IK170	10-22 CP	316		
|	I4KO	CA5	FT	102	IK040	10-23 CP	212		
|	I6KO	CA5	FT	103	IK060	10-23 CP	113		
|	I8KO	CA5	FT	104	IK080	10-23 CP	010		
|	I10KO	CA5	FT	105	IK100	10-22 CP	011		
|	I12KO	CA5	FT	106	IK120	10-22 CP	311		
|	I14KO	CA5	FT	107	IK140	10-22 CP	016		
|	SGKO	CA5	FT	108	SGKO	10-23 CP	112		

CAD 4

(CONT'D)

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............J4				10-21	JACK/CONN	(NOTE 5)..................			
	NC			200	3VC1021B	10-21 CONN	300		
TO CTLPNL CKT	DB7LO	CA6	FT	201	DB07LO	10-23 CP	016		
|	DB5LO	CA6	FT	202	DB05LO	10-23 CP	211		
|	DB1LO	CA6	FT	203	DB01LO	10-23 CP	102		
|	DB3LO	CA6	FT	204	DB03LO	10-23 CP	009		
|	I2KO	CA6	FT	206	IK020	10-23 CP	204		
|	I19KO	CA6	FT	207	IK190	10-22 CP	217		
|	I0KO	CA6	FT	208	IK000	10-23 CP	100		
|	GRDA	CA6	FT	300	3VG1021B	10-21 CONN	200		
|	DB8LO	CA6	FT	301	DB08LO	10-23 CP	217		
|	DB6LO	CA6	FT	302	DB06LO	10-23 CP	316		
|	DB0LO	CA6	FT	303	DB00LO	10-23 CP	302		
|	DB2LO	CA6	FT	304	DB02LO	10-23 CP	209		
|	DB4LO	CA6	FT	305	DB04LO	10-23 CP	111		
|	I3KO	CA6	FT	306	IK030	10-23 CP	311		
|	I1KO	CA6	FT	307	IK010	10-23 CP	103		
|	I18KO	CA6	FT	308	IK180	10-22 CP	017		

CAD 5

MAR MICROSTORE CONNECTOR

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............J1				07-41	JACK/CTF	....			
	0GD0643B			34	0GD0643B				315
	MAR0010			35	MAR0010	02-35 CP	303		315
............J1				07-42	JACK/CTF	....			
	0GD0643B			04	0GD0643B				315
	MAR0110			05	MAR0110	02-35 CP	104		315
	0GD0643B			14	0GD0643B				315
	MAR0210			15	MAR0210	02-35 CP	006		315
	0GD0643B			24	0GD0643B				315
	MAR0310			25	MAR0310	02-35 CP	305		315
	0GD0643B			34	0GD0643B				315
	MAR0410			35	MAR0410	02-35 CP	115		315
............J1				07-43	JACK/CTF	....			
	0GD0643B			04	0GD0643B				315
	MAR0510			05	MAR0510	02-34 CP	301		315
	0GD0643B			14	0GD0643B				315
	MAR0610			15	MAR0610	02-34 CP	300		315
	0GD0643B			24	0GD0643B				315
	MAR0710			25	MAR0710	02-34 CP	303		315
	0GD0643B			34	0GD0643B				315
	MAR0810			35	MAR0810	02-34 CP	302		315

3A CENTRAL CONTROL

OWG SIZE C2

ISSUE 4A

BELL LABORATORIES

SD-1C900-01

GB8

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12/13/76

CAD 6

TEST CONNECTORS#(SEE NOTE 212)

TO CONNECTION DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	FROM CONNECTION LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............TS8				10-26	CONNECTOR	(NOTE 7)..................			
	ER.F4080			201	ER.F4080	06-04 CP	103		
	ER.T4080			202	ER.T4080	02-02 CP	103		
	ERMARMT0			203	ERMARMT0	02-32 CP	301		
	ERMARPT0			204	ERMARPT0	02-31 CP	003		
	TR200			205	TR200	06-35 CP	214		
	TR100			206	TR100	06-35 CP	015		
	RU00			207	RU00	02-32 CP	002		
	DS00			208	DS00	06-35 CP	312		
	DR00B			209	DR00B	02-21 CP	107		
	CF00			210	CF00	06-35 CP	215		
	OPF00			211	OPF00	06-35 CP	313		
	ELNOP10B			212	ELNOP10B	02-33 CP	307		
	IFF11			214	IFF11	06-32 CP	008		
	P31			215	P31	06-31 CP	211		
	P21			216	P21	06-31 CP	018		
	P11			217	P11	06-31 CP	111		
	P01			218	P01	06-31 CP	009		
	SSBHC0A			301	SSBHC0A	06-10 CP	010		
	PT.MRF0			302	PT.MRF0	02-24 CP	208		
	MCTTMOC0			305	MCTTMOC0	06-29 CP	214		
	STPCLK0			306	STPCLK0	02-27 CP	112		
	MCTGCLK0			307	MCTGCLK0	02-27 CP	110		
	SSSTP0B			308	SSSTP0B	06-16 CP	210		
............TS9				10-27	CONNECTOR	(NOTE 7)..................			
	GBPL0			001	GBPL0	06-28 CP	010		
	GBPH0			002	GBPH0	06-28 CP	309		
	GB190			003	GB190	06-28 CP	117		
	GB180			004	GB180	06-28 CP	217		
	GB170			005	GB170	06-28 CP	017		
	GB160			006	GB160	06-28 CP	317		
	GB150			007	GB150	06-25 CP	213		
	GB140			008	GB140	06-25 CP	013		
	GB130			009	GB130	06-25 CP	201		
	GB120			010	GB120	06-25 CP	001		
	GB110			011	GB110	06-25 CP	100		
	GB100			012	GB100	06-25 CP	208		
	GB090			013	GB090	06-25 CP	108		
	GB080			014	GB080	06-25 CP	110		
	GB070			015	GB070	06-27 CP	213		
	GB060			016	GB060	06-27 CP	013		
	GB050			017	GB050	06-27 CP	201		
	GB040			018	GB040	06-27 CP	001		
	NC			200	3VG1027B	10-27 CONN	305		
	GR030			201	GB030	06-27 CP	100		
	GB020			202	GB020	06-27 CP	208		
	GB010			203	GB010	06-27 CP	108		
	GB000			204	GB000	06-27 CP	110		
	MAR0010T			205	MAR0010T				315
	MAR011DT			206	MAR011DT				315
	MAR021DT			207	MAR021DT				315
	MAR031DT			208	MAR031DT				315
	MAR041DT			209	MAR041DT				315
	MAR051DT			210	MAR051DT				315
	MAR061DT			211	MAR061DT				315
	MAR0710T			212	MAR0710T				315
	MAR0810T			213	MAR081DT				315
	MAR091			214	MAR091	02-34 CP	104		
	MAR101			215	MAR101	02-34 CP	006		
	MAR111			216	MAR111	02-34 CP	206		
	3VG1027B			305	3VG1027B	10-27 CONN	200		315
	3VG1027B			306	3VG1027B	10-27 CONN	305		315
	3VG1027B			307	3VG1027B	10-27 CONN	306		315
	3VG1027B			308	3VG1027B	10-27 CONN	307		315
	3VG1027B			309	3VG1027B	10-27 CONN	308		315
	3VG1027T			310	3VG1027T	10-27 CONN	311		315
	3VG1027T			311	3VG1027T	10-27 CONN	312		315
	3VG1027T			312	3VG1027T	10-27 CONN	313		315
	3VG1027T			313	3VG1027T	10-27 CONN	319		315
	NC			319	3VG1027T	10-27 CONN	313		

CAD 7

TO CONNECTION DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	FROM CONNECTION LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............+5A				09-36T	LUG	(NOTE 6)..................			
TO CONN CKT	5V061A			+5A	5V061A				
............GDA				09-37T	LUG	(NOTE 6)..................			
TO CONN CKT	3T058C			GDA	3T05 C				
............+5B				09-38T	LUG	(NOTE 6)..................			
	5V061A			+5B	5V061A	09-36T LUG	+5A	Y	
(2)TO CONN CKT	5V061B			+5B	5V061B			2	
............+5C				09-41T	LUG	(NOTE 6)..................			
TO CONN CKT	5V061C			+5C	5V061C				
............GDC				09-42T	LUG	(NOTE 6)..................			
TO CONN CKT	3T058C			GDC	3T058C				
............+50				09-43T	LUG	(NOTE 6)..................			
	5V061C			+50	5V061C	09-41T LUG	+5C	Y	
(2)TU CONN CKT	5V0610			+50	5V0610			2	
............GDD				09-44T	LUG	(NOTE 6)............. ...			
	NC			GDD	3T058C				

CAD 8

TEST CONNECTORS#(SEE NOTE 215)

TO CONNECTION DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	FROM CONNECTION LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
............TS4				10-18	CONNECTOR	(NOTE 7)..................			
	TSS0AC0			006	TSS0AC0	02-24 CP	205		
	SCM0			007	TSS0SCM0	02-24 CP	100		
	IFF.SBY0			008	TSS0BY0	02-24 CP	003		
	IO.ERC0			011	TSS0ERC0	02-23 CP	015		
	LNO.ERB0			012	TSS0ERB0	02-23 CP	315		
	BAK.ERA0			013	TSS0ERA0	02-23 CP	016		
	SG0.CC0			014	TSCC0	02-24 CP	103		
	SDPH0			015	TSSDEPH0	02-07 CP	117		
	SDPL0			016	TSSDEPL0	02-07 CP	317		
	3VG1018B			100	3VG1018B	10-18 CONN	200		
	3VG1018B			101	3VG1018B	10-18 CONN	100		
	3VG1018B			102	3VG1018B	10-18 CONN	101		
	3VG1018B			103	3VG1018B	10-18 CONN	102		
	3VG1018B			104	3VG1018B	10-18 CONN	103		
	3VG1018B			105	3VG1018B	10-18 CONN	104		
	3VG1018B			106	3VG1018B	10-18 CONN	105		
	3VG1018B			107	3VG1018B	10-18 CONN	106		
	3VG1018B			108	3VG1018B	10-18 CONN	107		
	3VG1018B			109	3VG1018B	10-18 CONN	108		
	3VG1018T			110	3VG1018T	10-18 CONN	310		
	3VG1018T			111	3VG1018T	10-18 CONN	110		
	3VG1018T			112	3VG1018T	10-18 CONN	111		
	3VG1018T			113	3VG1018T	10-18 CONN	112		
	3VG1018T			114	3VG1018T	10-18 CONN	113		
	3VG1018T			115	3VG1018T	10-18 CONN	114		
	3VG1018T			116	3VG1018T	10-18 CONN	115		
	3VG1018T			117	3VG1018T	10-18 CONN	116		
	3VG1018T			118	3VG1018T	10-18 CONN	117		
	3VG1018B			200	3VG1018B	10-18 CONN	100		
	SD150			201	TSSD310	02-07 CP	002		
	SD070			202	TSSD230	02-06 CP	306		
	S0140			203	TSSD300	02-07 CP	202		
	SD060			204	TSSD220	02-06 CP	201		
	SD130			205	TSSD290	02-07 CP	306		
	SD050			206	TSSD210	02-05 CP	117		

CAD 8

(CONT'D)

TO CONNECTION DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	FROM CONNECTION LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
.............TS4				10-18 (CONT'D)	CONNECTOR	(NOTE 7)..................			
	SD120			207	TSSD280	02-07 CP	201		
	SD040			208	TSSD200	02-05 CP	317		
	SD110			211	TSSD270	02-06 CP	117		
	SD030			212	TSSD190	02-05 CP	002		
	SD100			213	TSSD260	02-06 CP	317		
	SD020			214	TSSD180	02-05 CP	202		
	SD090			215	TSSD250	02-06 CP	002		
	SD010			216	TSSD170	02-05 CP	306		
	SD080			217	TSSD240	02-06 CP	202		
	SD000			218	TSSD160	02-05 CP	201		
	UTFR.1T0			219	C17.20	06-31 CP	103		
	3VG1018B			300	3VG1018B	10-18 CONN	301		
	3VG1018B			301	3VG1018B	10-18 CONN	302		
	3VG1018B			302	3VG1018B	10-18 CONN	303		
	3VG1018B			303	3VG1018B	10-18 CONN	304		
	3VG1018B			304	3VG1018B	10-18 CONN	305		
	3VG1018B			305	3VG1018B	10-18 CONN	306		
	3VG1018B			306	3VG1018B	10-18 CONN	307		
	3VG1018B			307	3VG1018B	10-18 CONN	308		
	3VG1018B			308	3VG1018B	10-18 CONN	309		
	3VG1018B			309	3VG1018B	10-18 CONN	109		
	3VG1018T			310	3VG1018T	10-18 CONN	311		
	3VG1018T			311	3VG1018T	10-18 CONN	312		
	3VG1018T			312	3VG1018T	10-18 CONN	313		
	3VG1018T			313	3VG1018T	10-18 CONN	314		
	3VG1018T			314	3VG1018T	10-18 CONN	315		
	3VG1018T			315	3VG1018T	10-18 CONN	316		
	3VG1018T			316	3VG1018T	10-18 CONN	317		
	3VG1018T			317	3VG1018T	10-18 CONN	318		
	3VG1018T			318	3VG1018T	10-18 CONN	319		
	3VG1018T			319	3VG1018T	10-18 CONN	318		

3A CENTRAL CONTROL

DWG SIZE	ISSUE
C2	6D

BELL LABORATORIES
SD-1C900-01
GB9

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CAD 8

(CONT'D)

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
..............TS5				10-19	CONNECTOR	(NOTE 7).................			
	TSSOCHO			006	TSSOCHO	02-24 CP	005		
	SCMO			007	TSSOSCMO	02-24 CP	100		
	IFF.SBYO			008	TSIFFO	06-35 CP	314		
	ID.ERCO			011	TSI.DO	02-24 CP	203		
	LNO.ERBO			012	TSLNOPO	02-31 CP	302		
	BAK.ERAO			013	TSBACKBO	02-25 CP	205		
	SGO.CCO			014	TSSOGOO	02-21 CP	208		
	SDPHO			015	TSSDPHO	02-18 CP	217		
	SDPLO			016	TSSDPLO	02-18 CP	114		
	3VG1019B			100	3VG1019B	10-19 CONN	200		
	3VG1019B			101	3VG1019B	10-19 CONN	100		
	3VG1019B			102	3VG1019B	10-19 CONN	101		
	3VG1019B			103	3VG1019B	10-19 CONN	102		
	3VG1019B			104	3VG1019B	10-19 CONN	103		
	3VG1019B			105	3VG1019B	10-19 CONN	104		
	3VG1019B			106	3VG1019B	10-19 CONN	105		
	3VG1019B			107	3VG1019B	10-19 CONN	106		
	3VG1019B			108	3VG1019B	10-19 CONN	107		
	3VG1019B			109	3VG1019B	10-19 CONN	108		
	3VG1019T			110	3VG1019T	10-19 CONN	310		
	3VG1019T			111	3VG1019T	10-19 CONN	110		
	3VG1019T			112	3VG1019T	10-19 CONN	111		
	3VG1019T			113	3VG1019T	10-19 CONN	112		
	3VG1019T			114	3VG1019T	10-19 CONN	113		
	3VG1019T			115	3VG1019T	10-19 CONN	114		
	3VG1019T			116	3VG1019T	10-19 CONN	115		
	3VG1019T			117	3VG1019T	10-19 CONN	116		
	3VG1019T			118	3VG1019T	10-19 CONN	117		
	3VG1019B			200	3VG1019B	10-19 CONN	100		
	SD150			201	TSS0150	02-17 CP	217		
	SD070			202	TSS0070	02-17 CP	114		
	SD140			203	TSS0140	02-16 CP	217		
	SD060			204	TSSD060	02-16 CP	114		
	S0130			205	TSSD130	02-13 CP	217		
	SD050			206	TSSD050	02-13 CP	114		
	SD120			207	TSSD120	02-12 CP	217		
	S0040			208	TSS0040	02-12 CP	114		
	SD110			211	TSSD110	02-11 CP	217		
	SD030			212	TSSD030	02-11 CP	114		
	SD100			213	TSSD100	02-10 CP	217		
	SD020			214	TSSD020	02-10 CP	114		
	SD090			215	TSSD090	02-09 CP	217		
	SD010			216	TSSD010	02-09 CP	114		
	SD080			217	TSSD080	02-08 CP	217		
	SD000			218	TSSD000	02-08 CP	114		
	UTFR.ITO			219	UTLFRZO	06-16 CP	109		
	3VG1019B			300	3VG1019B	10-19 CONN	301		
	3VG1019B			301	3VG1019B	10-19 CONN	302		
	3VG1019B			302	3VG1019B	10-19 CONN	303		
	3VG1019B			303	3VG1019B	10-19 CONN	304		
	3VG1019B			304	3VG1019B	10-19 CONN	305		
	3VG1019B			305	3VG1019B	10-19 CONN	306		
	3VG1019B			306	3VG1019B	10-19 CONN	307		
	3VG1019B			307	3VG1019B	10-19 CONN	308		
	3VG1019B			308	3VG1019B	10-19 CONN	309		
	3VG1019B			309	3VG1019B	10-19 CONN	109		
	3VG1019T			310	3VG1019T	10-19 CONN	311		
	3VG1019T			311	3VG1019T	10-19 CONN	312		
	3VG1019T			312	3VG1019T	10-19 CONN	313		
	3VG1019T			313	3VG1019T	10-19 CONN	314		
	3VG1019T			314	3VG1019T	10-19 CONN	315		
	3VG1019T			315	3VG1019T	10-19 CONN	316		
	3VG1019T			316	3VG1019T	10-19 CONN	317		
	3VG1019T			317	3VG1019T	10-19 CONN	318		
	3VG1019T			318	3VG1019T	10-19 CONN	319		
	3VG1019T			319	3VG1019T	10-19 CONN	318		

3A CENTRAL CONTROL

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